Fractional Gain Control Technique for a Low-Jitter and Area-Efficient Digital Phase-Locked Loop

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Abstract

This paper presents a fractional gain-control technique for a digitally controlled oscillator (DCO). The proposed fine-fractional gain-control scheme improves the jitter performance by suppressing the nonlinear effect of a bang-bang digital phase-locked loop (BB-DPLL). In addition, the proposed structure significantly reduces the chip area, because the proposed fractional DCO dithering circuit requires only one accumulator with an N-2-bit width, while conventional topologies require multiple accumulators with N-bit widths. The simulation result shows that the period jitter of the proposed structure (0.83 ps) is three times better than that of a digital PLL based on a conventional second-order sigma-delta modulator (2.58 ps).

Keywords*: Digitally controlled oscillator; jitter; phase-locked loop; sigma-delta modulation*

1. Introduction

Among several essential building blocks for a system-on-chip (SoC) circuit, the phase-locked loop (PLL) is widely used as a clock generator for CPU, DAC, ADC, and memory components, as shown in Figure 1. In response to the high performance requirements of SoC applications, the deep submicron CMOS process is considered as an attractive device technology due to its fast switching speed, low power consumption, small chip area, and low cost. However, analog circuit designs are at present faced with difficulties as their designers attempt to maintain the same noise and gain performance levels given the reduced voltage headroom available with advanced CMOS processes. In addition, the analog PLL occupies large chip area due to passive components such as resistors and capacitors, and the leakage current through the capacitor significantly degrades the performance. In contrast, the digital PLL has a smaller chip area because passive components are eliminated. Furthermore, the logic synthesis feature of the digital PLL reduces the design time and has better programmability, portability, and testability when the PLL is converted to different CMOS process technologies. As a result, digital PLLs have recently gained broad interest as an alternative to conventional analog charge-pump based PLLs [1-15].

In recent years, the bang-bang digital PLL (BB-DPLL) has been widely researched as an attractive topology for a clock generator for SoC applications owing to its simple implementation and small area [9-15]. Figure 2 shows a top-level diagram of a conventional BB-DPLL. In the conventional digital PLL, a sigma-delta modulator, which produces high-speed dithering streams to improve the effective frequency resolution of a digitally controlled oscillator (DCO), is used for the fractional dithering circuit. To suppress spurious tones, digital PLLs adopt the high-order sigma-delta modulator which randomizes dithering streams [2, 11, 12].
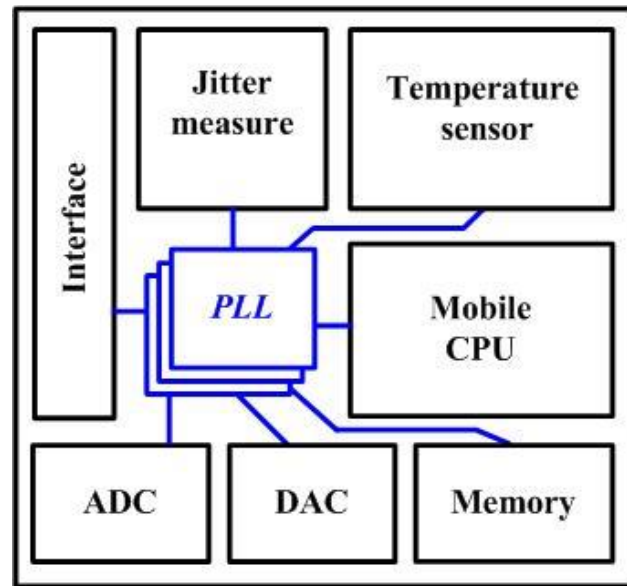
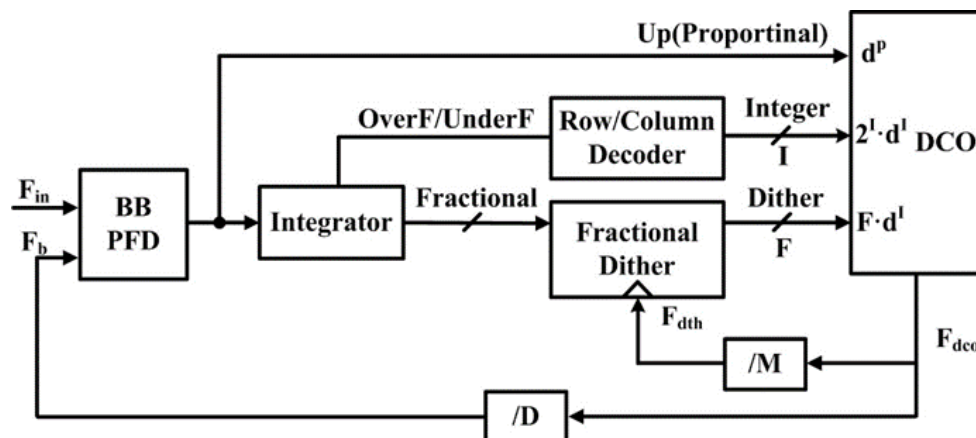**Figure 1. Block Diagram of a Mobile Application Processor**

Figure 2. Top-Level Diagram of a Conventional BB-DPLL

Among several DCO topologies, a ring-based DCO circuit with a large unit gain is most commonly adopted to achieve a wide frequency-locking range, a small chip area, and a fast lock time for the clock generator [10-14]. However, when the high-order sigma-delta modulator is applied to a ring-based DCO with a large unit gain, its quantization noise becomes the dominant contributor to increase the jitter and PLL phase noise in the high-frequency offset region. In addition, after the digital PLL is locked, the proportional (d^P) and fractional dither ($F \cdot d^I$) units are changed with bounds and therefore generate deterministic jitter. Therefore, in the conventional BB-DPLL, a larger unit gain eventually degrades the total period jitter of a BB-DPLL [14].

In this paper, a newly proposed fractional DCO dithering technique which divides the range of the fractional bit and controls the dither unit with a reduced gain is introduced [15]. The proposed finer fractional gain control scheme improves the jitter performance and significantly reduces the chip area. Section II describes the conventional high-order sigma-delta modulator for fractional DCO dithering topologies. Section III describes the operation principle and implementation of the proposed fractional gain control technique. For the verification and comparison, simulation results are also shown in Section III. Finally, Section V summarizes and concludes the findings of this paper.

2. Conventional DCO Dithering for a Fractional Gain Control

Figure 3 shows a second-order MASH sigma-delta modulator. Dithering streams of a high-order MASH sigma-delta modulator have been widely used not only to improve the effective frequency resolution but also to remove spurious tones of the DCO [1-11]. However, a wide dithering range of a high-order sigma-delta modulator increases the deterministic jitter; for instance, second and third-order sigma-delta modulators have maximal dithering gain ranges of $3 \times d^I$ and $5 \times d^I$, respectively [14]. The deterministic jitter caused by the fractional multi-dithering bits becomes the dominant noise source of the total period jitter for the digital PLL. On the other hand, although the first-order sigma-delta modulator dithers only one unit gain (d^I) of the DCO, its periodic output pattern generates fractional spurious tones in the DCO output phase noise. Moreover, assuming that the limited cycle noise due to the proportional gain (d^P) is ignored, the deterministic jitter of a first-order sigma-delta modulator is still the dominant contributor to the total amount of jitter of the digital PLL, under the large unit control gain of the DCO [14].
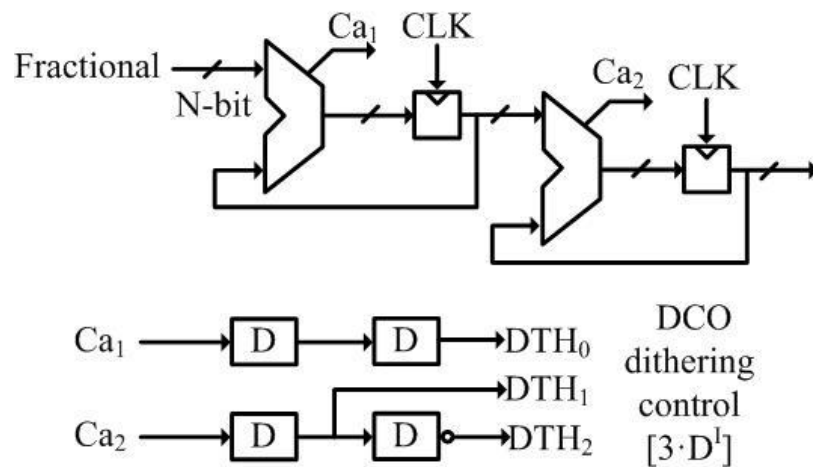

Figure 3. Second-Order MASH Sigma Delta Modulator

3. Operation Principle and Implementation

Figure 4 shows a block diagram of the proposed DCO dithering circuit for finer fractional gain control. The proposed DCO dithering circuit consists of a range detector, an adder, an accumulator, and MUXs. In the proposed circuit shown in Figure 2, an input fractional bit (Fractional) comes from the integrator, and the outputs of DTH_0, DTH_1, DTH_2, and DTH_3 connect to the DCO control units, whose gains are a quarter of that of the integer gain d^I, to improve the effective frequency resolution.
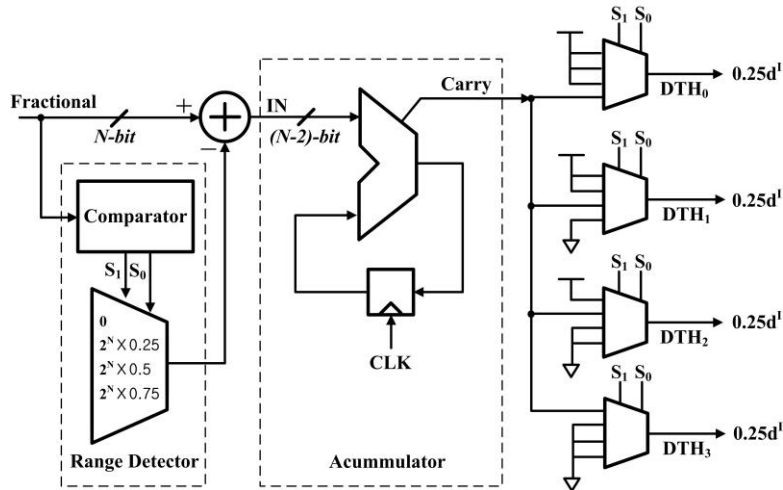
Figure 4. Block Diagram of the Proposed Fractional DCO Dithering Circuit
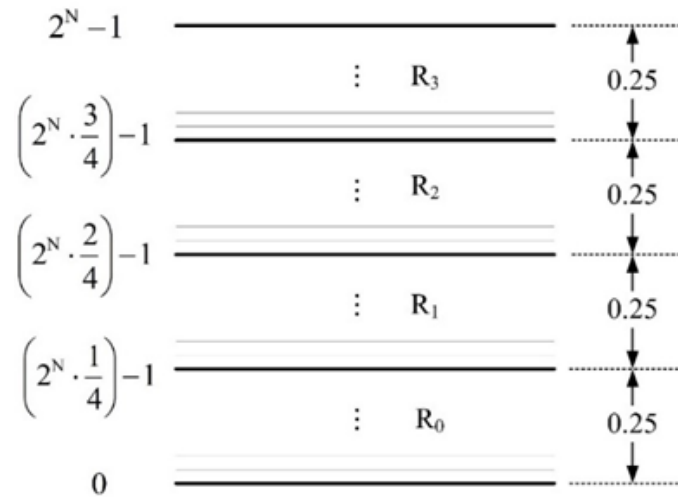

Figure 5. Division Range of the Range Detector with an N-Bit Width

Figure 5 illustrates the division range of the range detector with the N-bit width, and Table 1 shows its output values produced by the input fractional-bit. The comparator compares the input fractional bit with the division ranges (R_0~R_3) and generates S_0 and S_1, which control the selection signals of the MUXs. The next step is to subtract the selected output value of the MUX in the range detector from the input fractional bit.

It becomes the input of the accumulator input (IN) with a maximal N-2-bit width, as depicted in Figure 4. The time-averaged output carry of the accumulator becomes the normalized fractional value $IN/2^{N-2}$. According to the control signals (S_0 and S_1), the four MUXs on the right side of Figure 4 select one of three inputs, which are in this case 0, 1, and the output carry of the accumulator, as shown in Table 1. Finally, the four outputs of the MUXs (DTH_0, DTH_1, DTH_2, and DTH_3) generate the fractional value of the DCO by controlling one dither unit with a $0.25d^I$ gain.

Table 1. Values of S_0, S_1, IN, DTH_0, DTH_1, DTH_2 and DTH_3

Range	S_0	S_1	IN	DTH_0	DTH_1	DTH_2	DTH_3
R_0	0	0	Frac	$IN/2^{N-2}$	0	0	0
R_1	0	1	Frac-$(2^N \times 0.25)$	1	$IN/2^{N-2}$	0	0
R_2	1	0	Frac-$(2^N \times 0.5)$	1	1	$IN/2^{N-2}$	0
R_3	1	1	Frac-$(2^N \times 0.75)$	1	1	1	$IN/2^{N-2}$

From Table 1, the time-averaged fractional value produced by the proposed DCO dithering circuit can be expressed as follows:

$$DCO_{frac} = \left[DTH_0 + DTH_1 + DTH_2 + DTH_3 \right] \times d^I/4 \qquad (1)$$

For example, when the input fractional bit is 50 with a maximal 6-bit width, the range detector selects values in the range of R_3 such that DTH_0, DTH_1, and DTH_2 are 1, and DTH_3 is $(50-48)/2^{6-2}$. Therefore, DCO_{frac} becomes $(3+2/16) \times d^I/4$, which is equal to the normalized fractional value $[(50/64) \times d^I)]$ of the input. In this case, the three dithering outputs of DTH_0, DTH_1, and DTH_2 are fixed at a constant value of 1, but only DTH_3 dithers the fractional control unit of the DCO. The maximal fractional dithering range of the proposed DCO is $1/4 \times d^I$, as shown in Figure 4, while that of the second-order sigma-delta modulator, shown in Figure 3, is $3 \times d^I$. As a result, the proposed DCO dithering technique can significantly reduce both the deterministic and the total period jitter of the digital PLL compared to a second-order sigma-delta modulator. Furthermore, the conventional second-order sigma-delta modulator requires two series-connected accumulators with an N-bit width, as shown in Figure 3. However, the proposed scheme shown in Figure 4 consists of only one accumulator with an N-2-bit width. Therefore, the proposed DCO dithering structure also has the good features of ease of implementation, a small chip area, and a higher sampling clock operation.

Figure 6 shows the simulated period jitter of first-order and second-order sigma-delta modulators and the proposed fractional dithering circuit-based digital PLLs using the CppSim simulator [16]. The simulation results in Figure 5 are achieved from the BB-DPLL structure shown in Figure 2 with the following parameters: d^I = 3 MHz and d^P = 600 KHz. The input reference frequency (Fin) is 10 MHz, with a 6-bit width of the sigma-delta modulator, the natural DCO phase noise is -94dBc/Hz at a 1 MHz offset, and the frequency division value (D) is 92.
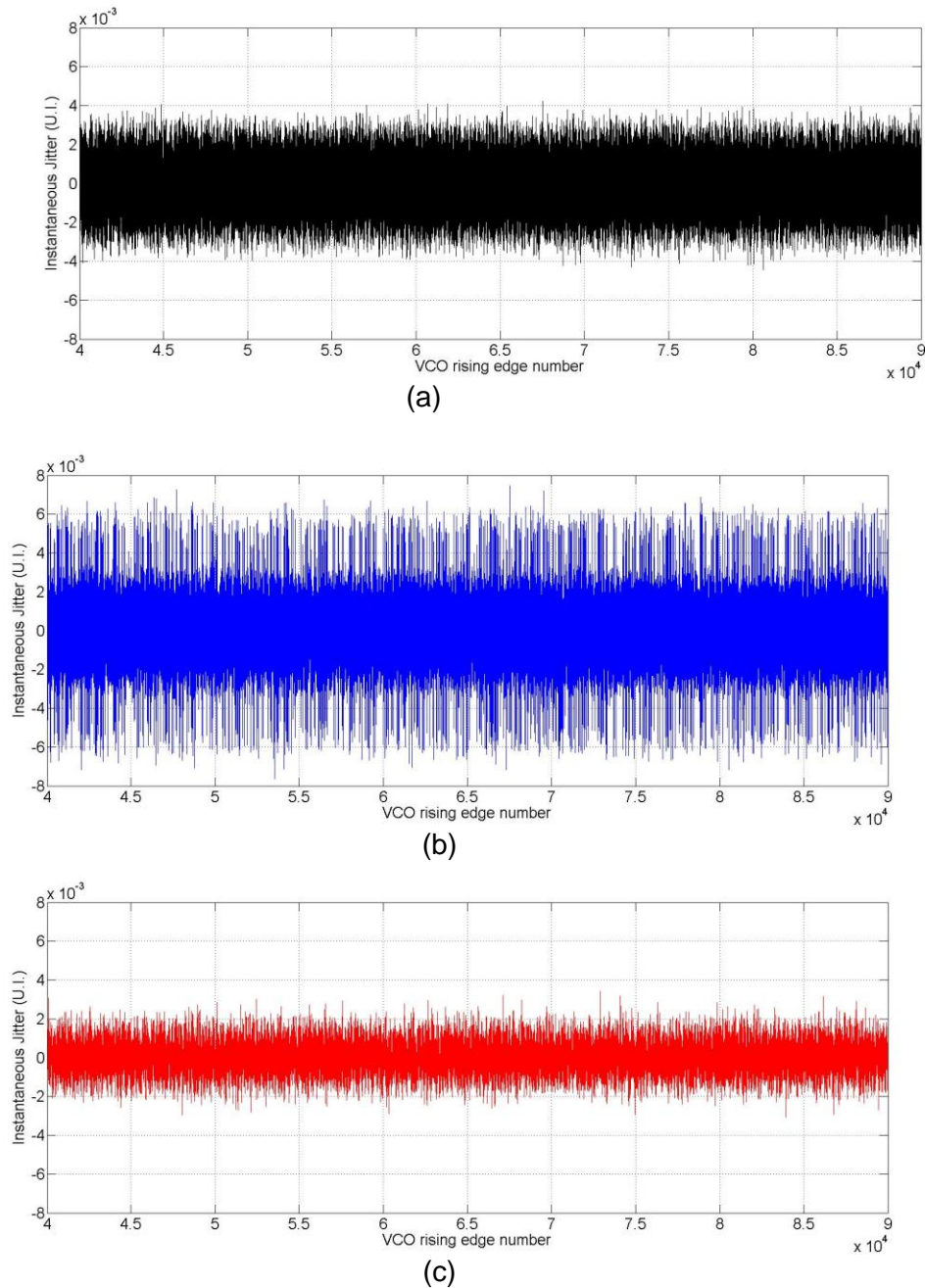
(a)

(b)

(c)

Figure 6. Simulated Period Jitter Of (A) A Conventional First-Order Sigma-Delta Modulator, (B) A Second-Order Sigma-Delta Modulator, and (C) The Proposed Digital PLL Based on a Fractional Dithering Circuit

The frequency division value, M, is 4, which results in an Fdth value of 230 MHz. As shown in Figure 6, the total period RMS jitter values of the digital PLLs based on the first- and second-order sigma-delta modulators are 1.93 and 2.58 ps, respectively, while that of the proposed dithering circuit-based digital PLL is 0.83 ps, which is approximately three times better than that of the digital PLL based on the conventional second-order sigma-delta modulator.
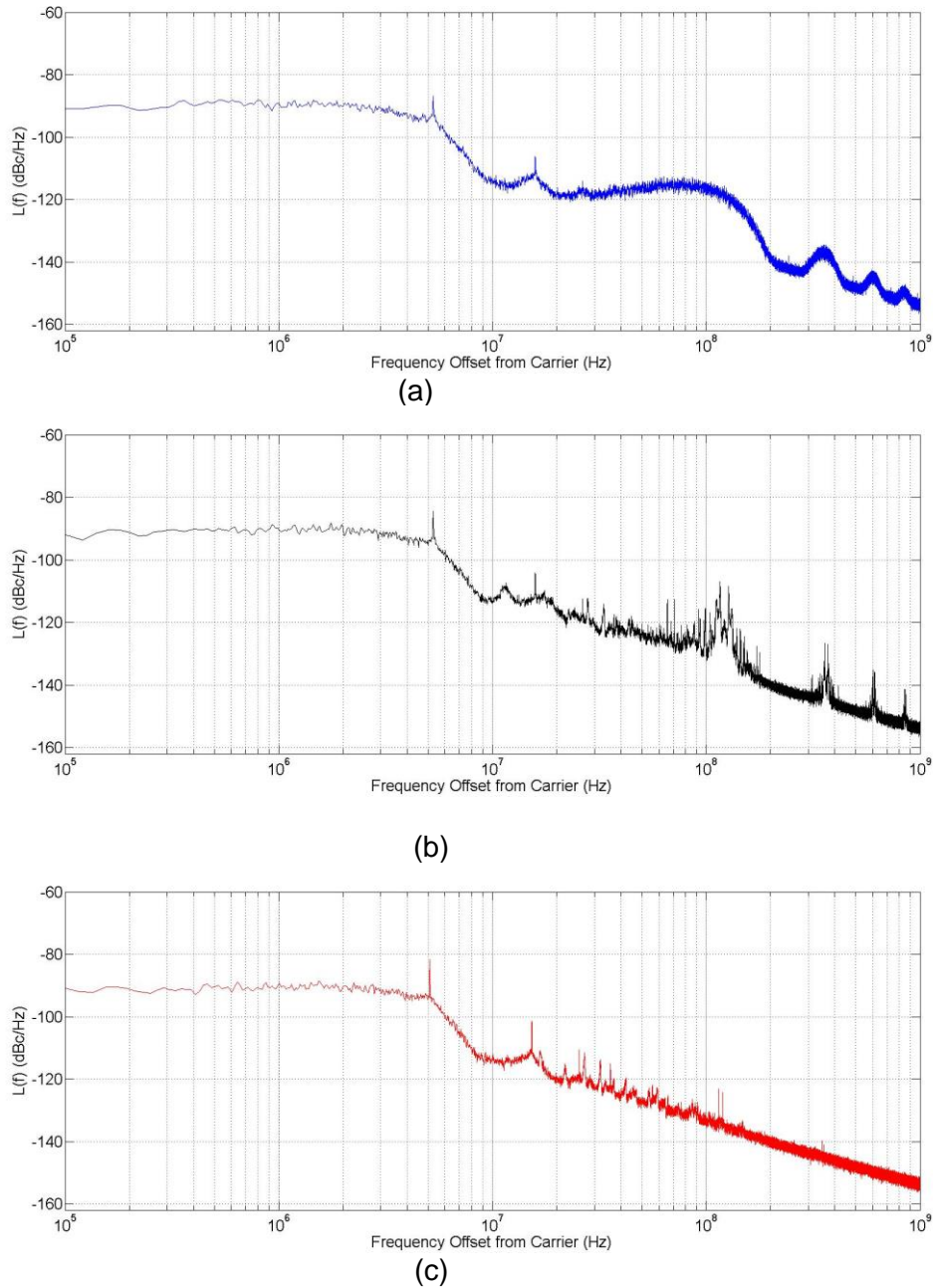
Figure 7. Simulated Phase Noise of Digital PLLs Based on (A) a Conventional First-Order Sigma-Delta Modulator, (B) a Second-Order Sigma-Delta Modulator, And (C) the Proposed Fractional Dithering Circuit

Figure 7 shows the simulated phase noise of the first- and second-order sigma-delta modulators, as well as the proposed fractional dithering circuit-based digital PLLs, using the CppSim simulator. As shown in Figure 7, the spurious tones and high-frequency quantization noise of the first- and second-order sigma-delta modulators significantly degrades the DCO phase noise at the high-frequency offset range, whereas the proposed dithering circuit shows much less noise degradation due to the reduced fractional gain. Table 2 shows the results of a performance comparison between the conventional second-order sigma-delta modulator and the proposed DCO dithering circuit-based digital PLL.

Table 2. Performance Comparison of Two DCO Dithering Circuits

	Bit-width of Accum.	Number of Accum.	Control Gain	RMS Jitter (ps)	Area
Second sigma-delta modulator	N	2	$3 \times d^I$	2.58	1
This work	N-2	1	$0.25 \times d^I$	0.83	1/8

4. Conclusion

This paper reports a new DCO dithering technique for fractional gain control. The proposed finer fractional gain control circuit significantly reduces the maximal dithering range. In addition, the proposed topology is implemented with an accumulator with an N-2-bit width, while the conventional high-order sigma-delta modulator structure requires multiple series-connected accumulators with an N-bit width. As a result, a digital PLL with the proposed fractional DCO dithering circuit offers less jitter and a smaller chip size. Simulation results verified the improved jitter performance in the proposed digital PLL compared to that of a digital PLL based on conventional high-order sigma-delta modulators. The proposed fractional DCO dithering circuit can be used for improved area efficiency and as a low jitter clock generator for SoC applications.

Acknowledgements

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