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Development of Machine Vision Monitoring System for Semiconductor Package Sorter

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Abstract

The sorter working at high speed in semiconductor production process has been a main reason for productivity failure, causing equipment failure and process halt as socket full or full status of the semiconductor package is not monitor in loading and unloading work of the semiconductor package of test socket board. Furthermore, it is necessary to promptly control vacuum to load and unload semiconductor package at high speed, but delicate on/off control error and limitation of engineer's bare eye checking are not free form error to package sorting. Therefore, the present study developed sorter process-focused image (video) processing algorithm and hardware-based MVMS to apply to production lines.

Keywords*: Sorter, Semiconductor package, Machine vision monitoring, Test socket board, Image processing*

1. Introduction

Semiconductor-related technologies have recently been developed toward realizing high-density and high-speed motion, reducing production cost to secure price competitiveness at the same time. In addition, as diameter enlargement, which is the main trend of semiconductor process equipment, gets more obvious, efforts are demanded to be made to improve the stagnation of long-term yield and productivity in semiconductor production process.

Sorter, which works in a high speed in semiconductor production process, has been a main reason for productivity failure, causing equipment failure and process halt due to package double phenomenon as socket full or full status of the semiconductor package is not monitor in loading and unloading work of the semiconductor package of test socket board. Furthermore, it is necessary to promptly control vacuum to load and unload semiconductor package at high speed, but delicate on/off control error and limitation of engineer's bare eye checking are not free form error to package sorting.

Therefore, the present study developed sorter process-focused image (video) processing algorithm and hardware-based MVMS (Machine Vision Monitoring System) to apply to production lines. This system enables to notify a process engineer in remote distance of the status of high-speed sorter without delay and helps him to take a proper action such as prompt correction and readjustment of equipment.

2. Composition of MVMS

The sorter working at high speed in semiconductor production process has been a main reason for productivity failure, causing equipment failure and process halt as socket full or full status of the semiconductor package is not monitor in loading and unloading work of the semiconductor package of test socket board. Furthermore, it is necessary to promptly control vacuum to load and unload semiconductor package at high speed, but

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delicate on/off control error and limitation of engineer's bare eye checking are not free form error to package sorting.

The system that this study aims for, as seen in Figure 1, consists of vision camera, image processing, sensor, communication unit, and machine control unit applied with algorithm specialized in controlling MVMS.

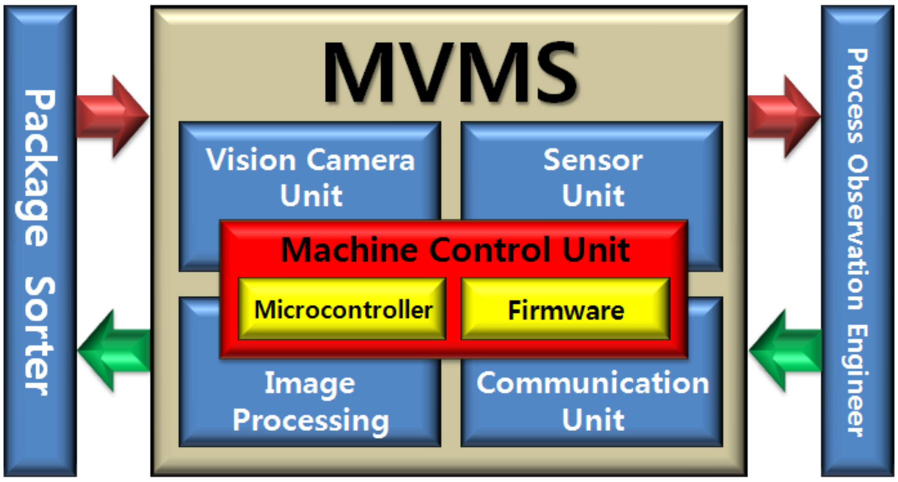

Figure 1. MVMS (Machine Vision Monitoring System) Structure

2.1. Sorter Motion Sequence and Operating Control Structure

Figure 2, 3 and 4 show 3 motion sequences divided by loading/unloading motion of a sorter.

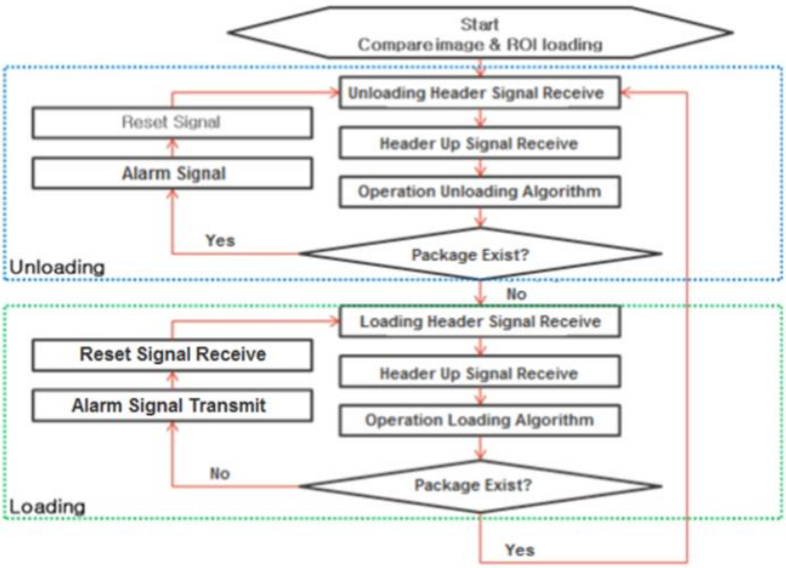

Figure 2. Loading/Unloading Sequence when Operating at the Same Time

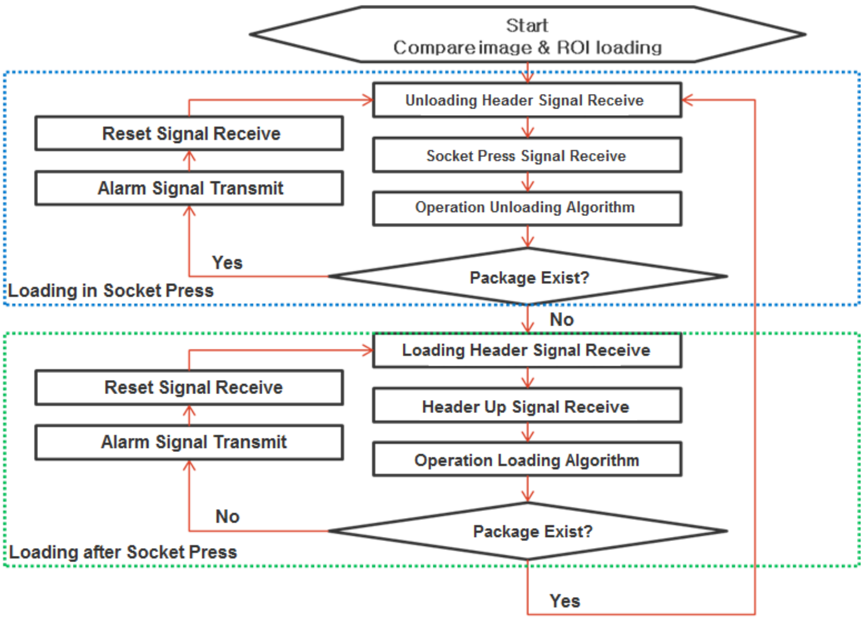

Figure 3. Sequence only when Loading Operation

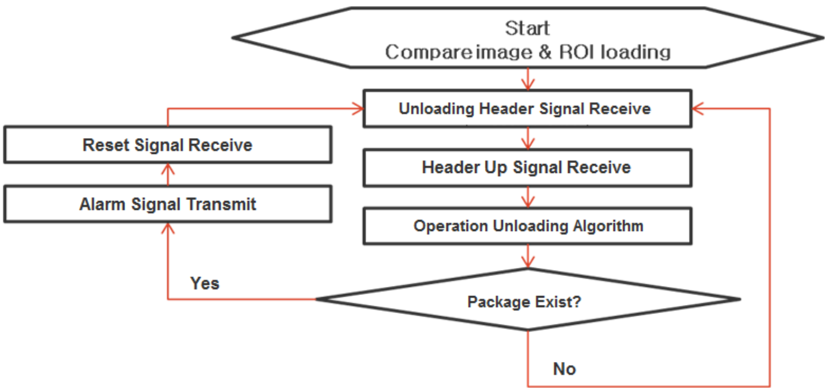

Figure 4. Sequence only when Unloading Operation

To develop vision recognition algorithm, this study examined the possible problems when existing algorithm is applied and defined the size, type and color of the chips used for the equipment. And it reviewed histogram method to analyze image and individual video information and develop an algorithm to normalize acquired images for work and multi-channel images. The developed algorithm is able to recognize in various environments (light sources). This system was designed in consideration of the computational speed and adequacy of the algorithm to be applied. Figure 5 shows the conceptual diagram of the system to handle visions.

Figure 5. Conceptual Diagram of Vision Processing

As seen in Figure 6, the motion structure of MVMS is that it uses machine vision to detect the presence of memory in the memory package socket and delivers information of the memory to memory package test equipment. The test equipment uses its own OS to analyze (with its software) machine control and data and transmits signals to control the equipment to the machine vision system.

Figure 6. MVMS Operating Control Structure

2.2. Hardware Block Diagram of the Developed Control Board

MVMS control board for the developed sorter in this study consists of main controller and double buffering, CAN interface block, LVDS sensor data interface block (de-serializer), USB3.0 interface engine block, and power block. Figure 7 shows hardware block diagram.

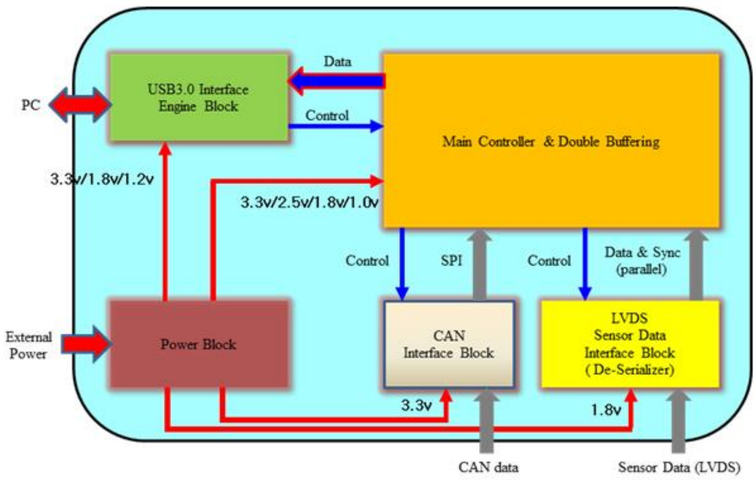

Figure 7. Hardware Block Diagram

2.3. Detailed Design and Dependence

2.3.1. LVDS De-Serializer

Video data coming in LVDS mode are converted into parallel data (Vsync, Hsync, Data0~7, Pclk) through de-serializer chip (DS90UB914) and sent to FPGA input pin. LVDS de-serializer signals of all the input/output pins except LVDS pins are controled by 1.8V IO Power. Mode should be selected in de-serializer (DS90UB914) according to the speed of coming LVDS data coming. Figure 8 shows the designed LVDS circuit diagram.

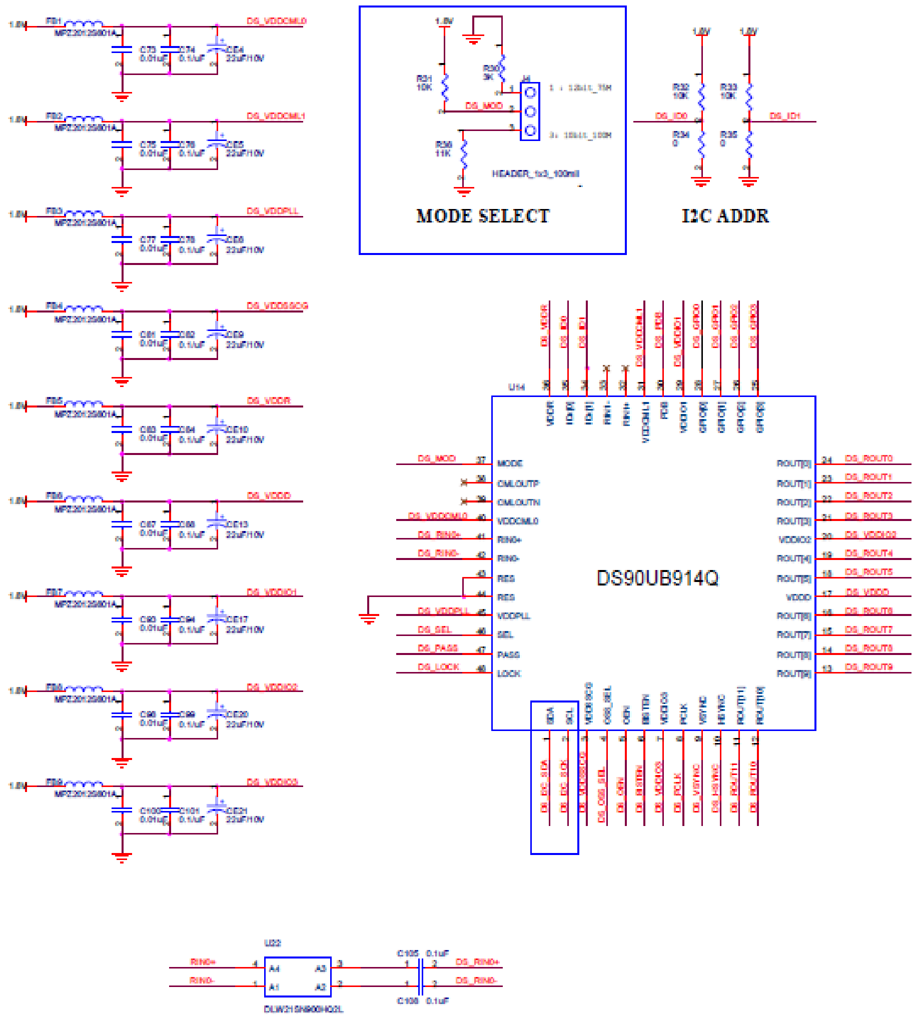

Figure 8. Designed LVDS Circuit Diagram

2.3.2. FPGA to USB

Video data coming in through LVDS input pins and dual CAN data from CAN input pins are combined into one video frame by FPGA. Those data are continuously transmitted to USB 3.0 interface of PC or a notebook through USB Controller (USB3014) chip in real time. USB Controller adopted for this study supports 5Gbps USB 3.0 PHY and 12C master controller up to 400KHz/10MHz and its host interface control and command support Data stream/12C/peripheral control mode and 32Bit data bus control.

Figure 9 shows USB controller input format in synchronous slave FIFO write mode.

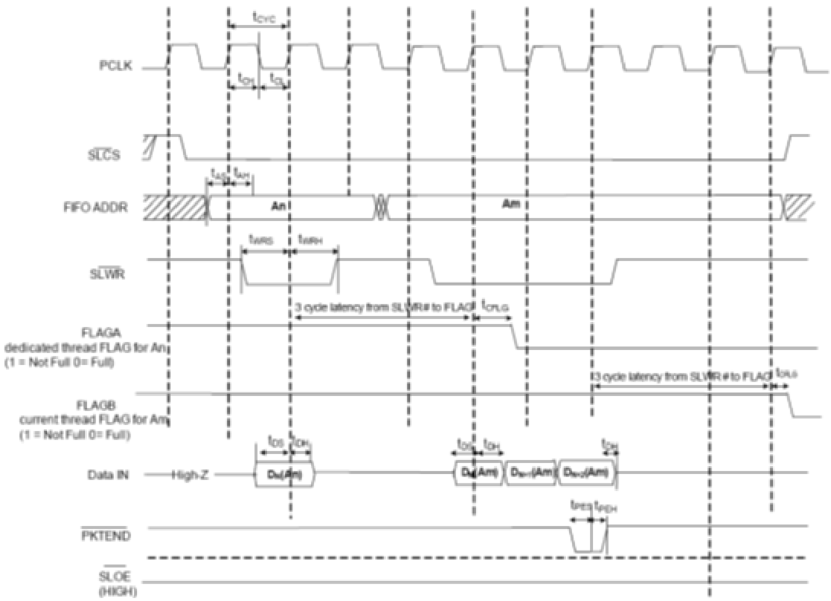

Figure 9. USB Controller Input Format

2.3.3. Top Module Using FPGA

In the top module, input data format has two paths of 'parallel' and 'LVDS de-serializer' and comprises uniformed data (Vsync, Hsync, Pclk, Data) through. CAN data that are converted to SPI are added to image data through CANController.v module. FrameCounter.v module adds count data to the beginning part of image data coming in real time and delivers them to Dram controller part. Dram controller consists of DramWrite.v module that inputs entered image data in Dram; DramRead.v module that outputs the data of Dram; and DrameInitial.v that initializes Dram. Image data that output from Dram are sent to CY3014 chip, which is USB controller, through SdReadCon.v module.

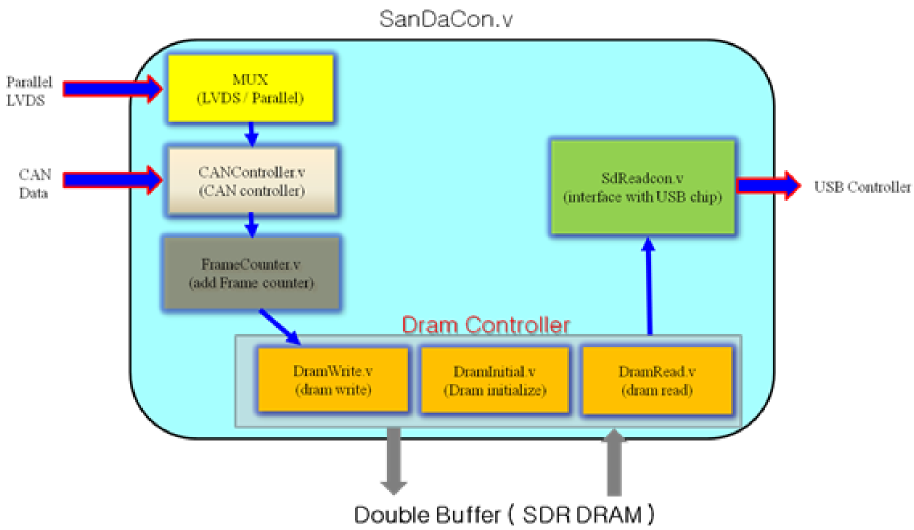

Figure 10. Top Module Structure

It synchronizes them to input RST signals and initializes two SDR Dram. Dram initialization proceeds in the order of Reset → PreCharge → Refresh → MRS Setting → EMR Setting → Active. Increasing their addresses of image data (Vsync, Hsync, Data, Pclk) in order, DramWrite module records them in SDR Dram. Ras-Cas latency is 3 and uses Bust 8 mode to record them in Dram. It is a module that increases data address stored in Dram according to Read pin High and reads and transmits them. When the data are transmitted, it helps valid data synchronize at the next phase by maintaining valid signals at high state. They are synchronized with input Enb signals, keeping ReadOut pin high; ReadOut signals are connected to read signals of DataRead.v module; and the data are read in Dram and transmitted to USB controller part. at this point, the data are put for each FiFo according to FifoAd[1:0] signal.

2.4. GUI Development and Signal Timing

For the sake of user's convenience, this study developed GUI that consists of ① Main view, ② ROI control, ③ S/W control, and ④ Camera condition control window as seen in Figure 11. ROI can be set and adjusted freely using a mouse after dragging it for changing position. When Set ROI button is clicked, it sets ROI to the defined setting.

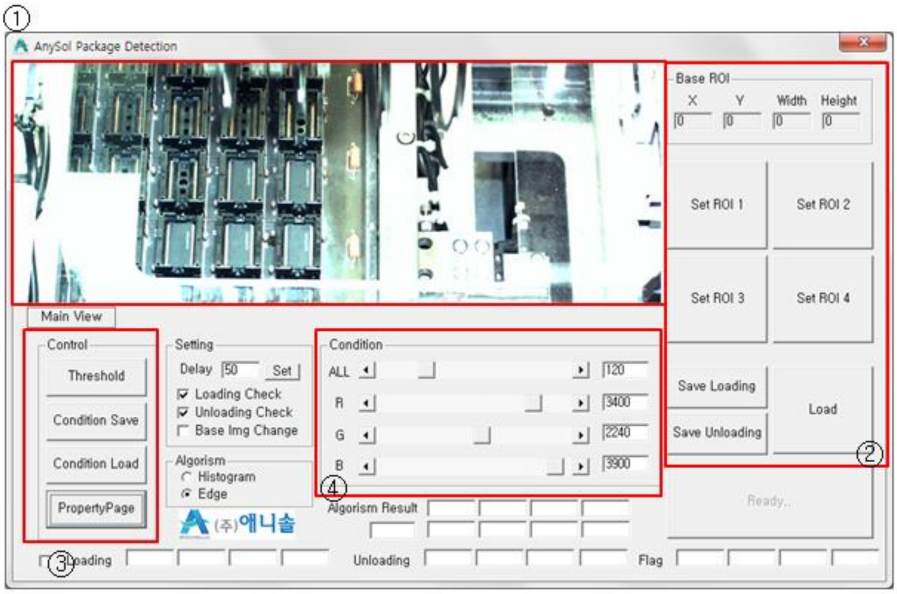

Figure 11. Graphic User Interface

In case that loading is applied by turning on Save Loading/Unloading with working equipment after setting ROI, pogo-pin image should be saved. As for unloading in this case, package image should be saved.

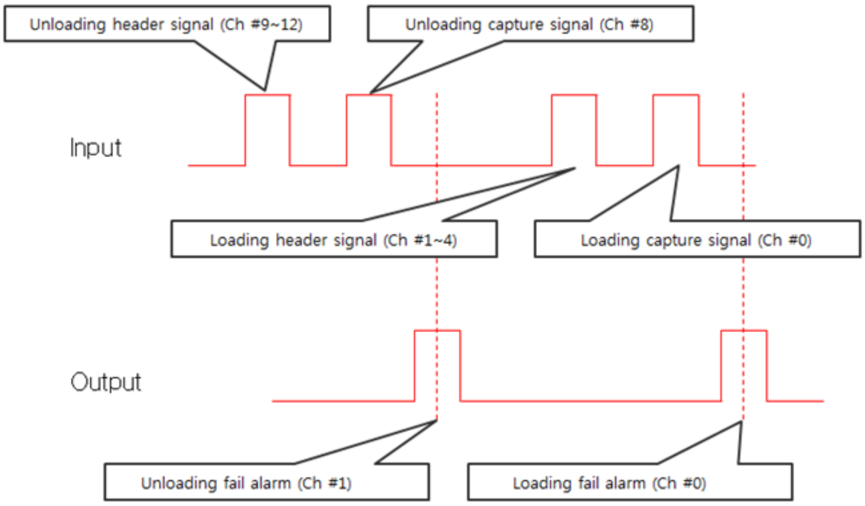

Figure 12. Signal Timing

3. Algorithm Verification and Hardware Performance Evaluation

When images are unloaded, edge is detected and its value is amplified. However, loading image barely has edge, so the resultant value is small even after amplification. Therefore, when the value of image unloading turns out smaller than threshold value, it is considered as "Fail", so is image loading when its value is greater than threshold value.

Figure 13. Unloading Image

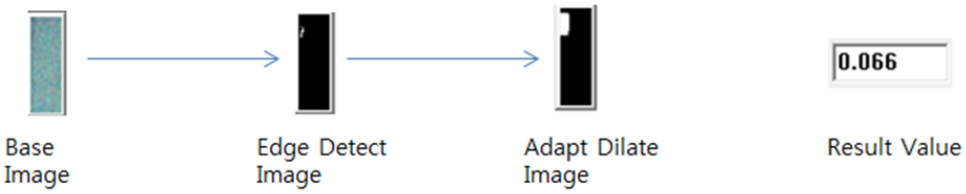

Figure 14. Loading Image

Consistent testing only with first-registered base images can't guarantee active response to ambient environment, which ever changes. Therefore, the base registration information and target information should be replaced often. After registering produced target information as base registration information in case of unloading (or loading) images, comparison is repeated between the replaced base registration information and target information for a sequence of loading (or loading). This is how to update base registration information.

Table 1. Performance Analysis

Specification	Unit	Values
1. Image gathering speed	ms	Max. 16ms
2. Exposure Time	ms	Max. 34.5ms
3. Calculate speed	ms	< 1ms
4. Alarm Response Delay	ms	Max. 32ms
5. Activity Pixel	HxV	1280x960
6. Interface speed	Bit/Sec	1GB/S
7. I/O scan time	Hz	10KHz
8. Lens FOV	mm	12mm

4. Conclusion

In this study, MVMS was developed by applying machine vision control algorithm specializing in sorter process and remote-monitoring technology for automated semiconductor package testing. Recognition for MVMS was advanced with color space developed through intelligent vision recognition algorithm and reliability was secured through histogram. In addition, the present study developed image sensor evaluation board to enable to notify a process engineer in remote distance of the status of high-speed sorter without delay and helps him to take a proper action such as prompt correction and readjustment of equipment. The developed system is expected to contribute to increasing the yield of semiconductor production process because its image gathering speed turned out to be 16[ms] and alarm response delay is 32[ms].

Acknowledgments

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