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SSTL IO Standard Based Low Power Arithmetic Design Using Calana Kalanabhyam On FPGA

Gaurav Verma[1], Sushant Shekhar[1], Kumar Shashi Kant[2], Vikas Verma[3], Himanshu Verma[4] and Bishwajeet Pandey[5]

[1,4]*Jaypee Institute of Information Technology Noida, India*
[2]*Symbiosis Institute of Technology, India*
Indian Institute of Technology, Roorkee
[5]*Gyancity Research Lab, India*
gaurav.iitkg@gmail.com, sushantshekhar09@gmail.com,
shashi.nitjsr26@gmail.com
vikasverma.iitr@rediffmail.com, himanshutechdn@gmail.com,
gyancity@gyancity.com

Abstract

Vedic mathematics consists of 16 formulas. Calanakalanabhyam is a Sanskrit word meaning "Sequential motion". Using this Vedic technique, we will find the roots of the equation in few seconds. We have tried to make an energy efficient Calanakalanabhyam Vedic formula based root finder with 4 inputs and 2 outputs. We have taken different SSTL Input/Output Standards and have done Study of Power by varying frequencies. SSTL Input/Output Standards used in this paper are SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. The code has been implemented on 28nm FPGA platform, XC7K160T device, FBG676 package and -3 speed grade. With our proposed technique, we have 41-60% achieved reduction in total consumption of power with frequency scaling.

Keywords*: Calanakalanabhyam, Vedic mathematics, FPGA, energy efficient, root finder*

1. Introduction

Vedic mathematics was rediscovered in the 20th century from Hindu scriptures (Vedas) that is dating back to 3000 BCE [1]. It has the fastest calculations methods based on 16 formulae [2]. These sutras is applicable in many branch of Mathematics in an efficient way [3].Vedic mathematics is basically used for solving tedious problems in short duration of time. Our ancient scholars used these sutras for doing calculation faster. Nowadays with the help of calculators and computers we are able to solve long and heavy calculations. Research on these sutras in various fields is going on and progress has been seen in DSP (Digital Signal Processing), filters and many more. Many papers have also been published using Vedic mathematics for different applications. Vedic mathematics also plays an important role in DSP (Digital Signal Processing). Reconfigurable FFT has been proposed using Vedic mathematics [4]. An introduction to a novel architecture using Vedic mathematics techniques for high speed multiplication [5]. 8-bit fixed point Vedic DSP processor core has also been studied [6]. Vedic mathematics is also used to design DSP processor based on Vedic Urdhava-Triyagbhayam multiplication sutra [7]. In this paper, we have designed a root finder using Vedic technique known as "Calanakalanabhyam". Calanakalanabhyam is a Sanskrit word which means 'Sequential motion'. Now also this formula is used to reduce the complexity of the equation or to reduce the execution time. In this paper we have tried to design a root finder using calanakalanabhyam Vedic technique. This root finder consists of 4 inputs. 1st three are the

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coefficients of the variable and the 4th one is clock. The three coefficients a, b and c are 4 bit inputs and result 1 and result 2 are also 4 bits outputs. Figure 1 represents the symbol of root finder using calanakalanabhyam.

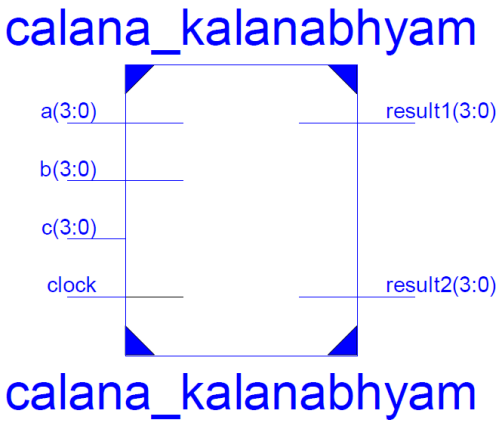

Figure 1. Symbol of Calanakalanabhyam

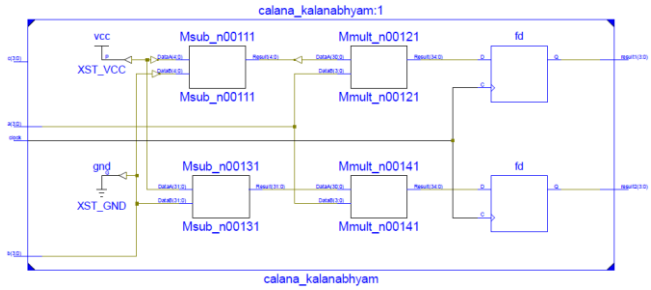

Figure 2. Schematic of Calanakalanabhyam

Figure 2 represents the schematic diagram of root finder using calanakalanabhyam. This Vedic technique can be explained by an example given below:

Example:

In order to find the quadratic roots of equation $7x^2 - 11x - 7 = 0$.
Swamiji called this sutra as calculus formula. Now by calculus formula we say:
$14x - 11 = \sqrt{317}$

In this research work, we have tried to make and energy efficient CalanaKalanabhyam Vedic root finder. We have taken different set of frequencies as mentioned in Table 2 and we have done Study of Power by varying frequencies and at different SSTL Input/Output Standards at fixed temperature *i.e.* is 25 degree Celsius. SSTL [8-11] family includes SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. Power has been calculated on these standards and analysis has been done to find the standard with least power consumption and to make an energy efficient [11-16] device. Table 1 shows different characteristics feature available in Kintex-7 FPGA.

Table 1. Different Features of Kintex-7 FPGA

I/O pins	676
Look Up Table	101400
Flip Flop	202800
IOBS	400
Giga bit transceiver	8
BRAM	325
Minimum operating temperature (OT)	273.15 K
Temperature Grade Letter	C

2. Study of Power

A. Study of Power for SSTL15 INPUT/OUTPUT STANDARD

Table 2. Study of Power for 6 Various Frequencies

FREQUENCY	POWER CONSUMED
1400Mega Hertz	0.257
1.2Giga Hertz	0.212
2100Mega Hertz	0.441
1700Mega Hertz	0.336
1800Mega Hertz	0.361
2.2Giga Hertz	0.467

There is 54.60% saving in total consumption of power with 1.2 Giga Hertz in compare to 2.2 Giga Hertz as visible in Figure 3 and Table 2.

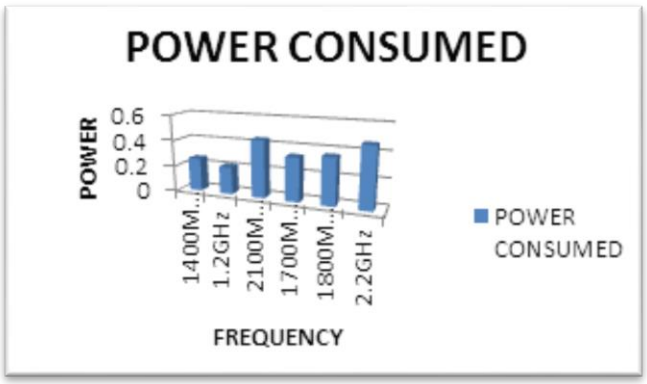

Figure 3. Study of Power for SSTL15 Input/Output Standard

B. Study of Power for SSTL18_II Input/Output Standard

Table 3. Study of Power for 6 Various Frequencies

FREQUENCY	POWER CONSUMED
1400Mega Hertz	0.440
1.2Giga Hertz	0.350
2100Mega Hertz	0.806
1700Mega Hertz	0.597
1800Mega Hertz	0.647
2.2Giga Hertz	0.858

There is 59.20% saving in total consumption of power with 1.2 Giga Hertz in compare to 2.2Giga Hertz as visible in Figure 4 and Table 3.

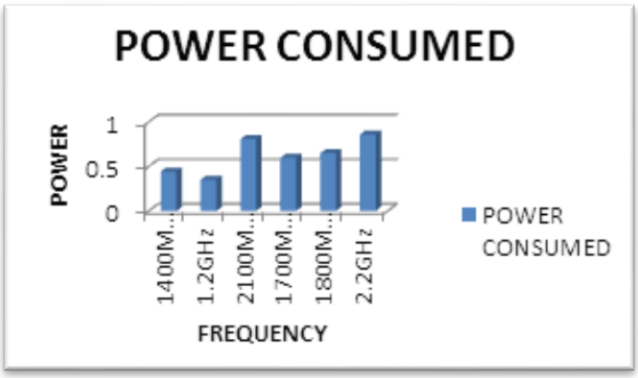

Figure 4. Study of Power For *SSTL18_II* Input/Output Standard

C. Study of Power for SSTL135 Input/Output Standard

Table 4. Study of Power for 6 Various Frequencies

FREQUENCY	POWER CONSUMED
1400Mega Hertz	0.251
1.2Giga Hertz	0.207
2100Mega Hertz	0.431
1700Mega Hertz	0.328
1800Mega Hertz	0.353
2.2Giga Hertz	0.457

There is 54.70% saving in total consumption of power with 1.2 Giga Hertz in compare to 2.2Giga Hertz as visible in Figure 5 and Table 4.

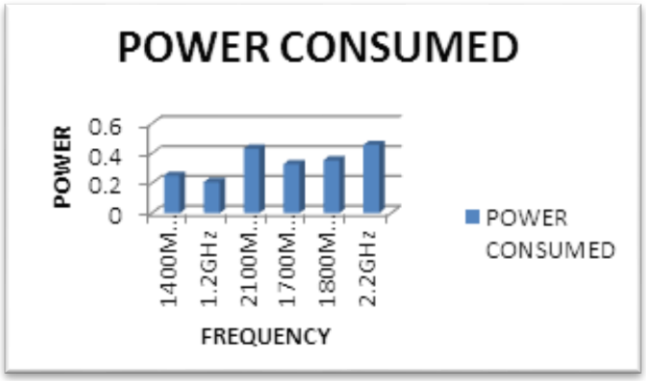

Figure 5. Consumption of Power for SSTL135 Input/Output Standard

D. Study of Power for SSTL12 INPUT/OUTPUT STANDARD

Table 5. Study of Power for 6 Various Frequencies

FREQUENCY	POWER CONSUMED
1400Mega Hertz	0.155
1.2Giga Hertz	0.138
2100Mega Hertz	0.225
1700Mega Hertz	0.185
1800Mega Hertz	0.195
2.2Giga Hertz	0.235

There is 41.27% saving in total consumption of power with 1.2 Giga Hertz in compare to 2.2Giga Hertz as visible in Figure 6 and Table 5.

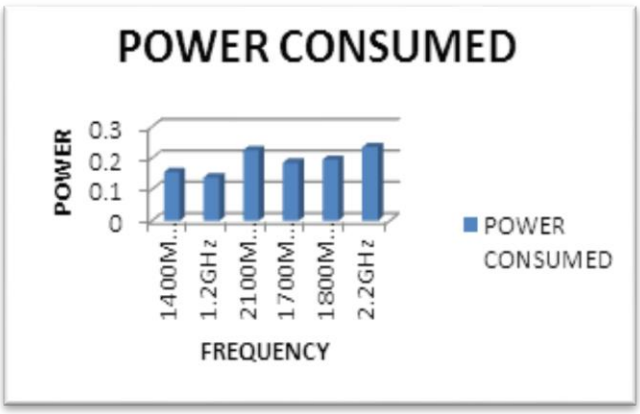

Figure 6. Study of Power for SSTL12 Input/Output Standard

E. Study of Power for SSTL18_I Input/Output Standard

Table 6. Study of Power for 6 Various Frequencies

FREQUENCY	POWER CONSUMED
1400Mega Hertz	0.378
1.2Giga Hertz	0.302
2100Mega Hertz	0.686
1700Mega Hertz	0.510
1800Mega Hertz	0.552
2.2Giga Hertz	0.730

There is 58.63% saving in total consumption of power with 1.2 Giga Hertz in compare to 2.2Giga Hertz as visible in Figure 7 and Table 6.

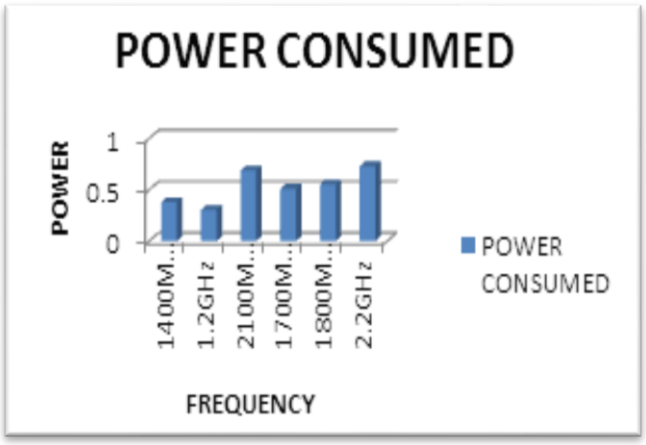

Figure 7. Study of Power for SSTL12 Input/Output Standard

F. Study of Power for different Input/Output Standard

Table 7. Study of Power for SSTL Family

INPUT/OUTPUT STANDARD	1400 Mega Hertz	1.2 Giga Hertz	2100 Mega Hertz	1700 Mega Hertz	1800 Mega Hertz	2.2 Giga Hertz
SSTL15	0.257	0.212	0.441	0.336	0.361	0.467
SSTL18_II	0.440	0.350	0.806	0.597	0.647	0.858
SSTL135	0.251	0.207	0.431	0.328	0.353	0.457
SSTL12	0.155	0.138	0.225	0.185	0.195	0.235
SSTL18_I	0.378	0.302	0.686	0.510	0.552	0.730

There is 64.77% saving in total consumption of power with SSTL12 in compare to SST18_II at 1400 Mega Hertz. There is 60.57% saving in total consumption of power with SSTL12 in compare to SST18_II at 1.2Giga Hertz. There is 72.08% saving in total consumption of power with SSTL12 in compare to SST18_II at 2100 Mega Hertz. There is 69.01% saving in total consumption of power with SSTL12 in compare to SST18_II at 1700 Mega Hertz. There is 69.86% saving in total consumption of power with SSTL12 in compare to SST18_II at 1800 Mega Hertz. There is 72.61% saving in total consumption of power with SSTL12 in compare to SST18_II at 2.2Giga Hertz. Comparison between different Input/Output Standards and frequencies visible in Figure 8 and Table 7.

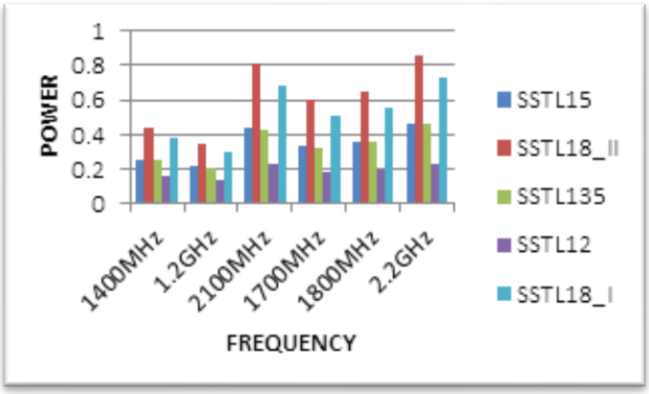

Figure 8. Study of Power for SSTL Family at Different Frequencies

3. Conclusion

The design is low power energy efficient and the code has been developed in Verilog HDL and results were implemented on Kintex-7 FPGA family. The device is designed to find the roots of an equation using the Vedic technique called Calanakalanabhyam. This Vedic root finder consists of 4 inputs and 2 outputs. 1 input is the clock pulse and other 2 inputs are the coefficients of the variables and remaining one is the constant of the equation. Output is the values of variables present in the equations. The inputs and the outputs all are 4 bit numbers. The design is tested by varying frequencies at different SSTL INPUT/OUTPUT STANDARDS at constant temperature that is 25 degree Celsius and also keeping air flow constant. There can be 41-60% saving of total consumption of power with frequency scaling too.

4. Future Scope

As we know that future is just anticipation based on our experience and repeated observation. In this work, we observe result with SSTL Input/Output Standards. We are curious about result with other Input/Output Standards like HSTL, LVCMOS, GTL, TTL, HSUL, MOBILE DDR and so forth. Here, we experience result based on 28nm FPGA then we are also waiting to observe result with 16nm and 20nm FPGA. Similar application of SSTL for solving mathematical problem other than finding root will also be challenge in our future research.

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