International Journal of Control and Automation
Vol. 9, No. 4 (2016), pp. 245-252
http://dx.doi.org/10.14257/ijca.2016.9.4.24

SSTL Input/Output Standard Based Energy Efficient Multiplier Design Using Urdhva Tiryagbhyam on 28nm FPGA

Md. Saifur Rahman[1], Md Mahbub E Noor[2], Tania Islam[2],
Rohit Tiwari[3], Kartik Kalia[4], Tanesh Kumar[5]

[1]*Noakhali Science and Technology University, Bangladesh*
[2]*Department of CSE, University of Barisal, Bangladesh*
[3]*National Institute of Technology, Srinagar, India*
[4]*Gyancity Research Lab, India*
5University of Oulu, Finland
iamsaif07@gmail.com, mahbub0601001@gmail.com,
tania.bd.09@gmail.com, rt220011@gmail.com

Abstract

We have taken different set of frequencies and done study of power by varying frequencies and with different SSTL Standard Used for Input/Outputs at fixed temperature i.e. 25 degree Celsius. SSTL family includes SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. Power has been calculated on these standards and analysis has been done to find the standard with least power consumption and to make an energy efficient device. The proposed multiplication algorithm is coded in Verilog, synthesized and simulated using Xilinx ISE design suit 14.2.at the end we can conclude that there can be 34-50% power consumption reduced by using frequency scaling technique and using SSTL Standard used for Input/Output. The maximum power has been consumed by SSTL18_II and minimum power consumption is by SSTL12.

Keywords*: Urdhva-Tiryagbhyam, Vedic Mathematics, FPGA, Energy Efficient, Multiplier*

1. Introduction

The Vedic Urdhva-Tiryakbhyam multiplier deliver faster performance than conventional multiplier [6]. Urdhva-tiryakbyham is used to implement vertical and cross wise operations [7]. It involves vertical and cross wise operations as illustrated in Example. Many research work has been done using Urdhva-Tiryakbhyam *e.g.* DSP operations using Vedic Urdhava-Triyagbhayam multiplication formula [10], 4*4 multiplier using Urdhva-Tiryakbhyam [11]. A multiplier that takes 8-bit complex number as input, processes it and gives the result has been designed and used Vedic mathematics for high speed performance [8]. Vedic mathematics has been used for designing a novel multiplier based on ROM approach [3]. A high speed low power circular convolutional has been implemented by using Urdhva-Tiryakbhyam multiplication algorithm [4]. Using Urdhva-Tiryakbhyam gives high speed processing. In this paper, we are designing a multiplier using Urdhvatiryagbhyam.

ISSN: 2005-4297 IJCA

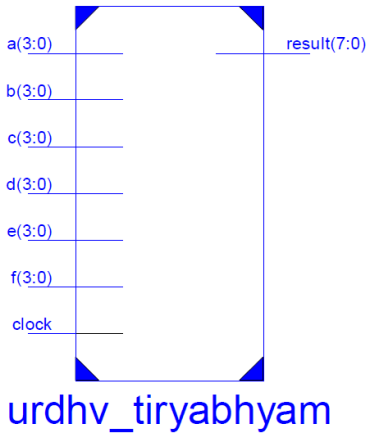


Figure 1. Symbol of UrdhvaTiryagbhyam

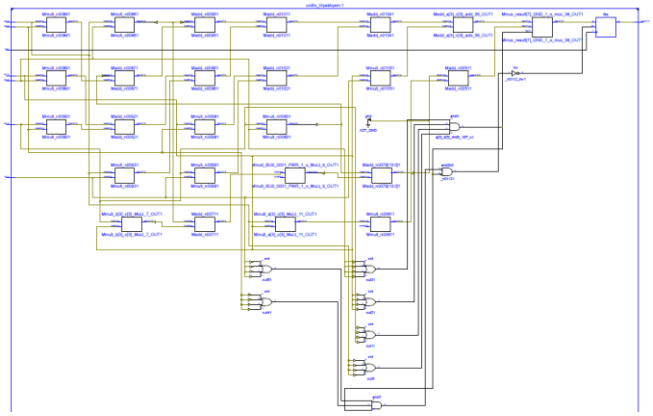


Figure 2. Schematic of UrdhvaTiryagbhyam

This design has been designed basically for multiplication and the technique UrdhvaTiryagbhyam can be well understood by using an example. The example below is multiplication of 2 digits number that's why inputs are a, b, c, d as visible in Table 2. But if, the multiplicands are 3 digits numbers e and f inputs will also be considered. as visible in Figure 1 there are seven inputs including the clock and the inputs a, b ,c ,d , e and f are 4 bits inputs and result (output) is 8 bits output as it is obtained by multiplication of 2 numbers. The schematic of the multiplier using UrdhvaTiryagbhyam is shown in Figure 2. The proposed multiplication algorithm is coded in Verilog, synthesized and simulated using Xilinx ISE 14.2. Table 1 shows different resource available in Kintex-7 FPGA.

Table 1. Different Option Available in Kintex-7 FPGA

IO pins	676
Operating Temperature Range	0-85 degree Celsius
Flip Flop	202800
DSP Block	600
Range of Operating Voltage	0.97-1.03V
Gb transceiver	8
BRAM	325
PCI Buses	1.1
MMCMS	8

Example: we are supposed to multiply 2 numbers that is 14 X 12.

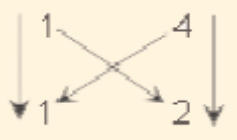
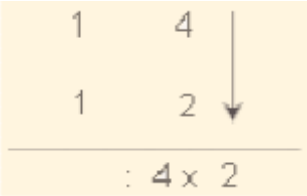


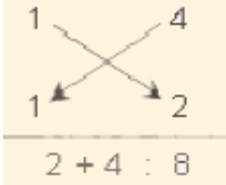
Table 2. Values of Multiplicands

a	b	c	d	e	f
1	4	1	2	-	-

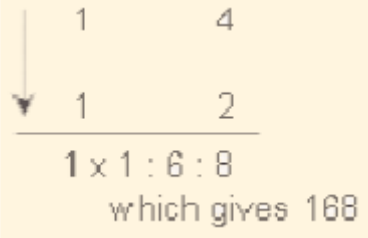
Step 1: The last digit of the multiplicand (14) *i.e.* 4 is multiplied by the last digit of the multiplier (12) *i.e.* 2. The product 4 X 2 = 8 forms last digit of the answer.



Step 2: Diagonally multiply last digit of multiplicand and 2nd digit of multiplier (answer 4 X 1=4); then multiply the 2nd digit of multiplicand and 1st digit of multiplier (1 x 2 = 2); add these two 4 + 2 = 6.



Step 3: Now, vertically multiply the second digit of the multiplicand and multiplier, *i.e.*, 1 X 1 = 1. It gives the first digit of the answer. Therefore, the answer is 168.



We have taken different set of frequencies as mentioned in Table 3 and we have done Study of power by varying frequencies and at different SSTL Standard Used for Input/Outputs at fixed temperature *i.e.* 25 degree Celsius. SSTL family includes SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. SSTL (Symmetrical Structure Transient Limiter) is widely used for suppressing capacitor switching transients [1]. Via SSTL technology, we achieve green computing with respect to low voltage impedance [2]. Power has been calculated on these standards and energy efficient analysis [9][12-19] has been done to find the standard with least power consumption and to make an energy efficient device.

Table 3. Operating Frequencies Taken In Consideration

Operating Frequency	Cellular Device
1400Million Hertz	Lumia 710
1.2Giga Hertz	Galaxy Core
2100Million Hertz	Apple IPhone6
1700Million Hertz	HTC/T
1800Million Hertz	Micromax
2.2Giga Hertz	Xperia

2. Power Analysis

A. Study of power for SSTL15 STANDARD USED FOR INPUT/OUTPUT

Table 4. Study of Power for SSTL15 STANDARD Used for Input/Output

FREQUENCY	POWER CONSUMED
1400Million Hertz	0.435
1.2Giga Hertz	0.361
2100Million Hertz	0.642
1700Million Hertz	0.526
1800Million Hertz	0.556
2.2Giga Hertz	0.670

There is 46.11% power consumption reduced when frequency is scale down from max to min as visible in Figure 3 and Table 7.

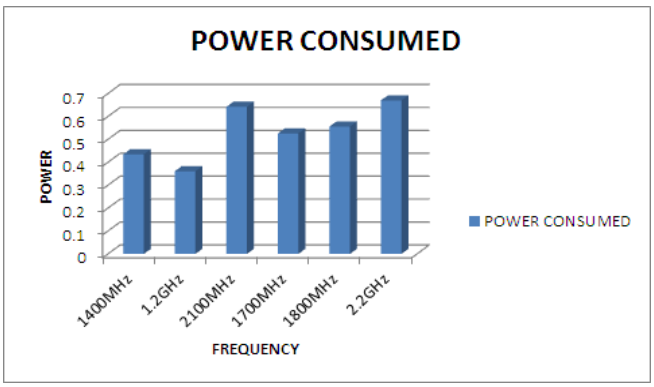


Figure 3. Study of Power for SSTL15 Standard Used for Input/Output

B. Study of power for SSTL18_II standard used for input/output

Table 5. Study of Power for *SSTL*18_II Standard Used for Input/Output

FREQUENCY	POWER CONSUMED
1400Million Hertz	0.706
1.2Giga Hertz	0.568
2100Million Hertz	1.089
1700Million Hertz	0.875
1800Million Hertz	0.930
2.2Giga Hertz	1.139

There is 50.13% power consumption reduced when frequency is scale down from max to min as visible in Figure 4 and Table 5.

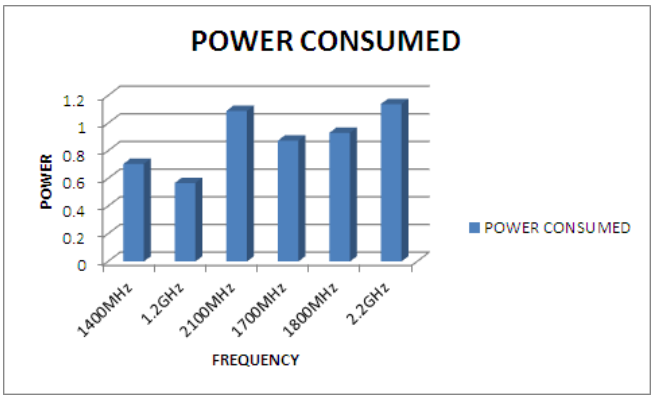


Figure 4. Study of Power For *SSTL18*_II Standard Used for Input/Output

C. Study of power for SSTL135 standard used for input/output

Table 6. Study of Power for *SSTL*135 Standard Used for Input/Output

FREQUENCY	POWER CONSUMED
1400Million Hertz	0.427
1.2Giga Hertz	0.355
2100Million Hertz	0.631
1700Million Hertz	0.517
1800Million Hertz	0.546
2.2Giga Hertz	0.658

There is 46.04% power consumption reduced when frequency is scale down from max to min as visible in Figure 5 and Table 6.

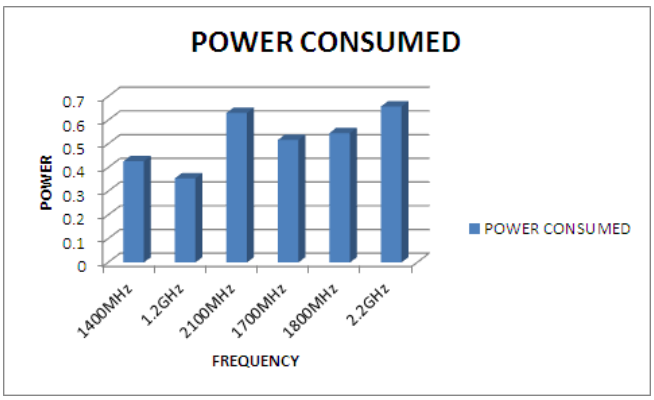


Figure 5. Power Dissipation for SSTL135 Standard Used for Input/Output

D. Study of power for SSTL12 standard used for input/output

Table 7. Study of Power for SSTL12 Standard Used for Input/Output

FREQUENCY	POWER CONSUMED
1400Million Hertz	0.313
1.2Giga Hertz	0.279
2100Million Hertz	0.415
1700Million Hertz	0.358
1800Million Hertz	0.373
2.2Giga Hertz	0.429

There is 34.96% power consumption reduced when frequency is scale down from max to min as visible in Figure 6 and Table 7.

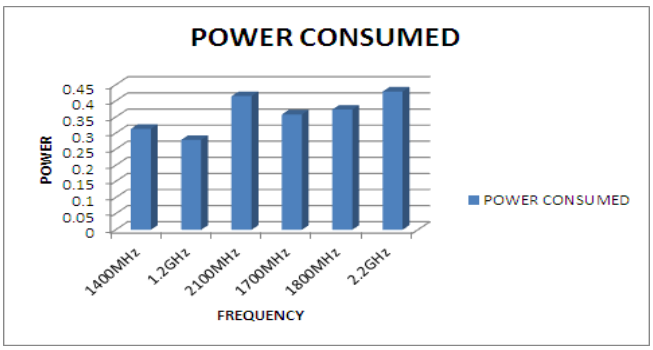


Figure 6. Study of Power for SSTL12 Standard Used for Input/Output

E. Study of Power for SSTL18_I Standard Used for Input/Output

Table 8. Study of Power for SSTL18_I Standard Used for Input/Output

FREQUENCY	POWER CONSUMED
1400Million Hertz	0.616
1.2Giga Hertz	0.498
2100Million Hertz	0.943
1700Million Hertz	0.761
1800Million Hertz	0.807
2.2Giga Hertz	0.989

There is 49.49% power consumption reduced when frequency is scale down from max to min as visible in Figure 7 and Table 8.

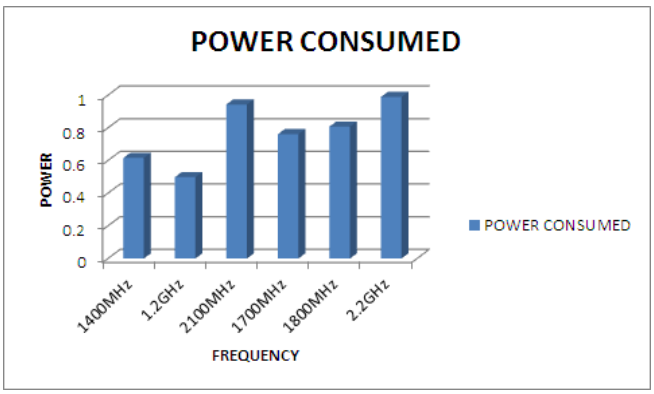


Figure 7. Study of Power for SSTL18_I Standard Used for Input/Output

F. Study of power for different standard used for input/OUTPUT with Various frequencies

Table 9. Study of Power for SSTL Family at Various Frequencies

STANDARD	1400MHz	1.2GHz	2100MHz	1700MHz	1800MHz	2.2GHz
SSTL15	0.455	0.361	0.642	0.526	0.556	0.670
SSTL18_II	0.706	0.568	1.089	0.875	0.930	1.139
SSTL135	0.427	0.355	0.631	0.517	0.546	0.658
SSTL12	0.313	0.279	0.415	0.358	0.373	0.429
SSTL18_I	0.616	0.498	0.943	0.761	0.807	0.989

From Figure 8 and Table 9 we can say that maximum power has been consumed by SSTL18_II and minimum power consumption is by SSTL12.

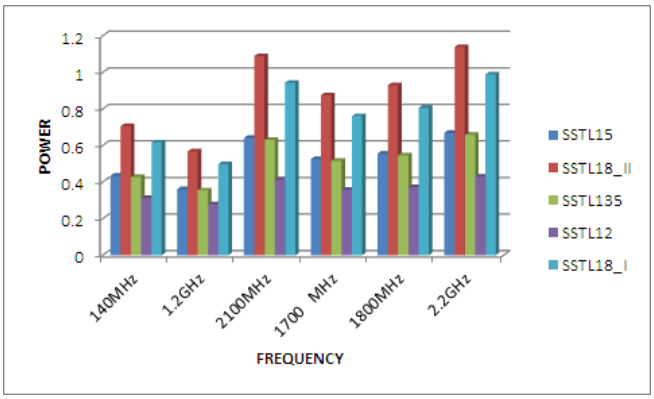


Figure 8. Study of Power for Sstlfamily at Various Frequencies

3. Conclusion

In this research work, we have tried to make an energy efficient Vedic multiplier using UrdhvaTiryagbhyam Vedic formula. Different set of frequencies and study of power by varying frequencies and different SSTL Standard Used For Input/Outputs at fixed temperature are taken uder consideratio. SSTL family includes SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. SSTL (Symmetrical Structure Transient Limiter) is widely used for suppressing capacitor switching transients. Power has been calculated on these standards and analysis has been done to find the standard with least power consumption and to make an energy efficient device. The proposed multiplication algorithm is coded in Verilog, synthesized and simulated using Xilinx ISE. The maximum power has been consumed by SSTL18_II and minimum power consumption is with SSTL12.

4. Future Scope

We have seen better result in present with SSTL input/output standards. In future, we can explore other variety of input/output standards mainly LVMCOS, PCI, HSTL, LVDCI, GTL, TTL. With current research in multiplier, options are available to explore other arithmetic circuits. Here our work is implemented on 28nm FPGA then future implementation will be on 3-D IC, and 16nm FPGA.

References

[1] T. Mahurkar, "Suppression of capacitor switching transients using Symmetrical Structure Transient Limiter [SSTL] and its applications." Intl Conf onComputation of Power, Energy, Information and Communication (ICCPEIC), IEEE, **(2014)**.
[2] T. Das, "Simulation of SSTL Standard Used For Input/Output based power optimized parallel integrator design on FPGA." Intl Conf onRobotics and Emerging Allied Technologies in Engineering (iCREATE), IEEE, **(2014)**.
[3] L. Sriraman, and T. N. Prabakar, "Design and implementation of two variable multiplier using KCM and Vedic mathematics." Intl Conf on Recent Advances in Information Technology (RAIT), IEEE, **(2012)**.
[4] J. Hazra, "An efficient design technique of circular convolution circuit using Vedic Mathematics and McCMOS technique." Intl Conf on Computer Communication and Informatics (ICCCI), IEEE, **(2012)**.
[5] A. Kumar, "Low power ALU design by ancient mathematics." Intl Conf onComputer and Automation Engineering (ICCAE), IEEE, vol. 5, **(2010)**.
[6] R. Gupta, "Design of high performance 16 bit multiplier using vedic multiplication algorithm with McCMOS technique." Intl Conf onGreen Computing Communication and Electrical Engineering (ICGCCEE), IEEE, **(2014)**.
[7] A. Bisoyi, "Comparison of a 32-bit Vedic multiplier with a conventional binary multiplier." Intl Conf onAdvanced Communication Control and Computing Technologies (ICACCCT), **(2014)**.
[8] B. S. Premananda, "Design of area and power efficient complex number multiplier." Intl Conf onComputing, Communication and Networking Technologies (ICCCNT), IEEE, **(2014)**.
[9] T. Kumar, "Mobile DDR IO Standard Based High Performance Energy Efficient Portable ALU Design on FPGA", Springer Wireless Personal Communications, An International Journal, vol. 76, Issue 3 **(2014)**, pp. 569-578.
[10] A. K. Itawadiya, "Design a DSP operations using vedic mathematics." IEEE Intl Conf onCommunications and Signal Processing (ICCSP), **(2013)**.
[11] D. K. Kundu, "Implementation of optimized high performance 4× 4 multiplier using ancient Vedic sutra in 45 nm technology." 2nd IEEE Intl Conf onDevices, Circuits and Systems (ICDCS), **(2014)**.
[12] B. Das, "Power Optimization of Semiconductor Laser Driver Using Voltage Scaling Techniques", ARPN Journal of Engineering and Applied Sciences, vol. 10, no.10, **(2015)** October.
[13] H. Kaur, "Processor Specific Data Processing Device (DPD) Design for Energy Efficient Data Center", International Journal of Energy, Information and Communications, vol.6, Issue 3 **(2015)**, pp. 29-38.
[14] A. Moudgil et.al.. "Low Voltage Complementary Metal Oxide Semiconductor Based Internet of Things Enable Energy Efficient RAM Design on 40nm and 65nm FPGA", International Journal of Smart Home, vol. 9, no. 9, **(2015)**, pp. 37-50.
[15] S. Madhok, "HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA", International Journal of Control and Automation (IJCA), vol. 8, no. 8, **(2015)**.
[16] S. Nagah, "I/O Standards Based on Green Communication Using Fibonacci Generator Design on FPGA", IJCA, vol. 8, no. 8, **(2015)**.
[17] T. Kumar, "CTHS Based Energy Efficient Thermal Aware Image ALU Design on FPGA", Springer Wireless Personal Communications, An International Journal, vol. 83, no. 1, (2015).
[18] D. Singh, "Thermal aware Internet of Things Enable Energy Efficient Encoder Design for security on FPGA", International Journal of Security and Its Applications, vol. 9, no. 6, **(2015)**, pp. 271-278.
[19] T. Kumar, "IoTs Enable Active Contour Modeling Based Energy Efficient and Thermal Aware Object Tracking on FPGA", Springer Wireless Personal Communications, vol. 85, no. (2), **(2015)**, pp. 529-543.

