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A Low Voltage Tunable Filter for Analog Baseband of Software Defined Radios

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Abstract

This paper presents a new low voltage tunable Low Pass (LP) filter for Software Defined Radios (SDR) wireless transceivers. The proposed LP filter attempts to optimize the performance of SDRs as it operates at relatively low voltage while providing wide tunable range at the same time. It is constructed using Gm-C technique employing three Operational Transconductance Amplifiers (OTA) and two grounding capacitors. The filter also exhibits independent electronic tuning of center frequency (fc) and quality factor (Q) providing more accuracy in its frequency response. Also its circuit can be synthesized to produce multiple other filter frequency responses by varying inputs which can be useful in other applications. The OTA is the main active element in the filter operating at input supply voltage of 1 V and providing open loop dc gain of 38 dB with power dissipation of 270 uW. The proposed LP filter is envisioned as a part of Zero-IF SDR architecture operating at a baseband section. Simulations are done in HSPICE using CMOS 0.18μm process parameters as functional verification of the presented theory.

***Keywords**: Software Defined Radio, Filter, Operatonal Transconductance Amplifier, Gm-C*

1. Introduction

As wireless and mobile technology is rapidly developing it can be expected that Fourth Generation (4G) mobile systems will be replaced by Fifth Generation (5G) mobile systems in few years or so. On the one hand, the existing tradeoffs among power consumption, performance and cost in a single handset will remain and circuit designers will continue to seek improvement on these aspects. On the other hand, the increasing use of wireless applications especially personal communication devices with different wireless standards has given additional challenge to create complex multi-mode transceiver which can process multiple wireless standards on the single hardware platform. Software Defined Radio (SDR) has emerged to address this issue which supports multi-standard reception by tuning to any carrier frequency and selection of any channel bandwidth. Its key performances are defined by software and the goal is to push the digital domain as near as possible to the antenna [1-4]. Different architectures of multi-standard receiver exists in the literatures and in practice. The zero-If receiver is the most preferable architecture from the view point of reconfigurable radios as it has the highest potential to reduce cost, size and power, even under flexibility constraints.

Filters, in any communication system pass the desired signals and reject the undesired signals with minimal distortion. Analog baseband filters play a crucial role in the design of wireless transceiver system since the performance of these filters directly affects various important parameters of the system. Especially, SDR needs programmable filters with wide tuning range since it deals with widely

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varying signal bandwidths. However, wide tuning range has to make tradeoffs with linearity and power consumption [5]. This paper proposes a LP filter tunable to a wide range while optimizing power consumption in the circuit at the same time. Also its cutoff frequency (f_c) and Quality (Q) factor can be tuned electronically without disturbing each other, thus providing more accurate frequency response. It employs three Operational Transconductance Amplifiers (OTA) as its active element and two grounded capacitors.

In analog integrated circuits Active RC and Gm-C are popular used techniques to construct filters. Both have their own merits and demerits while considering frequency response accuracy, linearity, and sensitivity, stability and power consumption [6]. The proposed LP filter is constructed using Gm-C technique since it is more favorable for low voltage and high frequency applications. Besides tunability and low power consumption, this circuit can also realize multifunction filter outputs by making alteration in input signal ports which can prove to be efficient in other applications. Chapter III presents the design of the low voltage tunable LP filter along with sensitivity analysis and non-ideal analysis. Chapter IV presents various simulations results done in HSPICE using Metal Oxide Semiconductor Implementation Service (MOSIS) 0.18 μm SPICE datasheet process parameters.

2. Software Defined Radios

As mentioned in the introduction part SDRs supports multiple wireless communication standards in a single hardware platform. A typical example might be a modern smart phone which supports GSM/WCDMA for voice communication, GPS for location and Bluetooth for short distance multimedia files transfer. All of these applications operate at different frequency bands and require their own communication standards. Table.1 shows different wireless communication standards existing today.

Table 1. Wireless Communication Standards

Standards	Frequency Bands (GHz)	Channel Bandwidth (MHz)
GSM	0.93 - 0.96	0.2
WCDMA	2.11 - 2.17	3.84
802.11a	5.25 - 5.35	20
WiMAX	2 - 11	1.25-28
GPS	1.575	-
Bluetooth	2.4 - 2.483,	1

There are several types of architectures for SDR transceivers which exist in practice and literature. Different architectures serve for different purposes so the selection of right architecture is also very important in the design of a SDR. A well designed transceiver architecture should utilize and share the programmable hardware resources like low noise amplifier (LNA), filters, analog to digital converters (ADC) and so on to bring the overall performance to the maximum. Selection of right architecture is also very important for the performance of overall communication system.

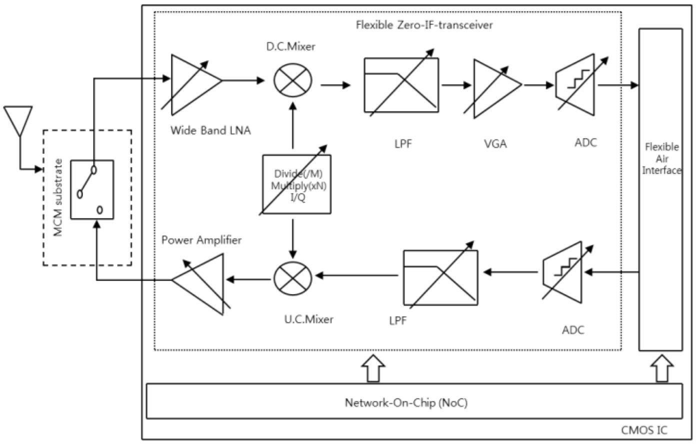


Figure 1. Block Diagram of the Zero-IF SDR Transceiver Implemented In IMEC

Fig.1 shows the Zero-IF SDR transceiver implemented in Interuniversity Electronics Centre (IMEC). It has high integration level with high multi-standard ability and dissipates low power which is highly favorable for SDRs [5].

3. Low Voltage Tunable Gm-C Filter

Wide range of filter topologies exist in practice and in literature. This paper uses Gm-C technique for constructing a tunable low pass filter as mentioned in the introduction part. The open loop in Gm-C topology ensures good performance in high frequency applications. Since high loop gain is not required the OTA bandwidth does not have to greatly exceed the filter cutoff frequency making it suitable for low power applications. Also since the use of grounded capacitors in Gm-C filter helps to reduce the parasitic capacitances in the circuit. The biggest drawback of Gm-C filters is poor linearity because of the nonlinear relationship between differential input voltage and output current in the transconductance.

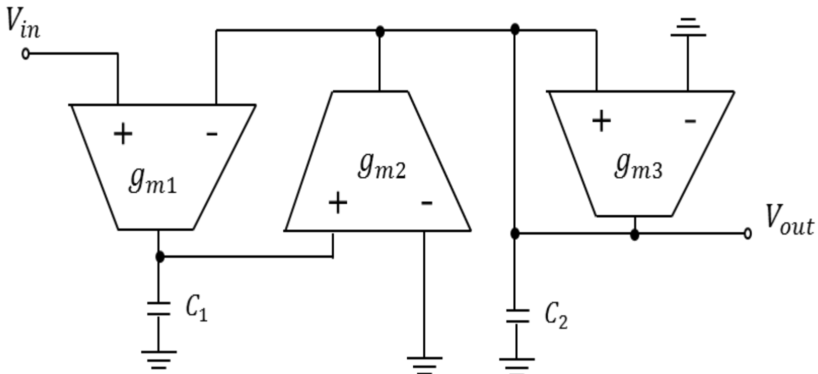


Figure 2. Proposed Low Pass Filter

Figure 2 shows the proposed LP filter for SDRs with wide tuning range and low power consumption. It employs three OTAs and two grounded capacitors. The transfer function of the LP filter can be derived as shown in the Equation (1).

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{S^2 + S\left(\frac{g_{m3}}{C_2}\right) + \frac{g_{m1}g_{m2}}{C_1C_2}} \qquad (1)$$

The angular frequency (ω_0) and Q factor of the filter can be derived as in equation (2).

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}},\ Q = \omega_o\frac{C_2}{g_{m3}} \qquad (2)$$

In equation (2) if g_{m3} is adjusted separately then controllable value for Q can be derived. This feature can improve the frequency response of a tunable filter since tuning cutoff frequency won't affect the Q factor and vice versa.

$$f_c = \frac{g_m}{2\pi\sqrt{C_1C_2}} \qquad (3)$$

Equation (3) represents the cutoff frequency by controllable value of g_m. Similarly, the sensitivity analysis of the LP filter can be derived as shown in the Table 2.

Table 2. Sensitivity of the Circuit Components

Parameters	$S_x^{\omega_o}$	S_x^Q
g_m	1	0
C_1	-1/2	0
C_2	-1/2	0

Here, Table.2 shows circuit sensitivity level of ω_0 and Q factor with respect to g_m and C_1 and C_2 values. The sensitivity level is quite low giving the reasonable approximation of the transfer function in the presence of component variations.

Filters use transconductance as their active element which are composed of transistors. Transistors do not react instantaneously to the applied voltage and there is some delay associated with it which create internal poles in the transconductances. This effect deviates filter from its ideal characteristics. Transfer function of a simple one pole system is shown in Equation (4).

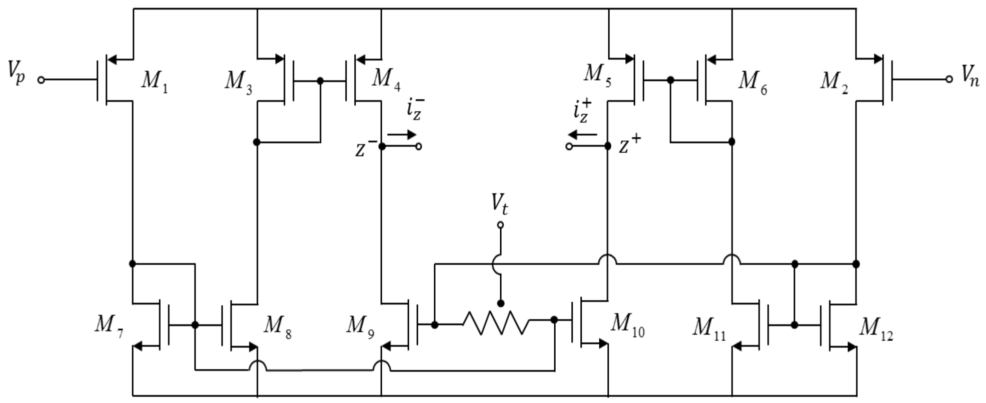
$$A(s) = \frac{g_m}{1 + \frac{S}{\omega_p}} \qquad (4)$$

Here, g_m is the transconductance DC gain and ω_p is the parasitic pole frequency. So in order to reduce these parasitic pole effect in the filter following criteria must be fulfilled as shown in Equation (5).

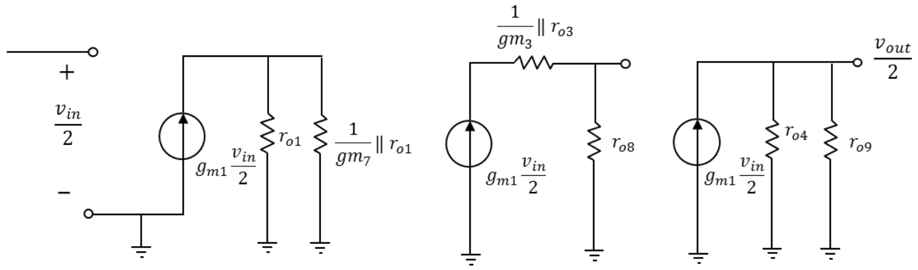
$$\omega_p \gg \omega_0 \qquad (5)$$

3.1. Low Voltage Operational Transconductance Amplifier

OTA circuits are extensively used in active filters design. An ideal OTA is a voltage controlled current source (VCCS). It uses it inverting and non-inverting voltage inputs to give current output with the externally controlled transconductance (g_m).



(a)



(b)

Figure 3. (A) CMOS Implementation of OTA (B) Small Signal Analysis of OTA

$$g_m = \sqrt{\mu C_{ox}(W/L) I_b} \tag{6}$$

$$A_v = -g_{m1}(ro_4 || ro_9) \tag{7}$$

$$f_{-3dB} = \frac{1}{2\pi\, r_{o1} C_L} \tag{8}$$

$$\omega_{0dB} = A_v \times f_{-3dB} \tag{9}$$

In Figure (a) assuming all MOS transistors operating in saturation regions, the value of g_m can be expressed as equation (5), where I_b is the current flowing in the each branch of the circuit, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W/L is the ratio of effective channel width and length of an individual MOS transistor. V_p and V_n are differential inputs which goes through M_1 an M_2 respectively. The circuit in Figure 4 (a) is perfectly symmetric and can be divided into two equal circuits. Figure 4 (b) represents the small signal analysis of one half of the circuit where small signal gain (A_v), pole frequency (f_{-3dB}) and gain bandwidth (ω_{0dB}) of the amplifier can be estimated as shown in equation (6-9).

Table 3 Comparison with Existing Gm-C Filters

References	Supply Voltage	Electronic Tuning (f_c and Q)
[7]	3	No
[8]	1.25	No
[9]	1.8	No
[10]	4	Yes
Proposed	1	Yes

Here in Table.4 reference [2], [7] and [9] has constructed Gm-C filter with 3 V, 1.25 V and 1.8 V of power supply without independent tuning of f_c and Q. Reference [10] has independent tuning of f_c and Q but the used supply voltage of 4 V. The proposed filter has just 1 V of power supply while supporting independent electronic tuning of f_c and Q.

4. Simulations and Results

The proposed second order low pass filter is simulated in HSPICE. Currents were biased in the MOS transistors to give g_m = 125 µS and capacitors C_1 and C_2 were assigned with the value of 25 pF.

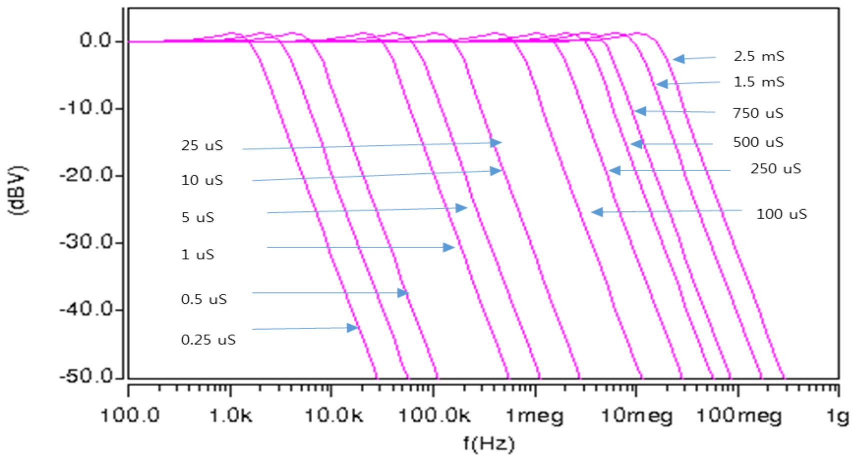


Figure 4. Frequency Tuning of the Proposed LP Filter

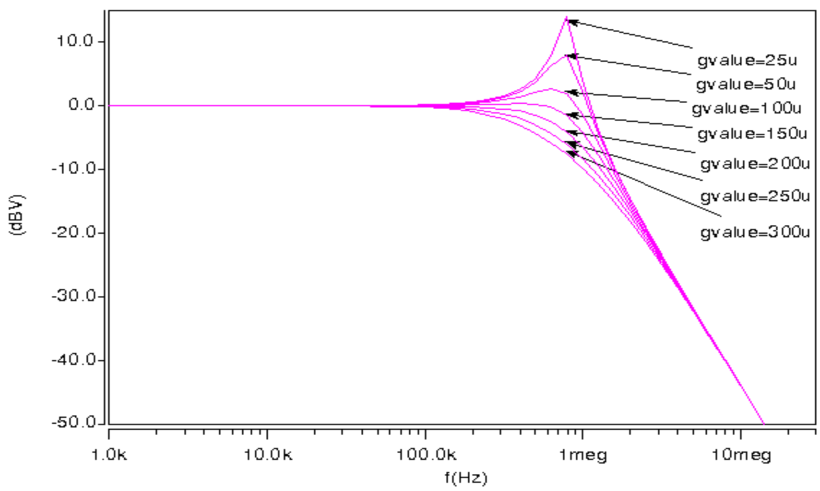


Figure 5. Q Factor Tuning of the Proposed LP Filter

Figure 4 shows the tuning of f_c from 5 KHz to 20 MHz when g_m values from were changed from 0.25 uS to 2.5 mS. . Figure 5 shows tuning of Q factor of the LP filter from 2 to 0.707 when g_m values were changed from 50 uS to 300 uS.

All the g_m values were adjusted by changing the aspect ratio (W/L) of transistor M_1, M_2, M_4 and M_5 from 5 to 400. The simulation data is arranged and shown in Table 4.

Table 4. Frequency Tuning With Aspect Ratio

Parameters	AspectRatio (W/L)	Cutoff Frequency (f_c)
M_1, M_2, M_4 and M_5	160	6 MHz
M_1 and M_2	300	12 MHz
M_4 and M_5	300	9 MHz
M_1, M_2, M_4 and M_5	300	16 MHz
M_1, M_2, M_4 and M_5	400	20 MHz
M_1 and M_2	16	650 KHz
M_4 and M_5	16	300 KHz
M_1, M_2, M_4 and M_5	16	200 KHz
M_1, M_2, M_4 and M_5	5	5 KHz

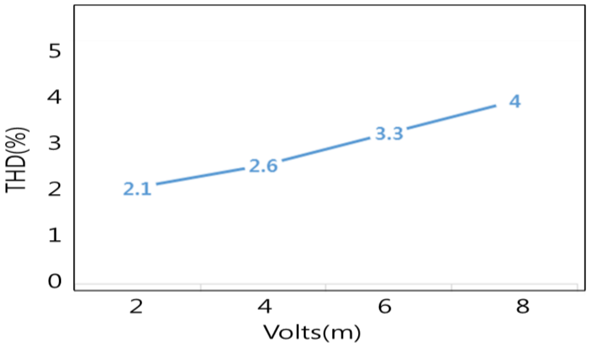


Figure 6. Total Harmonic Distortion (THD) of the Proposed LP Filter

Figure 6 shows the THD (%) of the designed LP filter. As seen in the figure THD rises from 2.1% to 4% when input amplitude of 5 MHz Sine wave increases from 2 mV to 8 mV. THD is calculated as

$$\mathrm{THD}(\%) = \frac{100\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}}{V_t}$$

where, V_n^2 is RMS voltage of n harmonics and V_t is total RMS output voltage.

5. Conclusion

A low voltage low pass filter with wide tuning capability was proposed for Software Defined Radios (SDR) transceiver systems. The filter was designed using Gm-C technique and it main advantage is its internal circuitry which helps balancing the tradeoff between power consumption and tuning range. Operatonal Transconductance Amplifier (OTA) was used as an active element for the filter which could operate on 1 V of DC power supply. Also as extra features, the circuit provided electronically tuning capability of cutoff frequency and quality factor of the filter giving more accuracy in its frequency response. In addition to that band pass filter response could also be realized by altering inputs. The sensitivity analysis also showed quite low sensitivity of various circuit components to the network. It is therefore expected that the use of this architecture might optimize the power consumption in the transceiver systems of SDRs.

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