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The Dynamic Pattern Test Method for ASIC's Fault Detection

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Abstract

The ASIC for control of the digital signal is progressing in the development of the avionics of the aircraft. In addition, the proportion used the ASIC in the industries is increasing continuously. However, it occurs the difficult problems of the maintenance of ASIC fault due to the maintenance company's bankrupt, equipment's aging, test equipment exchange and test requirement document's absence in the case of avionics systems. Therefor it will be expensive repair costs. To solve these problems, we proposed the method to testing the analog board with ASIC and without the TRD. In this paper, we proposed the Dynamic Pattern test method which created the TRD based on analyzed logic data extracted from ASIC and diagnosed on the ASIC circuits at the point of level of gate. We could identify the 17 pattern from tests, and figure out faults in 16 addresses. According to the experiment for target board applied with proposed methods, it is possible to diagnose fault for abnormal computerized chip, ASIC, by utilizing test unit board. We've also obtained the excellent performance for fault detection.

Keywords*: TRD (Test Request Document), Dynamic Pattern Test, ATE (Automatic Test Equipment), Fault Detection, ASIC(Application Specific Integrated Circuit)*

1. Introduction

In accordance with the development of an integrated semiconductor, the ASIC (Application Specific Integrated Circuit) has rapidly developed the level of the integration in the semiconductor on the digital system of the aircraft's avionics equipment. Because the trend to use ASIC is shrink in size and provide higher function densities and faster working speeds, while consuming less power and taking less area and weigh on the boards, ASICs increase in its usage in the field of electronic industries such as communication, automotive, consumer electronics, computers and avionics[1]-[4].

An ASIC is developed with customized logic that is specific application. ASIC manufacturer is designed to unable to modify the chip software for protected of IP (intellectual property). Particularly, it occurs the difficult problems of the maintenance of ASIC fault due to the maintenance company's bankrupt, equipment's aging, test equipment exchange(from analog system to digital system) and test requirement document's absence in the case of avionics systems. Therefor it will be expensive repair costs. To solve these problems, we proposed the method to testing the analog board with ASIC and without the TRD.

The faults of ASIC in the circuit board, it is possible for the traditional method of BIST (Built In Self Test) technology which applies the test pattern and compares the response signals with the predicted value from the outside of the chip may be designed in the circuit and prevent the faults [2][3], however, lots of costs are required at the development phase. Although the ASIC without BIST may be able to diagnose the failure using

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LASAR (Logic Automated Stimulus and Response) program, it takes a lot of cost and time in the development process. In addition, it impossible to develop the test method without the Test Requirement Document (TRD).

To shorten the period of the system development, the requirement for the development of ASIC continues to increase, and accordingly, the automation technique to facilitate the test is being introduced. From the user's aspect, the test may be performed of the system test through the failure diagnosis at the level of the system or sub-system using the Automatic Test Equipment (ATE)[4][5].

In this paper, it is proposed the test method of the ASIC, without the TRD, extracting the internal logic circuit and analyzed the function of the ASIC using the multipurpose development program and simulation. In addition, using a general Dynamic Pattern Test method, it intends to suggest the approaching method of the failure diagnosis on the circuit which is not provided by the TRD. To recreate the TRD, it performs the logic simulation through the internal logic extraction of ASIC and VHDL, and based on the rewritten test requisition, manufactures the Dynamic Pattern signals and ITA (Interface Test Adapter) which is a hardware interface. Mounting the circuit board of the test target on ITA and applying Dynamic Pattern signal, and then controlling the input signals in the in/output pin at the ASIC gate level, the fault extraction in the failure ASIC based on the output signal. As a result of the experiment, applying the suggested technique to the non-memory circuit, the excellent fault extraction capability was confirmed.

2. Conventional Fault Detection Method

In general, test methods for ASIC are both hardware based BIST (Built-in Self-Test) and software based LASAR (Logic Automatic Stimulus and Response). The BIST method is a form of self-test which is built into integrated circuits allowing self-test algorithms to examine their own operation, as opposed to reliance on external automated test equipment [5]. And LASAR method utilized as standardized test program to defense industries in the United States is a technique for detecting defects which fault dictionary generated a database of fault model at the test unit board [6],[7]. If it wants to the best performance of result from test methods. Both BIST and LASAR methods must have the test requirement information for ASIC. However, if there is not test requirement information in test target board, it is difficult to detect faults of ASIC.

2.1. Typical ASIC Test

Both ASIC and ordinary semiconductor devices may be produced with imperfect function in their production processes. ASIC test method is the design technique for the usage of the test at the development phase and the design method to ease the test at the production phase for the verification of hardware and the method to develop the algorithm which enables to generate the pattern for the test automatically in order to overcome DFT (Design for Testability) which can test using ATE (automatic test equipment) and high hardware design costs and relatively low failure extraction rate. It can be tested by using ATPG (Automatic Test Pattern Generation) technique [2].

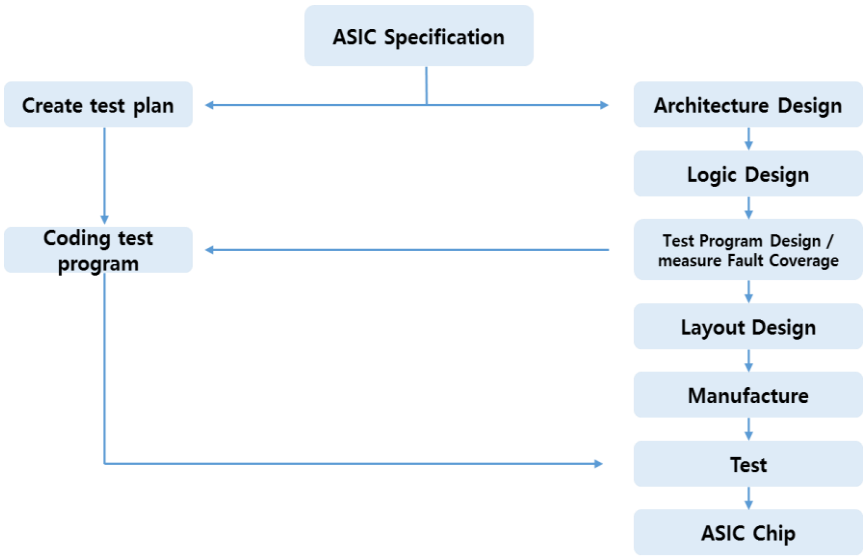


Figure 1. ASIC Test Process

Figure 1 illustrates the step of the test in ASIC manufacturing process. In the manufacturing process of ASIC, the plan for the test as well as the structure design shall be simultaneously created, and the detailed test program will be created and the fault coverage will be measure while designing the logic and in accordance with its result, all the procedures related to the test such as the test pattern and program creation *etc*. can be effectively completed and the reliability of ASIC can also be enhanced.

2.2. BIST (Built in Self-Test)

BIST (Built in Self-Test) is the method to mount the TPG (Test Pattern Generation) and TDE (Test Data Evaluation) in the same chip for self-test, to which Boundary Scan technique based on JTAG (Joint Test Action Group) belongs. Generally, ASIC test can be divided into three steps, and it applies the test pattern into the chip and compares the predicted output value and actual output value to extract faults. Herein, if the value different from the predicted value is output, it is regarded that the chip contains the physical fault and is determined as fault. [12]

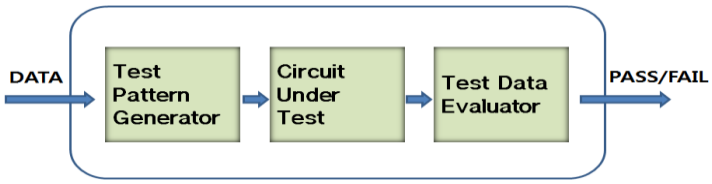


Figure 2. BIST Test Process

As seen in the Figure 2, the structure of BIST is composed of three step processors, running the pattern generator for the test and applying it to the circuit that intends to test and comparing the output data with the predicted value to determine if it is pass/fail. As BIST method is developed and led by the developer at the development step; it is general to use the fault extraction in the manufacturing line for mass production. Since its application to the operation process shall be applied by designing a separate circuit to the system, it has a disadvantage requiring additional development costs.

2.3. LASAR

LASAR is the standard of the defense industry in the United States for the development of the digital test program set. Different from the design simulator, when a test engineer is focusing on the problem encountering and there is a physical or logical error, LASAR predicts the timing variation of the test target signals and establishes the database for accurate diagnosis on the fault isolation and simplifies TPS development [7].

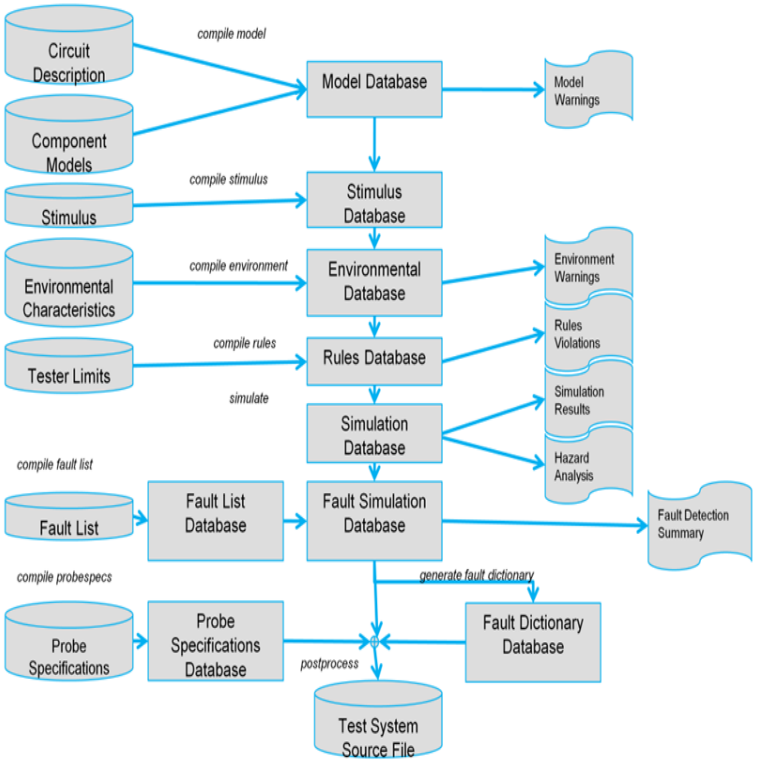


Figure 3. LASAR Test Process

As shown in Figure 5, LASAR is the program to generate the model database targeting the test object circuit through generation, pattern application, and the fault dictionary through simulation in accordance with the circuit composition, and develop the files possible for the physical function test to the test target units. In other words, it can entirely realize the circuits of the test target units to calculate the fault coverage, however, it necessarily requires the data about the component of test target units and such data shall be a database for simulation through modeling. Because, if any single process is omitted from the entire processes, the fault diagnosis procedure cannot be composed, the application is impossible without ASIC data which this paper intends to test and the long development lead time is required, depending upon the workmanship of the developer. In addition, it has another disadvantage that it is expensive for ordinary developers to use.

2.4. Dynamic Pattern Test

Dynamic Pattern Test purports to use for the test program development as well as to verify if it has the function equivalent with the ASIC test requisition for the test objects. Conventional test methods are to analyze the internal logic data of ASIC that we want to test in advance and to use the simulation data, or to perform the test applying the standardized protocol for the test, however, Dynamic Pattern Test is to diversely input the pattern signals into the input pins of test target ASIC and to control the clock signals and

to identify the output signals of the test target units and to diagnose if there is a fault in ASIC. If you have the in/output data for ASIC in the process of the fault diagnosis, you may improve the fault coverage [1].

Pattern is the input signal to apply the stimulus signal to the test objects and to check what kinds of responses the test objects output during the designated time intervals or which channel it reacts. A series of patterns in Dynamic Testing will be stored in the pattern memory section in RAM, and control the dedicated hardware and may accurately control the signal timing generated in the digital channel card by providing the signals to the test objects through the pattern controller, and prevent the distortion phenomena occurring in the process transmitting the signals in high speed. Such feature has advantages to preciously obtain the input and output patterns. In this regard, Dynamic Pattern Test technique may be able to apply various Dynamic Pattern signals to the test objects and to control the input signals of the ASIC in/output pins and to compare the reference output signals with the actual output signals and to extract the fault of failure ASIC.

3. Dynamic Pattern Test Method for Fault Detection

3.1. System Concept

In case of unknown TRD for the test unit board exists, it is impossible to take the fault diagnosis. It requires the TRD to analyze the confidence of fault detection on test unit board. Therefore, it makes the TRD based on the analyzed logic data of the ASIC, and diagnoses of the ASIC circuit at the gate level through the signal control of I/O pins using the Dynamic Pattern Test[1] [7], [8].

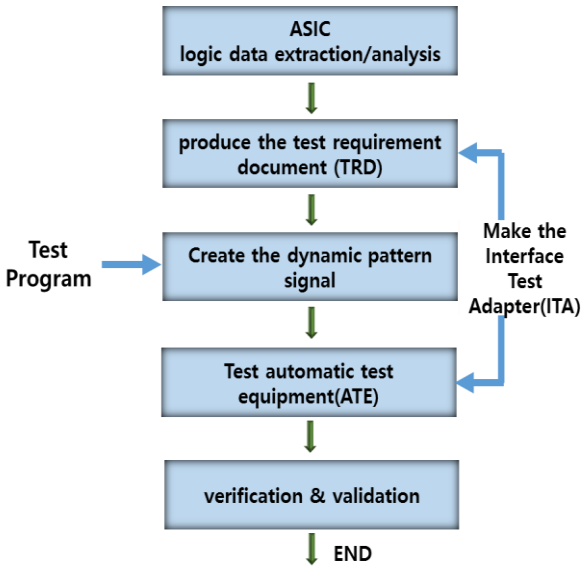


Figure 4. Dynamic Pattern Test Process

Reviewing the procedures to be processed on each step as shown in Figure 4, firstly at the logic data extraction and analysis step, data of the test target units will be analyzed. Secondly for the development of the TRD, it is necessary for analyzing the test unit board primarily. As the approach method for the failure diagnosis on the circuit which is not provided with the TRD using Dynamic Pattern Test technique [6-7], the logic simulation using the internal logic extraction of ASIC and the logic simulation using VHDL will be implemented, and based on the generated TRD, Dynamic Pattern Signals and ITA

(Interface Test Adapter) which is the hardware adapter will be produced. Mounting the test target circuit board in ITA, the fault diagnosis will be carried out. At the TRD production step, these shall be classified each signal name and input data and comparable output data and Dynamic Pattern signals will be created by those signals. At the final verification and validation step, after installing the test target units in ATE, fault will be diagnosed by realizing the function of circuit board mounted with ASIC by running the test program.

3.2. ASIC Logic Data Extraction and Analysis

There is methodology on processing for ASIC Logic data extraction and analysis steps as shown in Figure 5. This step extracts JEDEC files through the ROM writer from ASIC and converts into the logic equation text file utilizing JEDEC TO LOGIC EQUATION program. The text file can be redesigned from an equation text file into an OR-CAD EDA tool, which is circuit design program. We are able to simulate the redesign logic, analyze outcome from in/output and power/ground port and generate TRD with dynamic pattern test signals.

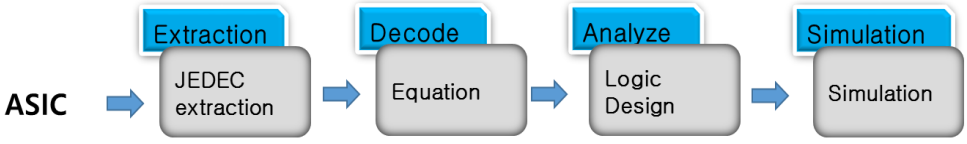


Figure 5. ASIC Logic Data Extraction and Analysis

3.3. Test Requirement Document (TRD) Production

Data logic analysis and the simulation results will be obtained for the output data for compared to the input data signal and the performance of the signal name of test target units. This value is used as a reference to create the Dynamic Pattern signal, and also utilized as the evaluation item of the TRD.

Therefore, TRD will contain the signal names, pin names, instrument channel number, the information defined by the pattern signal and the reference value to determining the normal and non-normal test for the peripheral device failure detection circuit, based on the analysis of the test target units[10]. As the TRD is developed for the purpose of operational maintenance of the test target units, this paper will apply the below variables and utilize the test requirement items in order to extract the faults.

1) Test requirement items for controlling ASIC (Table 1.)
- Classification of in/output of the test target units
- Signal name of the test target units
- Pin number
- Number and value of channel card

2) Test requirement items for controlling channel card data(Table 2.)
- Classification of in/output of the test target units
- Signal name of the test target units
- Address and data by signal

Table 1. Test Requirement Items for the ASIC

Seq.	Test Target Unit			Setup	
	I/O	Signal Name	Pin No.	DTI CH ID	Value
1	Input	MEMREQ	P1-507	192	H
2	Input	ISYSCRASH	P1-405	134	H->L
3	Input	DMAAD_16	P1-437	165	L
4	Input	DMAAD_15	P1-438	166	L

Table 2. Test Requirement Items for the Channel Card Data

NO	Test Target Unit		Set up Value	
	I/O	Signal Type	Address	Data
1	Input	SRAM_WRITE_B	0x0000	0x0000
2	Input	SRAM_WRITE_B	0x0001	0x0101
3	Input	SRAM_WRITE_B	0x0002	0x0202
…		omitted		
18	Output	SRAM_READ_B	0x0000	0x0000
19	Output	SRAM_READ_B	0x0001	0x0101
20	Output	SRAM_READ_B	0x0002	0x0202
.		omitted		

As shown in Table 1 and 2, we could identify that there was no problem in data transmission in case of normal condition. We obtained the 17 data set of Dynamic Pattern signals. As the results for comparison of 17 data by each address, we could figure that faults exist in 16 addresses

3.4. ITA (Interface Test Adapter)

Next, after the analysis of I/O signals required for the test requirement items is complete. We make the ITA. As shown in Figure 6, ITA is the device electrically interconnected with the test target unit in the middle to make it tested possible in ATE (Automatic Test Equipment)[1].

The ICA (Interface Connector Assembly) attached to the ATE is directly connected with the channel card M9 in the ATE. It can be achieved by implementing simultaneously or separately the input channel and output channel [10]. In this paper, we implement the design by separating the input pin and the output pin for ease of testing.

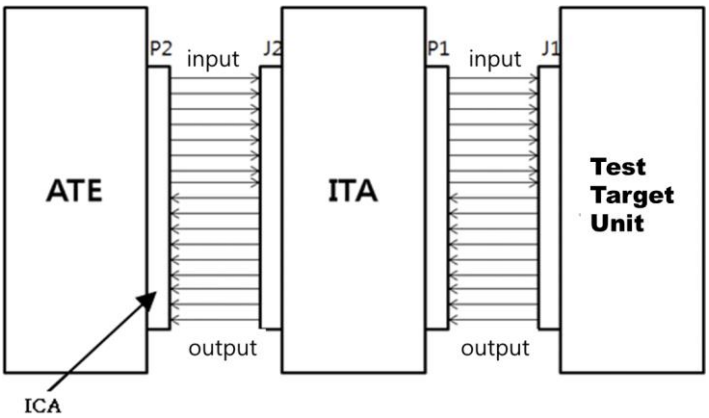


Figure 6. ITA System Concept

3.5. Dynamic Pattern Signal Implementation

The ASIC of a test target unit is inputted to the Dynamic Pattern signals, and this signal data analyzes the output signal according to a channel card allocated to each input signal. In this paper, a Dynamic Pattern Signal was implemented using the M9 Series DTI Soft Front Panel program developed by Teradyne Corporation.

Look at the operation step according to Dynamic Pattern signals, as shown in Figure 7, ISYSCRASH signal (Table 1) of ATE will send the ISYSCRASH signal of the test target unit to ITA. As the ISYSCRASH signal is converted from HIGH pulse to LOW pulse, the signal is changed from signal ready state(ready) to activation state(active) in ASIC, At the moment, memory data of the test target objects will be outputted as shown in Table 2 in accordance with the signals of ISYSCRASH.

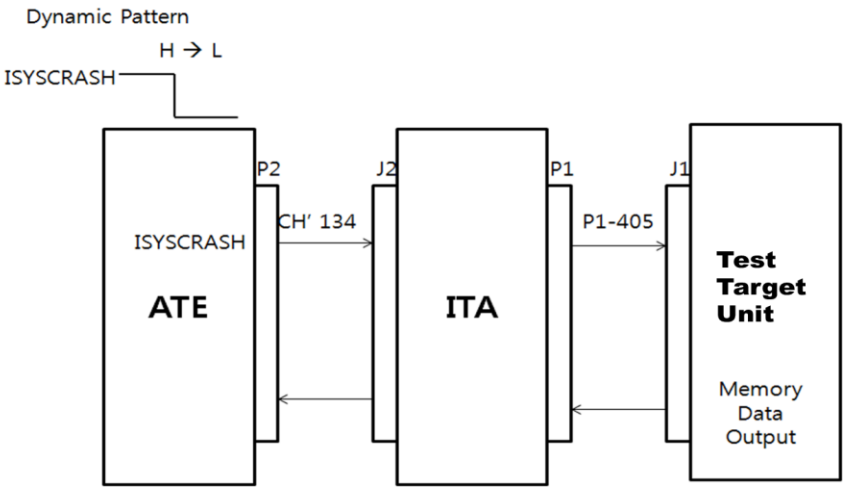


Figure 7. Operation Concept of Dynamic Pattern

As shown in Table 1 and Figure 7, in order to control MEMREQ signal of the test target objects, Dynamic Pattern signals will be added through P1-507 of the input pin number (Pin No) of the test target object and channel 192 of ATE (DTI CH). ISYSCRASH signals will maintain as the initial signal High through P1-405 of the test target object's input pin number (Pin No) and channel 134(CH' 134) of ATE (DTI CH) and then change High to Low to get the outcome.

3.6. Validation & Verification

Finally, faults will be diagnosed by realizing the function of circuit board mounted with ASIC by running the test program after installing the test target unit in ATE. If the data flowing through the pattern has no problem, it is considered as PASS, and if fails, abnormal signal occurs to notice the fault was found to the user, which enables to diagnose the fault.

4. Experiment Results

Test target unit has extracted software from ASIC to handle centralized control of the radar signal processor. We analyzed logic data mounted on ASIC replaced to PALCE16V8 class EE CMOS 20-PIN UNIVERSAL PROGRAMMABLE ARRAY LOGIC manufactured by the ATMEL Company. ATE uses the Teradyne Inc. M9-series Digital Test instrument and the dynamic pattern signal code has been implemented to Visual C++ 8.0.

This chapter carries the result of the experimental procedures explained in chapter 3. Firstly, for extraction the JEDEC Files, we use the ROM Writer which supports ASIC device. Extracted JEDEC Files are converted into the decodable files using JEDEC TO LOGIC EQUATION program. Table 3-(a) illustrates JEDEC file source extracted from ASIC for the test. Extracted JEDEC files are converted into the text format using the equation program (Table 3-(b)).

Table 3. JEDEC File Extraction

JEDEC file generated by PROVIEW* DM TEXAS INSTRUMENTS* DD PAL16L8A* QP20* QF2048* QV0* G0*F0* L00000 11111111111111111111111111111111* L00032 11111111111111111111101110111111* L00064 10101111111110111111111111111111* L00096 00000000000000000000000000000000* — omitted — L01856 11111111111111111111011110111111* L01888 01111011111111111111111111111111* L01920 00000000000000000000000000000000* L01952 00000000000000000000000000000000* L01984 00000000000000000000000000000000* L02016 00000000000000000000000000000000* C5990*	i1=1, i2=2, i3=3, i4=4, i5=5, i7=7, i8=8 GND=10 o12=12, o13=13, o15=15, o16=16, o17=17, o18=18, o19=19 VCC=20 equations /o19 = /i7 * /i8 + /i2 * /i1 * /i5 o19.oe = vcc /o18 = /i4 * /i7 * /i8 + /i2 * /i1 * /i4 * /i5 o18.oe = vcc /o17 = i1 * /i5 + i7 * /i8 + i2 * /i5 o17.oe = vcc /o16 = i1 * /i4 * /i5 + /i4 * i7 * /i8 + i2 * /i4 * /i5 o16.oe = vcc /o15 = i4 * /i5 o15.oe = vcc /o13 = /i7 * /i8 + /i2 * /i1 * /i3 o13.oe = vcc /o12 = i1 * /i3 + i7 * /i8 + i2 * /i3 o12.oe = vcc
(a) JEDEC Extraction Source	(b) JEDEC TO LOGIC EQUATION

As a result of implementing the JEDEC to Equation program on the extracted JEDEC files from ASIC, the format of text files which are composed of the 8 inputs and 7 outputs, the power supply part and the connector part will be outputted as shown in Table 3-(b).

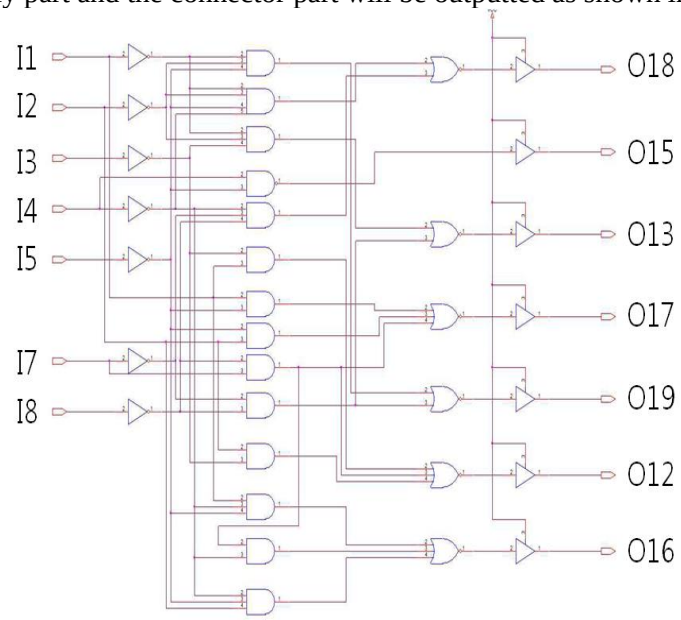


Figure 8. Device Logic Schematic

Text file can be expressed as a circuit drawing by using Or-CAD EDA Tool which is the circuit design program. Figure 8 shows re-designing an Equation text file into a circuit drawing. In order to identify the operation status or function the logic function of ASIC, it shall convert the logic schematic to VHDL(VHSIC Hardware Description Language) which is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits.

After VHDL source coding is completed, we must check whether to perform a compilation syntax error. If the syntax error is not occurred, we simulate the VHDL source. The simulation result is enabled to generate the input/output data signal of TRD as shown in Figure 10. Figure 10 can derive the TRD input and output data shown in Table 1 and Table 2. This I/O data can be applied to the test target unit using the ATE and detected fault defects by comparing the simulation data with acquired date.

Figure 9. VHDL Simulation Result

To accurate fault detection, it connects the test unit board to ITA and applies the control signal to ATE as shown Figure 2. According to the Dynamic Pattern Test signal, if the test unit board is operating normally by the Dynamic Pattern signal, it is considered as PASS, and if abnormal operation, it can diagnose the fault.

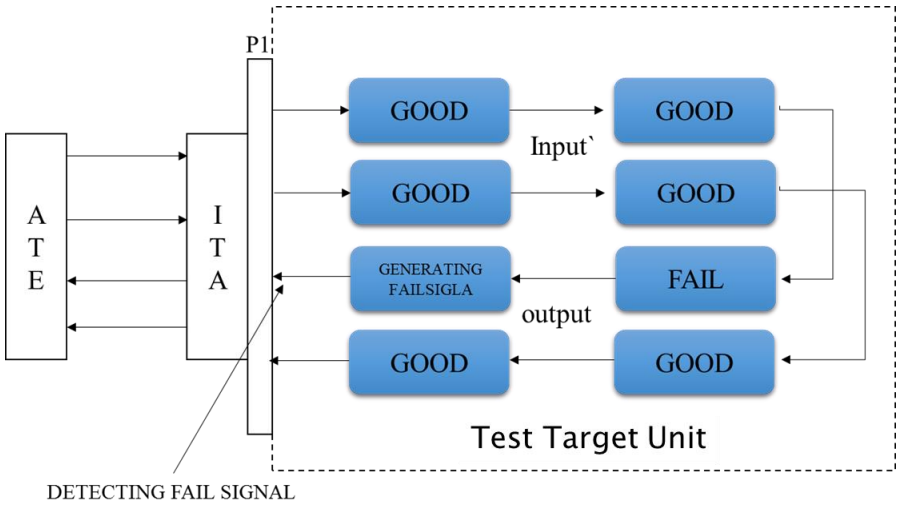
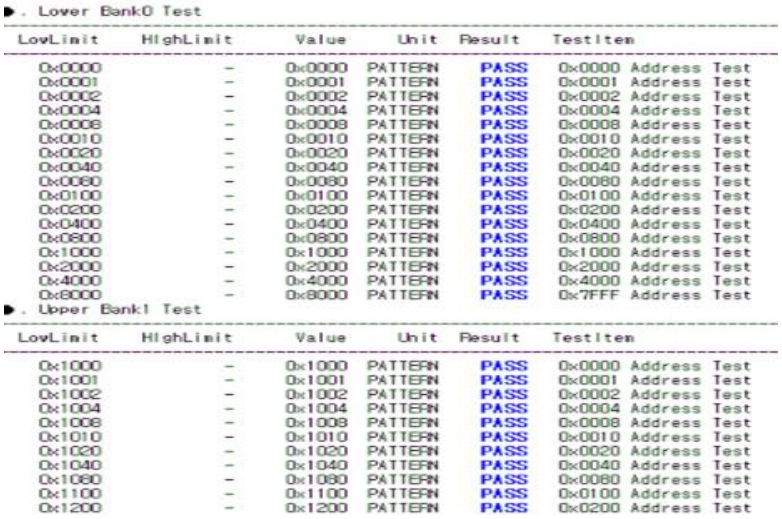


Figure 10. Fault Signal Detecting Method

As described above, we could identify that there was no problem in data transmission in case of normal condition. Figure 11 illustrates the result after comparing the response applied with data signals, coded into the test program. Figure 12 is the result to identify data, applied to signals on the test board, which has been detected as a failure. As the results for comparison of 17 data by each addresses, we could figure that faults exist in 16 addresses. Those faults, demonstrated in accordance with the test result, should be checked in the failure inducing devices tracked down by the user.

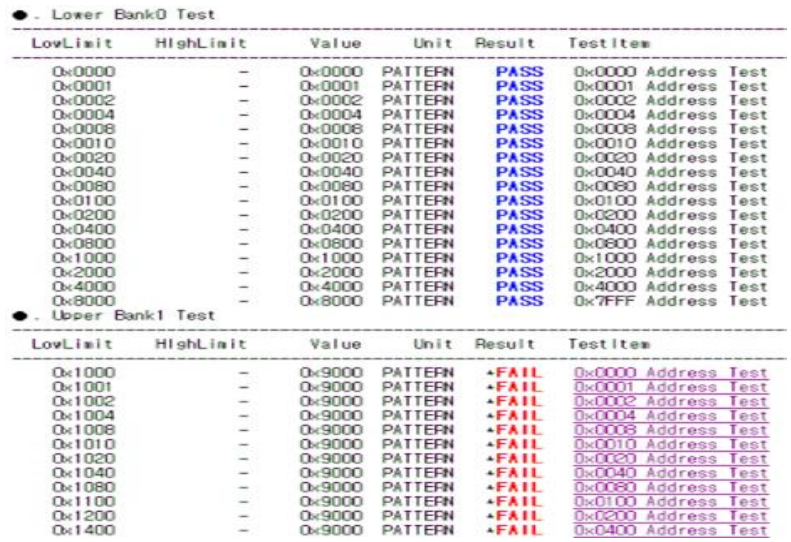

▶. Lover Bank0 Test

LowLimit	HighLimit	Value	Unit	Result	TestItem
0x0000	-	0x0000	PATTERN	PASS	0x0000 Address Test
0x0001	-	0x0001	PATTERN	PASS	0x0001 Address Test
0x0002	-	0x0002	PATTERN	PASS	0x0002 Address Test
0x0004	-	0x0004	PATTERN	PASS	0x0004 Address Test
0x0008	-	0x0008	PATTERN	PASS	0x0008 Address Test
0x0010	-	0x0010	PATTERN	PASS	0x0010 Address Test
0x0020	-	0x0020	PATTERN	PASS	0x0020 Address Test
0x0040	-	0x0040	PATTERN	PASS	0x0040 Address Test
0x0080	-	0x0080	PATTERN	PASS	0x0080 Address Test
0x0100	-	0x0100	PATTERN	PASS	0x0100 Address Test
0x0200	-	0x0200	PATTERN	PASS	0x0200 Address Test
0x0400	-	0x0400	PATTERN	PASS	0x0400 Address Test
0x0800	-	0x0800	PATTERN	PASS	0x0800 Address Test
0x1000	-	0x1000	PATTERN	PASS	0x1000 Address Test
0x2000	-	0x2000	PATTERN	PASS	0x2000 Address Test
0x4000	-	0x4000	PATTERN	PASS	0x4000 Address Test
0x8000	-	0x8000	PATTERN	PASS	0x7FFF Address Test

▶. Upper Bank1 Test

LowLimit	HighLimit	Value	Unit	Result	TestItem
0x1000	-	0x1000	PATTERN	PASS	0x0000 Address Test
0x1001	-	0x1001	PATTERN	PASS	0x0001 Address Test
0x1002	-	0x1002	PATTERN	PASS	0x0002 Address Test
0x1004	-	0x1004	PATTERN	PASS	0x0004 Address Test
0x1008	-	0x1008	PATTERN	PASS	0x0008 Address Test
0x1010	-	0x1010	PATTERN	PASS	0x0010 Address Test
0x1020	-	0x1020	PATTERN	PASS	0x0020 Address Test
0x1040	-	0x1040	PATTERN	PASS	0x0040 Address Test
0x1080	-	0x1080	PATTERN	PASS	0x0080 Address Test
0x1100	-	0x1100	PATTERN	PASS	0x0100 Address Test
0x1200	-	0x1200	PATTERN	PASS	0x0200 Address Test

Figure 11. Normal Test Results


● . Lower Bank0 Test

LowLimit	HighLimit	Value	Unit	Result	TestItem
0x0000	-	0x0000	PATTERN	PASS	0x0000 Address Test
0x0001	-	0x0001	PATTERN	PASS	0x0001 Address Test
0x0002	-	0x0002	PATTERN	PASS	0x0002 Address Test
0x0004	-	0x0004	PATTERN	PASS	0x0004 Address Test
0x0008	-	0x0008	PATTERN	PASS	0x0008 Address Test
0x0010	-	0x0010	PATTERN	PASS	0x0010 Address Test
0x0020	-	0x0020	PATTERN	PASS	0x0020 Address Test
0x0040	-	0x0040	PATTERN	PASS	0x0040 Address Test
0x0080	-	0x0080	PATTERN	PASS	0x0080 Address Test
0x0100	-	0x0100	PATTERN	PASS	0x0100 Address Test
0x0200	-	0x0200	PATTERN	PASS	0x0200 Address Test
0x0400	-	0x0400	PATTERN	PASS	0x0400 Address Test
0x0800	-	0x0800	PATTERN	PASS	0x0800 Address Test
0x1000	-	0x1000	PATTERN	PASS	0x1000 Address Test
0x2000	-	0x2000	PATTERN	PASS	0x2000 Address Test
0x4000	-	0x4000	PATTERN	PASS	0x4000 Address Test
0x8000	-	0x8000	PATTERN	PASS	0x7FFF Address Test

● . Upper Bank1 Test

LowLimit	HighLimit	Value	Unit	Result	TestItem
0x1000	-	0x9000	PATTERN	*FAIL	0x0000 Address Test
0x1001	-	0x9000	PATTERN	*FAIL	0x0001 Address Test
0x1002	-	0x9000	PATTERN	*FAIL	0x0002 Address Test
0x1004	-	0x9000	PATTERN	*FAIL	0x0004 Address Test
0x1008	-	0x9000	PATTERN	*FAIL	0x0008 Address Test
0x1010	-	0x9000	PATTERN	*FAIL	0x0010 Address Test
0x1020	-	0x9000	PATTERN	*FAIL	0x0020 Address Test
0x1040	-	0x9000	PATTERN	*FAIL	0x0040 Address Test
0x1080	-	0x9000	PATTERN	*FAIL	0x0080 Address Test
0x1100	-	0x9000	PATTERN	*FAIL	0x0100 Address Test
0x1200	-	0x9000	PATTERN	*FAIL	0x0200 Address Test
0x1400	-	0x9000	PATTERN	*FAIL	0x0400 Address Test

Figure 12. Abnormal Test Results

5. Conclusion and Future Works

The ASIC for control of the digital signal is progressing in the development of the avionics of the aircraft. In addition, the proportion used the ASIC in the industries is increasing continuously. However, it occurs the difficult problems of the maintenance of ASIC fault due to the maintenance company's bankrupt, equipment's aging, test equipment exchange and test requirement document's absence in the case of avionics

systems. Therefor it will be expensive repair costs. To solve this problems, we proposed the method to testing the analog board with ASIC and without the TRD.

In this paper, we extracted JEDEC file targeting this ASIC by utilizing the program for general purpose on logic data of internal ASIC, and, the logic simulation was possible based on the extracted data and the logic simulation was also possible by using the extraction of circuit design. Based on the analyzed data, we developed the test program to control the test, and applying to ATE, we realized the fault research possible. We could identify the 17 pattern from tests, and figure out faults in 16 addresses. According to the experiment for target board applied with proposed methods, it is possible to diagnose fault for abnormal computerized chip, ASIC, by utilizing test unit board. We've also obtained the excellent performance for fault detection.

However, as such algorithm was applied to a specific ASIC and the ASIC unable to extract more integrated and functionalized internal logic was impossible to be analyzed, it is indeed that more researches and efforts may be required for applying the methods suggested by this paper. Therefore, it remains a challenge to evolve through a further study in order to the similar test devices.

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