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Ring-Oscillator Type Multi-Chip Clock Signal Synchronization Technique with In-Phase Clock Bus Lines

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Abstract

This paper suggests a simple method to solve the clock skew problem generated on two or several separate chips when voltage difference, or gradient, occurs between/among the chips. Generation and distribution of clock signals with minimum skews becomes a critical factor in overall system performance in today's GHz operation speed. With a few connection lines, similar to Data Bus, between two chips, named CBL (Clock Bus Line), a multi-chip synchronization method is newly proposed and proved through simulations and TTL chip measurements. With 2% of supplied voltage differences in different chips, within 3% of the period clock skew is guaranteed in this new scheme.

A feasible way of implementation of this CBL method in today's integrated circuits is also described along with CMOS layout.

Keywords*: Ultra-high-speed oscillator, System-on-Chip, Clock generation and distribution, Synchronization, Supply voltage gradient, PLL, Clock skew*

1. Introduction

In today's GHz range of digital systems, clock generation and distribution is an essential engineering factor because the clock skew becomes critical, and needs to be controlled within a certain range, guaranteeing system synchronization in a few pico-seconds time window [1]. Especially, when a set of chips are operating in the digital systems, synchronization among those chips becomes an issue for unlike a single chip, where the transistors are designed in micro-meter scale, the synchronization on printed circuit board needs to handle external centimeter scaled interconnection lines between chips [2]. When supply voltage difference happens between two chips, even with a few millivolt deference will yield this skew problem between chips if they are operating in ultra-high-speed, say GHz range, and can cause malfunction of the digital system.

Data bus, or data bus lines, is well known in digital communication, as a set of data lines through which data, 256bits, for instance, are exchanged between chips in a single chip or, on printed circuit board. Exact same concept can be applied to clock lines, named Clock Bus Line (CBL), for a set of different phase clock signals of the digital system. This new technique can be easily implemented if we use a simple ring oscillator for a clock generator.

Although Phase Locked Loop (PLL) are a widely-used means in detecting phase difference and making circuit synchronized, its complicated structure with voltage-controlled oscillator, phase detector not only increase wiring area in essential layout design but also inevitable clock skew and Jitter in distributing clock signals[3-4].

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The technique suggested in this paper can minimize the clock skews between clock signals generated under asymmetrical voltage condition in a very simpler way than the existing PLL method above mentioned [6]. Moreover, it allows us to reduce layout design area in current well-developed CMOS technology.

Ring oscillator is composed of three inverting amplifiers [5]. In a triangular layout, having one inverter at each node, this basic ring oscillator can be expanded and spread out in two dimensional, yielding a Cellular Oscillator Network (CON) [2]. In simulations and tests, this CON has been proven to have robustness against temperature and voltage gradient in a single chip [7-8]. At the same time, by using a different cell that is composed of nine inverters, instead of original three inverters, this CON is proven to function a frequency modulator as well [9-10].

In this paper, a possible application of the CON in two or several separate chips as clock generation and distribution is seek and studied. In a GHz speed and with supply voltage difference between chips, a new way for minimizing system clock skew is proposed.

Section 2 describes the structure of ringing oscillator and multi-chip clock signals distribution and synchronization with In-phase Clock Bus Lines technique insensitive to supply voltage variation. Section 3 describes the results and verification measured by using SPICE simulations along with TTL hardware test. Section 4 describes conclusions of this research.

2. Clock Distribution technique with CMOS Ring Oscillator Network

2.1. CMOS Ring Oscillator Network

Figure 1 show a ring oscillator network spread out in two dimensions. At the center, with triangle of nodes 10, 11, and 12, a ring oscillator is composed of three inverting amplifiers. Notice here that each branch is shared adjacent three triangles, 10-8-12, 11-9-10, and 12-7-11, composing four ring oscillators with nine inverting amplifiers. Likewise, if each and every branch of this basic triangle is shared with an adjacent cell, this structure can spread out infinitely in 2D in a fractal mode as seen in Figure 1 [7-10]. We named this structure Cellular Oscillator Network (CON), and if we use a simple inverter, with one PMOS and one NMOS transistors, the simplest form of CON can be designed and implemented easily in today's well-established CMOS technology.

Since it is based on ring oscillators, every node will have the same frequency oscillatory wave, with exact 50% of duty cycle [5]. Three nodes of a basic cell have three different waves, with $\frac{2}{3}\pi$ phase a part between each, meaning there are only three different clock in-phase signals generated from the CON. Nodes 1-7-10-4, 2-9-12-5, and 3-8-11-6 are those different in-phase nodes in Figure 1. Thus, theoretically, the CON has infinite number of clock signals, and with feedback connections in the networks, each and every in-phase node will have synchronized signals with minimum skews among them.

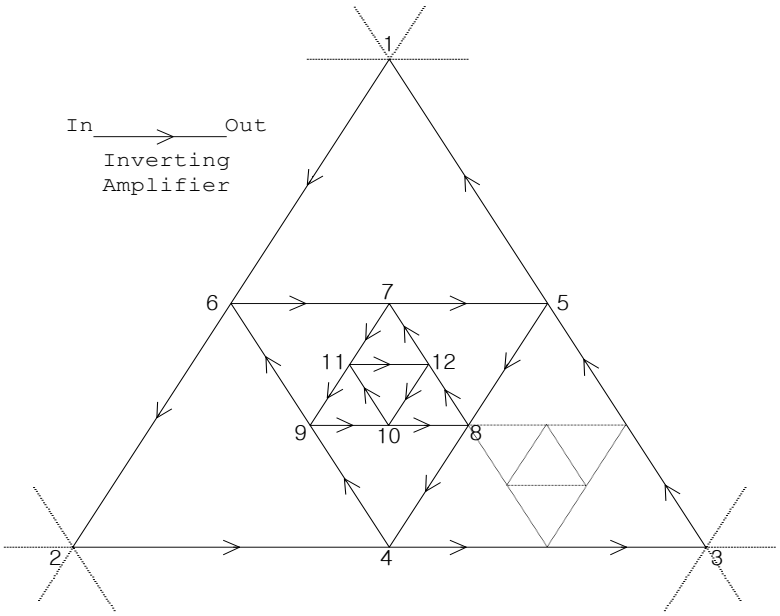


Figure 1. Conceptual Diagram for Ring Oscillator in 2-D Spread

Figure 2 shows a concept of Clock Bus Line (CBL) between two chips for synchronization. With only three CBLs between in-phase nodes of two chips, system clock synchronization can be achieved. It has an advantage in reducing wiring area in layout due to simple formation of it.

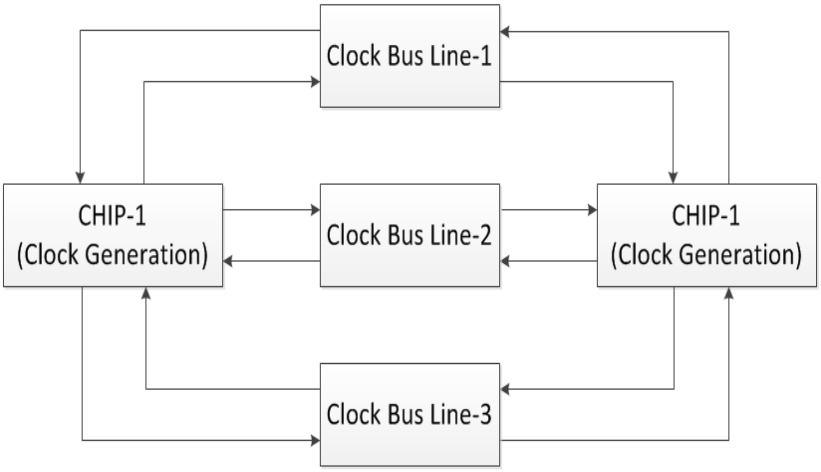


Figure 2. Proposed Clock Bus Lines Diagram between Two Chips

2.2. Clock Signals Generation and Synchronization Technique with Two Oscillator Networks

Figure 3 shows a possible composition of two chips designed with the proposed method. Two CONs are used in two different chips, and each CON consists of 30 inverters. Two chips (CHIP-1, CHIP-2) are connected with three Clock Bus Lines and seen in the Figure 3, between three different in-phase nodes of two chips. We claim here in this scheme, that although a supply voltage difference exists between two chips, this CBL technique can minimize clock skew between two chips.

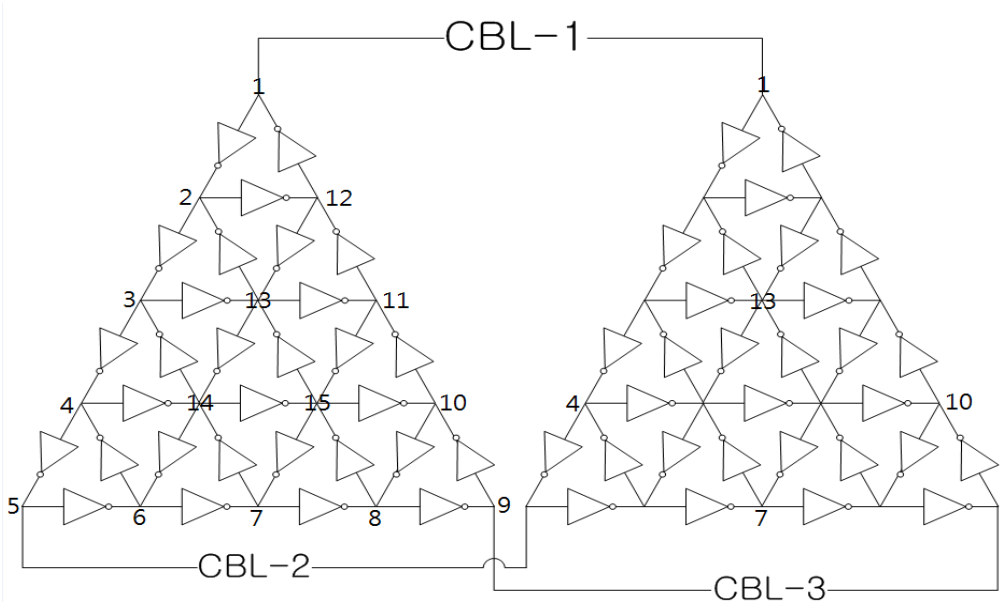


Figure 3. Circuit Diagram for the CON in Two Chips with Clock Bus Line

Figure 4 depicts a structural diagram of Figure 3 using stacked layers in today's multi-layer CMOS processing technology. Due to the simplicity of the CBL method, wiring overload between two chips can be minimized.

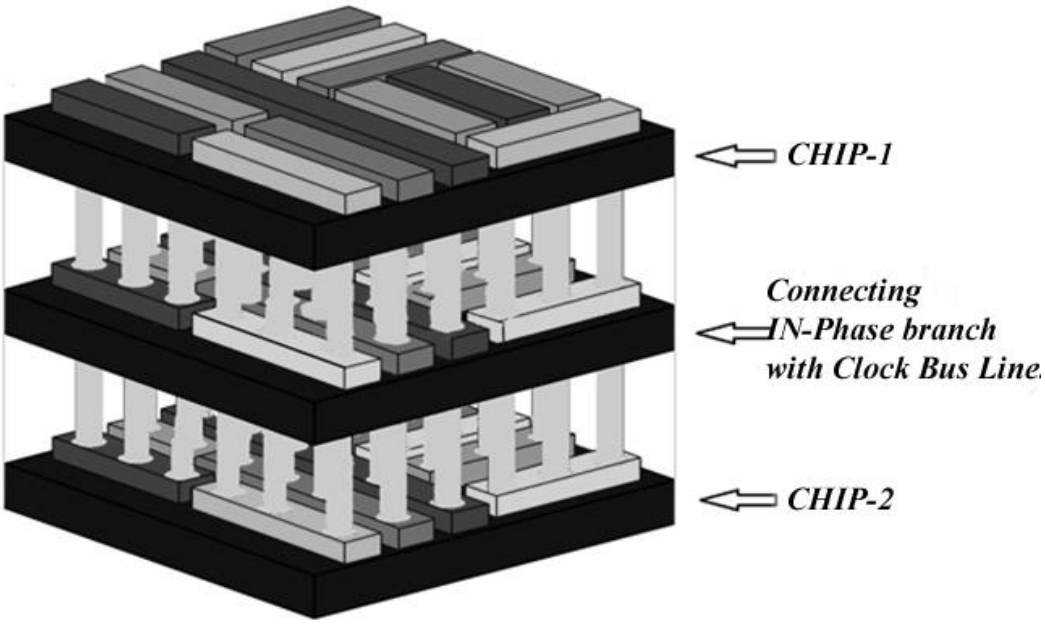


Figure 4. Multi-Layer Diagram of Clock Bus Line in A Stacked Structure

2.3. Hardware Implementation and Test with Low-Speed TTL Chips

Not just simulations, but for actual measurements, hardware implementation for the Cellular Oscillator Networks with Clock Bus Lines for two chips is set up as seen in Figure 4. Each CON consists of five TTL chips (7404) and external three CBLs are connected between three different in-phase nodes.

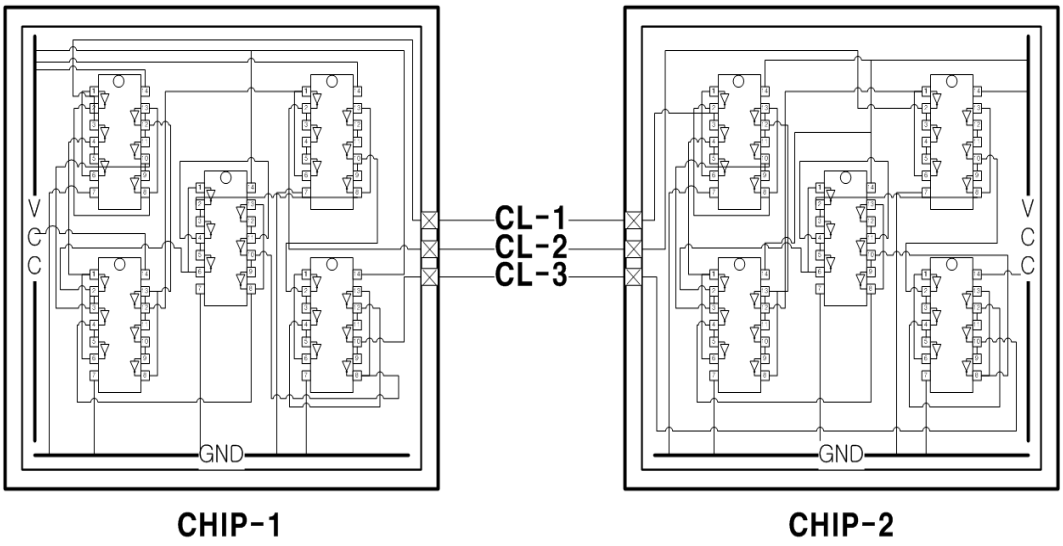


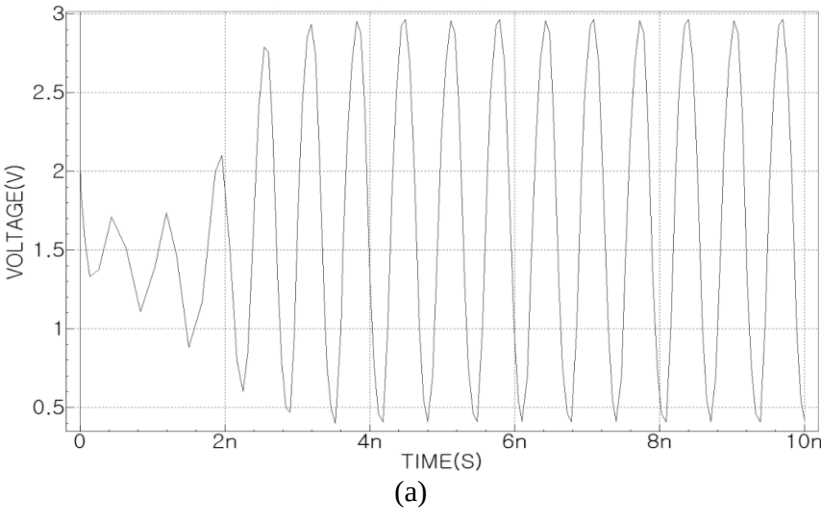
Figure 5. TTL Ring Oscillator Network Diagram for Two Chips for a Test

Although this circuit will operate at much lower frequency range than CMOS chips, we expect the nature of Cellular Oscillator Network with CBL for synchronization can still be tested.

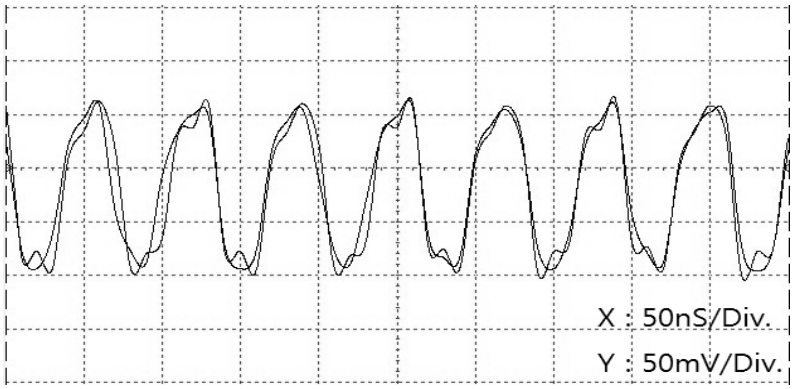
3. Spice Simulations and Measurements

3.1. With the Same Supply Voltage

Figure 6 shows two in-phase clock signals from two chips when given the same power supply voltage, simulation (a) and measurement (b), respectively. As seen, two waves from two chips are exactly same, with no skews between waves. The waves are from node 13 of two chips in Figure 3.



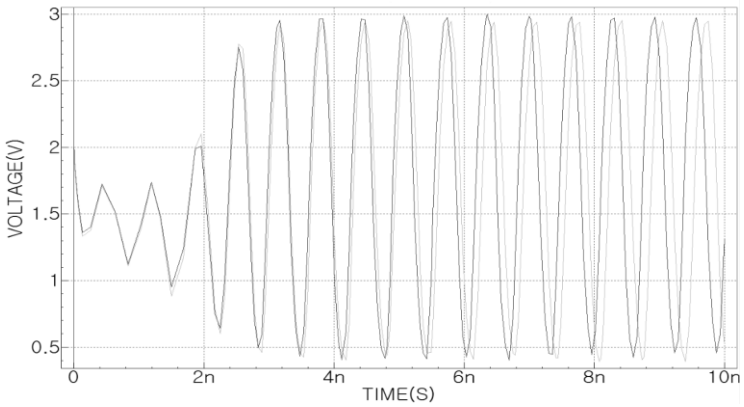
(a)



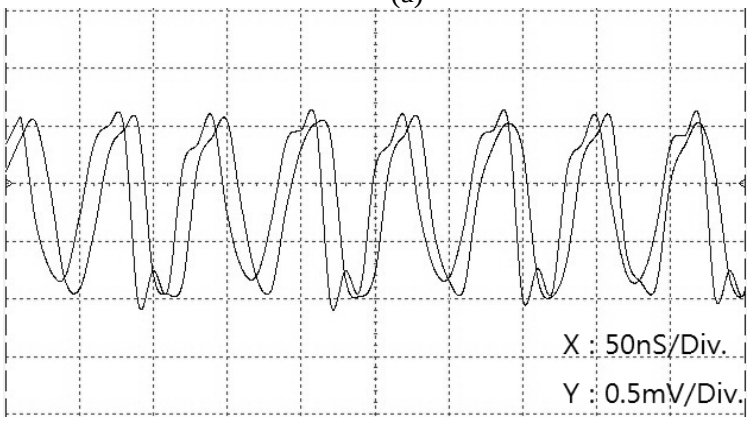
(b)

Figure 6. Output Waveform of Ring Oscillator with the Same Supply Voltages between Two Chips: (a) SPICE Simulation and (b) Measurement Waveform

Now, with a 1% power supply voltage increase in CHIP-2 with respect to CHIP-1, a clock skew is witnessed between two clock signals in Figure 7, (a) SPICE simulation, and (b) measurement. CHIP-1 has 3V supply voltage, while CHIP-2 has 3.03V. As seen, in Figure 7 (a) and (b), noticeable skew is simulated and measured, caused by supply voltage difference between chips.



(a)



(b)

Figure 7. Output Waveform of Ring Oscillator with +1% of a Voltage Difference: SPICE Simulation and (B) Measurement Waveform

Figure 8 displays magnified skew, measured at the center voltage level, here 1.5V, in Figure 7. Approximately, 4.8ns skew was measured between two waves in Figure 8 (b).

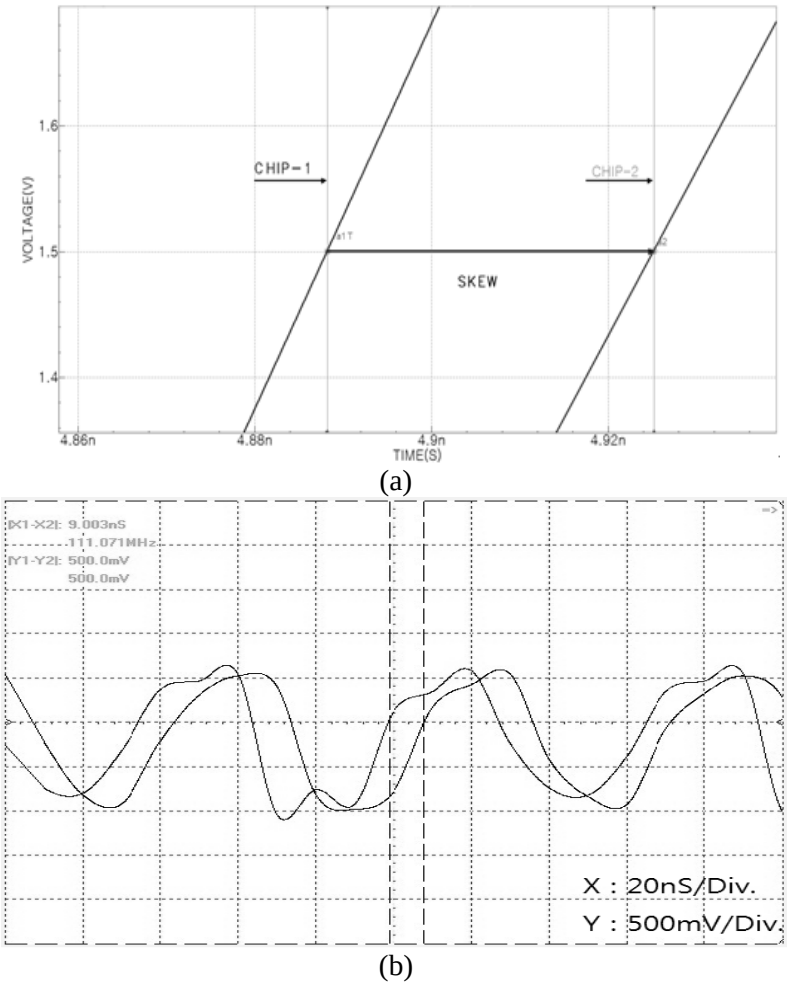


Figure 8. Output Waveform of Ring Oscillator for +1% of a Voltage Difference: (A) SPICE Simulation and (B) Measurement Waveform

In the same way, clock signal skews are simulated and measured with ±2% of voltage difference between two chips, where we expect more skews between two chips.

Figure 9 summarizes measured clock skews from simulations and TTL circuit measurements of Figure 5. Up to 143ps skew is seen from simulation result, with 2% voltage difference between two chips, which is 22% of clock period.

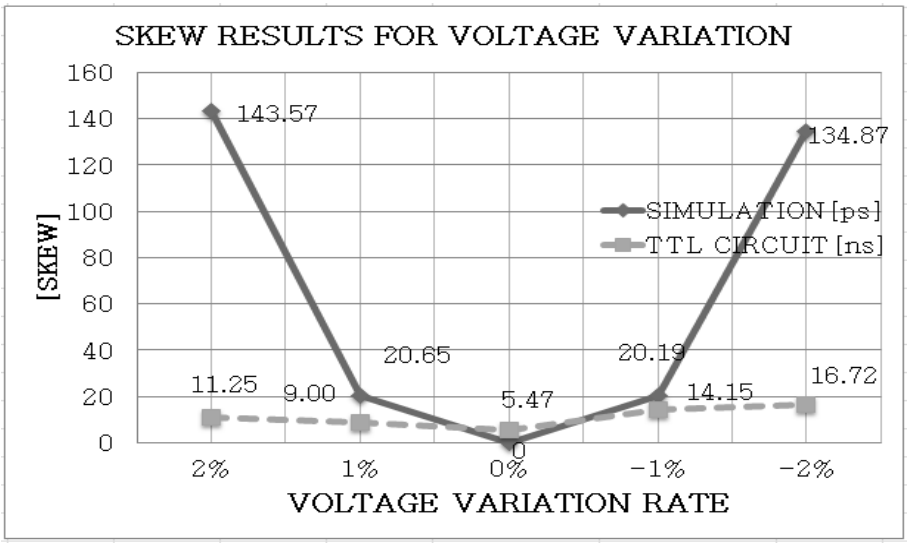
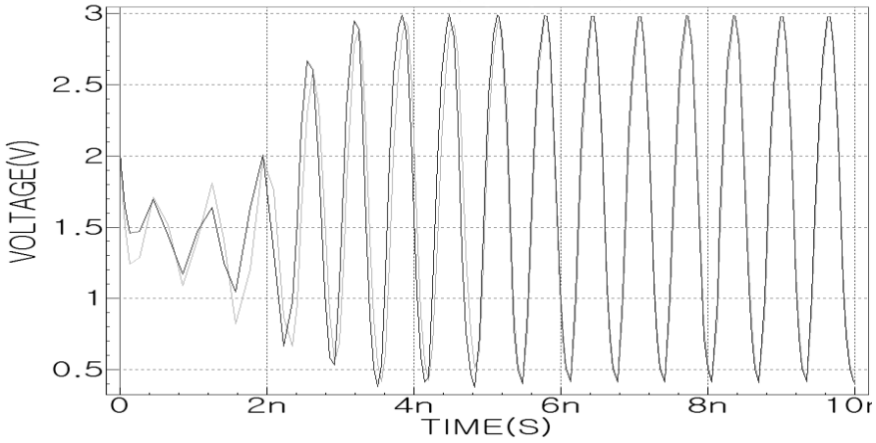


Figure 9. Skews from SPICE Simulations and Measurements of Figure 5 Due To Voltage Variation of CHIP-2

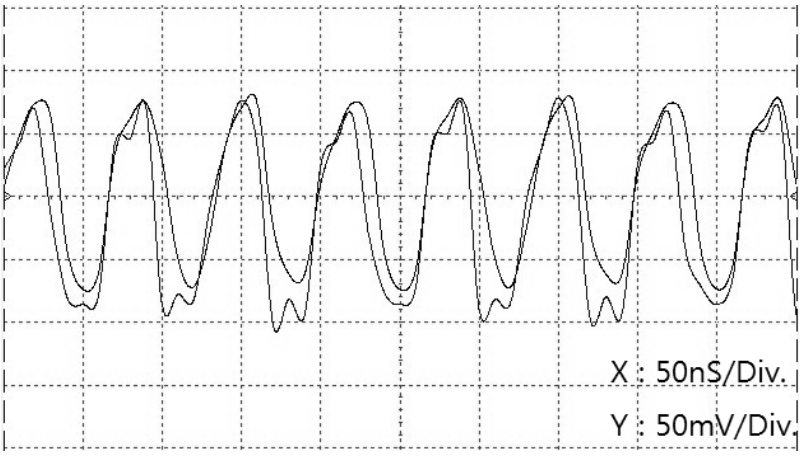
3.2. Proposed Clock Bus Line Synchronization Technique with voltage differences

Figure 10 shows both simulation and measurement results, now with three Clock Bus Line (CBL) between two chips as shown in Figure 3 and Figure 5. Three in-phase nodes between to chips are connected with +1% of voltage difference, seen in Figures 7 and 8.

Compared with Figures 7 and 8 without CBLs between two chips, now severely decreased skews are achieved and measured.



(a)



(b)

Figure 10. Output Waveforms with +1% of a Voltage Difference: (a) SPICE Simulation and (b) Measurement Waveform

Figure 11 summarizes clock skews measured the same node with CBLs. Compared with Figure 9 now, a significant decreased skew both in simulation 3% and measurements 1.63% are achieved.

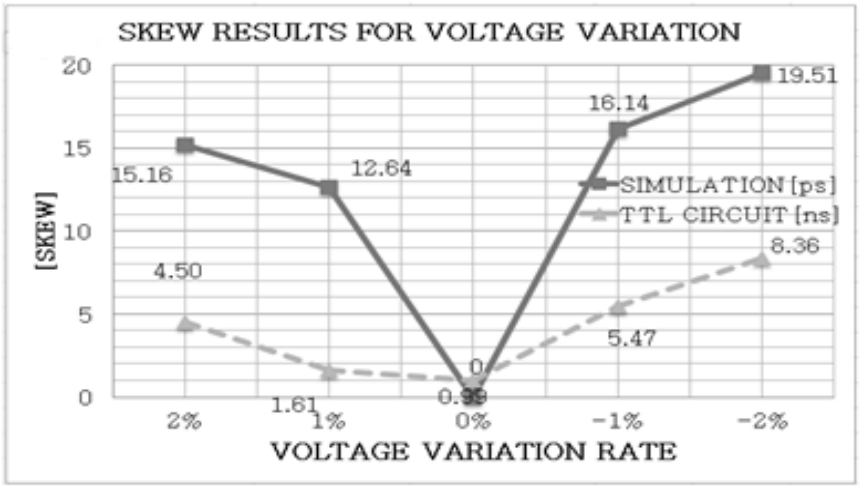


Figure 11. Clock Skews with a Voltage Variation and Measured Value of a TTL Circuit (Time Unit: Simulation (ps), TTL (ns))

Figure 11 indicates a clock skew measured on a point IN-Phase of each of Two chips. It indicates there is an improvement in a clock skew and clock synchronization problem under maximum of 2% of a voltage variation.

Figure 12 shows the layout of a CMOS ring oscillator with 108 CMOS inverters.

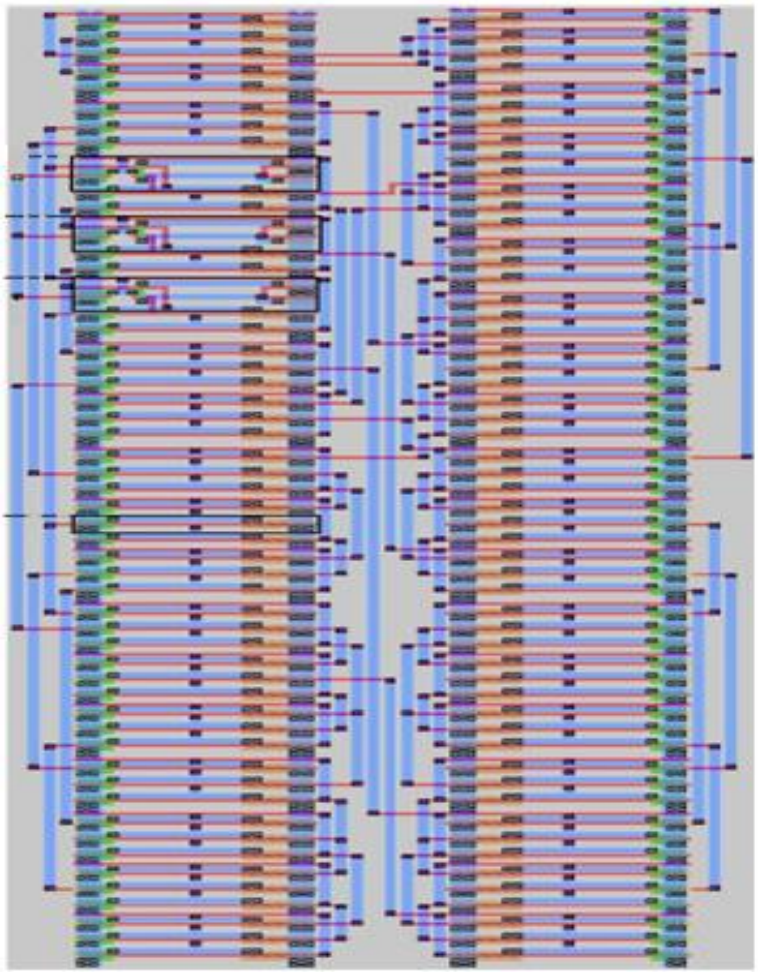


Figure 12. CMOS Ring Oscillator Layout

4. Conclusion

This paper introduces Ring Oscillator type of multi-chip clock signals distribution and synchronization with In-Phase clock bus line technology. This is a technique that synchronizes clock signals generated on two separate chips through an advanced concept of Clock Bus Line (CBL) with simple ring oscillators, insensitive to voltage variation. The composition of circuit could be realized relatively simply, which makes designer could extend freely depending on system complexity. It also improves and minimizes clock skew problem inevitably generated for generation and distribution of clock signals. Skew measured is within 3% (19.51ps) despite max 2% of voltage variation on a SPICE simulation standard. The CBL method proposed in this paper can be realized in reducing wiring area by simplifying circuit structure. Chip design and fabrication are under way for test in GHz range in the future.

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