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Low Area Complexity Demultiplexer Based on Multilayer Quantum-dot Cellular Automata

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Abstract

Nanoscience and nanotechnology involve the ability to see and to control individual atoms and molecules. A quantum-dot cellular automata(QCA) is one of the attractive alternative technology among nanotechnology solutions. Demultiplexer is used in communication systems to convert the serial data to the parallel data. A demultiplexer receives the output signals from the multiplexer. For that reason, it is important components for making integrated circuit. This work target is designing a high optimized demultiplexer in QCA framework. We proposed designs of 1:2 and 1:4 demultiplexer and the simulation results reveal that our proposed designs have significant improvements, such as low complexity and power consumption aspects.

Keywords*: Nanotechnology, Quantum-dot cellular automata, Demultiplexer*

1. Introduction

Microelectronics have been expressive developed for the last five decades, and has resulted in integrated circuits with device densities of tens of millions of transistors per chip. As a result, this kind of integration has caused an increase in non-ideal device behavior, such as leakage currents through the gate, resulting in chip power density levels comparable to a hot plate and set to approach that of nuclear reactors. QCA is a binary logic architecture which can make on a smaller digital circuit at the nanotechnology levels and operate at very low power levels [1].

Quantum dots are nanostructures created from standard semi conductive materials. These structures are modeled as quantum wells. They exhibit energy effects even at distances several hundred times larger than the material system lattice constant. A dot can be visualized as well. Once electrons are trapped inside the dot, it requires higher energy for electron to escape. QCA is a new technology that attempts to create general computational functionality at the nanoscale by controlling the position of single electrons [2, 3]. QCA devices encode and process binary information as charge configurations in arrays of coupled quantum dots, rather than current and voltage levels. In the last few years, several basic QCA elements: a QCA cell, small binary wire, and digital logic gate and also some combinational circuits, have been demonstrated [1, 2].

We presented the novel QCA demultiplexer design using quantum-dot cellular automata technology which is a very effective and efficient way of manufacturing the nano devices. The proposed design reduced the number of QCA cells and also minimized total area of circuit when compared to previously reported design.

This paper is organized as follows. Section 2 introduces QCA basic concepts and about demultiplexer basically. Previously designed 1:2 and 1:4 demultiplexers are discussed and proposed design demonstrated in section 3 and in section 4 respectively. Section 5

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compares and analyzes the efficiency and performance between the proposed and previous structures. Finally, we conclude the paper in section 6.

2. Related Works

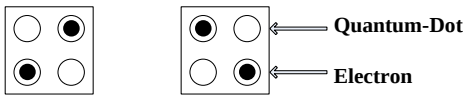
2.1. Basic QCA

QCA is implemented by quadratic cells, the so-called QCA cells. Basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. Tunneling action only occurs within the cell and no tunneling happens between cells. The numbering of the dots (denoted as *i*) in the cell goes clockwise starting from the dot on the top right: top right dot *i*=1, bottom right dot *i*=2, bottom left dot *i*=3 and top left dot *i*=4. A polarization *P* in a cell is defined as:

$$P = \frac{(\rho 1+\rho 3)-(\rho 2+\rho 4)}{(\rho 1+\rho 2+\rho 3+\rho 4)} \quad (1)$$

where ρ*i* denotes the electronic charge at dot *i*. The polarization measures the charge configuration that is, the extent to which the electronic charge is distributed among the four dots [4].

If two excess electrons are placed in the cell, coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations, as shown in Figure 1, which can be labeled logic "0" and "1". If two cells are brought close together, coulombic interactions between the electrons cause the cells to take on the same polarization. If the polarization of one of the cells is gradually changed from one state to the other, the second cell exhibits a highly bi-stable switching of its polarization [5].



P = +1 (Binary 1) P = -1 (Binary 0)

Figure 1. Basic Four-Dot QCA Cell

If two QCA cells are placed next to each other, it is possible to exchange their states. The QCA cell that should transfer its state to a neighboring cell have to be open, to allow the electrons to travel through the tunnel junctions between the potential wells. As soon as they open, the electrons in the neighboring cell are pushed by the coulomb force of the original cell as far away as possible. As they also are pushed away from each other, they will travel into the same potential wells as in the original cell. As soon as the tunnel junctions are closed again, the transfer of the state is completed.

The state of a cell can also be transferred to multiple neighboring cells. It works the very same way as with a single neighbor cell, but the tunnel junctions of all the sequentially neighboring cells should be open at the same time, which makes the transfer much faster than transferring the state cell by cell. This allows us to build "wires", made of QCA cells, to transport information over larger distances [6].

The simplest QCA array is a line of cells, shown in Figure 2(a). Since the cells are capacitively coupled to their neighbors, the ground state of the line is for all cells to have the same polarization. In this state, the electrons are as widely separated as possible, giving the lowest possible energy. To change the polarization of the line, an input is applied at the left end of the line, forcing it to one polarization. Since the first and second

cells are now of opposite polarization, with two electrons close together, the line is in a higher energy state and all subsequent cells in the line must flip their polarization to reach the new ground state.

An inverter or NOT, is shown in Figure 2(b). In this inverter the input is first split into two lines of cells then brought back together at a cell that is displaced by 45° from the two lines, as shown. The 45° placement of the cell produces a polarization that is opposite to that in the two lines, as required in an inverter [5].

AND and OR gates are implemented using the topology shown in Figure 2(c), called a majority gate. Majority gate consist of five QCA cells that realize the following equation:

$$M(A,B,C) = AB + BC + AC \tag{2}$$

In this gate three inputs "vote" on the polarization of the central cell and the majority wins. The polarization of the central cell is then propagated as the output. One of the inputs can be used as a programming input to select the AND or OR function. If the programming input is logic 1 then the gate is an OR, but if a 0 then the gate is an AND. For example, a two-input AND gate is realized by fixing one of the majority gate inputs to "0":

$$AND(A,B) = M(A,B,0) = AB \tag{3}$$

Similarly, an OR gate is realized by fixing one input to "1".

$$OR(A,B) = M(A,B,1) = A + B \tag{4}$$

Thus, with majority gates and inverters it is possible to implement all combinational logic functions [7].

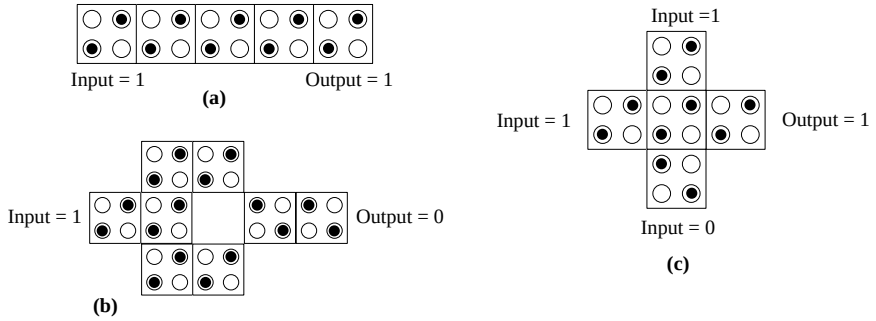


Figure 2. (a) Line of QCA Cells, (b) Inverter of QCA, (c) QCA Majority Gate(MG)

Functional QCA circuits need to be clocked in order to operate correctly. The transitions of QCA states occur under the control of potential barriers between the quantum dots in QCA cells and it is the QCA clock that lowers and raises the tunneling barriers. Clocking not only controls data flow but also serves as the power supply [8].

Therefore, multi phased clocking mechanism is used in the QCA circuit to flow the information. Clock actually provides power to run the circuit. Four distinct and periodic clock signals are required for QCA circuits to operate and these signals are shifted by 90 degree of relative phase difference with each other [9]. Clock signals are generated through an electric field which is applied to the cells to control the tunneling barrier height between the dots within a cell. The cells in each clock zone behave like a single latch. In clocking sequence the device transition occurs from a mono-stable to a bi-stable state.

The clocking scheme can be accomplished by controlling the potential barriers between adjacent quantum dots. The four clocking zones can be divided as switch, hold, release and relax state as shown in Figure 3. In switch phase the actual computation occurs according to the input. Here in this phase, inter dot potential barriers are low first and then barriers and QCA cell become polarized to the state of its input driver. By the end of this clock phase, barriers are high enough and there is no possibility of electron tunneling and hence cell states are fixed. The second phase of clocking at where barriers are still high and does not allow the electron tunneling and hence output of this state can be used as the inputs to the next in the third phase *i.e.* in release phase potential barrier is lowered and electron positions are configured according to the original state. The cells are in relaxed or nonpolarized state which is the fourth clocking phase. So, the overall polarization of the QCA cell is determined in the switch and hold phase where cells are in polarized state depending upon the neighboring cell polarizations.

In realize and relax phases the states are nonpolarized. Therefore, QCA clocking mechanism consist of four clock signals of equal frequencies if one signal considered as reference (phase=0) others are delayed one (phase=$\pi/2$), two (phase=π) and three (phase=$3\pi/2$) quarters of periods. Signals pushed from one clock region to another as the phase of the clock of these regions increases [9].

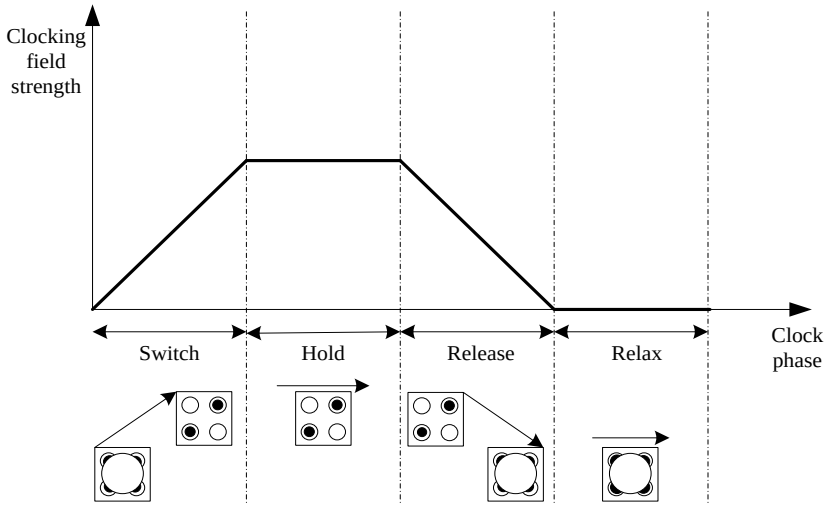


Figure 3. Four Phase of Clock Signal

During the design of QCA circuit, the situation is likely to occur that QCA wires have to be crossed. In contrast to classic transistor technology, where wires can only cross on by inserting another layer, QCA wires can be crossed in the same layer. This works by introducing QCA cell type, where the four potential wells are not in the corners of the cell but in the middle of the edges, as shown in Figure 4.

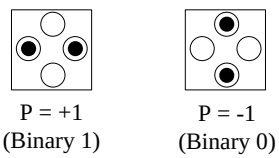


Figure 4. Symmetric Adjustable QCA Cell

If several of these QCA cells are put together to form the wire, the adjustment of the succeeding cell is the inverted to its predecessor and so on. The advantage of this type of QCA cell originates from its symmetric effect of Coulomb force on regular cells. Though

the electrons indeed interact with electrons in neighboring regular QCA cells, but by the symmetry, they do not push the electrons in regular QCA cells to particular adjustment. In the other direction, electrons in the regular cell do not push the electrons in symmetric cell into particular potential well. This allows building wire crossing of these QCA cells with regular ones. A crossing is built by continuous wire of special cells, building a gap in across the wire of regular cells [6].

There exist two representative wire-crossing techniques: a coplanar-based and a multilayer-based. A coplanar-based wire-crossing technique was proposed by Tougaw and Lent [10]. Figure 4(a) shows a simple geometry of the coplanar-based wire-crossing technique. In this example, the vertical (*i.e.,* Y) and horizontal (*i.e.,* X) wires are transmitting the value '1' and '0', respectively.

To implement this wire-crossing, the cells of horizontal wire are rotated by 45 degree. If the length of the vertical wire after an intersection cell is sufficient (that is, the length of the wire is more than or equal to 3), a transmitting value does not affect from the other wire. Also, the horizontal wire should be composed of odd number cells because the property of the rotated cells has an inverter chain that the polarization alternates direction between each adjacent cells.

The other alternative method is a multilayer crossing, which uses more than one layer of cells similar to the routing of metal wires in CMOS technology. Namely, the multilayer-based wire-crossing technique uses a crossover bridge method. This technique is similar to coplanar-based technique in the perspective of the floor plan because it looks like appearance of two wires crossing. In fact, it consists of the stereoscopic structure as shown in Figure 4(b).

Figure 4 (b) shows a simple geometry of the multilayer-based wire crossing technique. In this example, the wire "X" is using a crossover bridge. The structure of this technique can be more miniaturized and generalized than coplanar-based technique because it does not need to rotate cells. Although this technique has some advantages, the noise problem between intersection cells in crossover area is existed. There are also several things to consider for design and simulation processes in QCA Designer such as the number of layers, crossover and vertical cells [11].

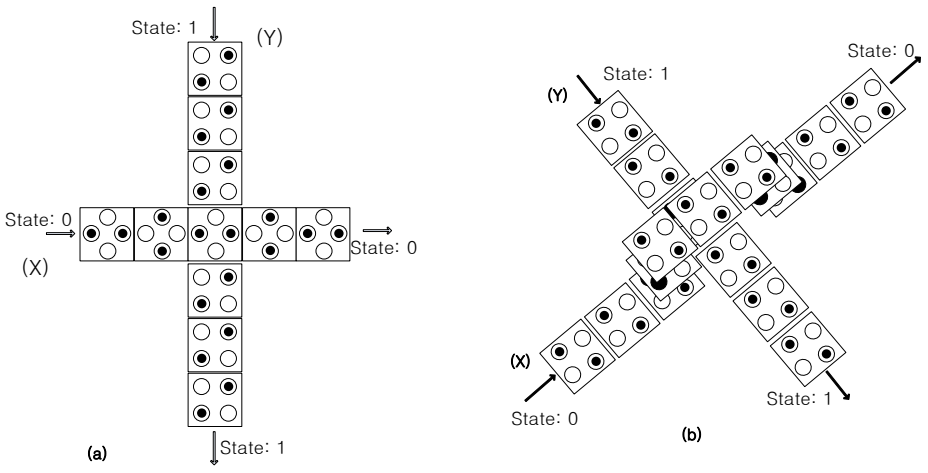


Figure 5. Typical QCA Wire-crossing Techniques: (a) Geometry Example of Coplanar-Based QCA Wire-Crossing, (b) Geometry Example of Multilayer-Based QCA Wire-Crossing

In addition, multilayer crossover wires are not easy to fabricate due to the multiple layer structure and the cost to fabricate a multilayer crossover is expected to be significantly greater than that of a coplanar crossing. The cost difference

between the coplanar and multilayer crossovers affects the overall cost of a design to some extent [12]. However, if we need robust structure, this type of crossover is more suitable for our circuit.

2.2. Demultiplexer

Demultiplexer is the reverse of the multiplexer process – combining multiple unrelated analog or digital signal streams into one signal over a single shared medium, such as a single conductor of copper wire or fiber optic cable. It is located at the receiver end to split the serial high-speed input data stream into parallel outputs [13]. Thus, demultiplexer is reconverting a signal containing multiple analog or digital signal streams back into the original separate and unrelated signals [14].

It is usually used in communication system where multiplexer are used. Most of communication system has function in two directions. In this case, multiplexer and demultiplexer work in system as synchronic. Communication system use multiplexer to carry multiple data like audio, video and other form of data using a single line for transmission. This process makes transmission easier. The demultiplexer receives the output signals of the multiplexer and converts them back to the original form of the data in communication system.

Demultiplexer is also used for reconstruction of parallel data and ALU (Arithmetic Logic Unit) circuits. In this circuit, the output of ALU can be stored in multiple registers or storage units with the help of demultiplexer. The output of the ALU is fed as the data input to the demultiplexer. Each output of demultiplexer is connected to multiple register which can be stored in the registers.

A serial to parallel converter is used for reconstructing parallel data from incoming serial data stream. In this technique, serial data stream is given as data input to the demultiplexer at the regular interval. A counter is attached to the control input of the demultiplexer. This counter directs the data signal to the output of the demultiplexer where these data signals are stored. When all data signals have been stored, the output of the demultiplexer can be retrieved and read out in parallel [15].

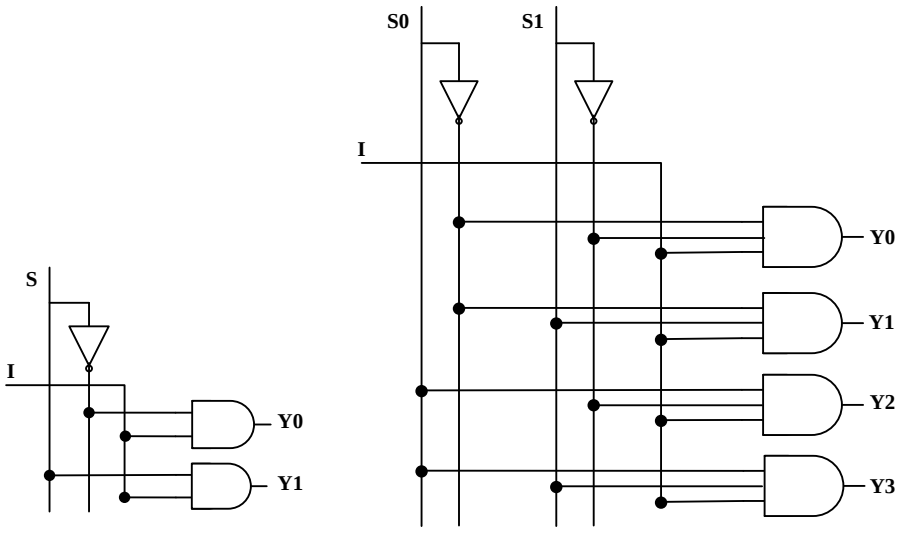


Figure 6. Logic Diagrams of 1:2 and 1:4 Demultiplexer

Although demultiplexer is the reverse of the multiplex process, because the multiple signals are not related, it is not the opposite of multiplexing. The opposite of multiplexing is inverse multiplexing, which breaks one data stream into several related data streams. Thus, the difference between working process of demultiplexer and inverse multiplexing

is that the output streams of demultiplexer are unrelated, but the output streams of inverse multiplexing are related [16].

A related term is channel bank, the foundation of all digital telecommunication transmissions. It is part of a carrier-multiplex terminal serving two functions:

1) Multiplexing a group of (unrelated) channels into a higher bit-rate (transmission speed) channel.
2) Demultiplexing these (unrelated) aggregates back into individual channels.

Table 1. Truth Table of 1:2 Demultiplexer

Select	Input	Output	
S	I	Y1	Y0
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

Table 2. Truth Table of 1:4 Demultiplexer

Input	Select inputs		Outputs			
I	S0	S1	Y3	Y2	Y1	Y0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

3. Previous Demultiplexer

There exist some reported designs of demultiplexer. Some of them prefer to implement QCA demultiplexer using multilayer based wire-crossing technique and others coplanar wire-crossing technique. For example, we can review demultiplexer design to be implemented by author [17]. It is constructed using coplanar wire-crossing technique. Layout of an 1:2 demultiplexer design was illustrated below with two clocking phase and two majority gates.

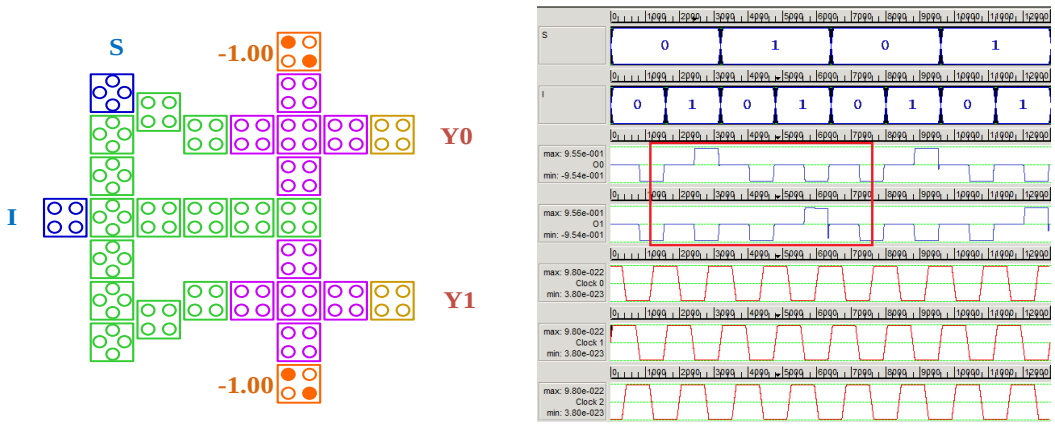


Figure 7. Layout of 1:2 Demultiplexer Design and Simulation in Paper [17]

The second presented 1:4 demultiplexer designed using multilayer wire-crossing technique. It has one input line (IN), two selection lines (SEL_0 and SEL_1) and four output lines (OUT_0, OUT_1, OUT_2, OUT_3). In this structure there are six majority gates and inverters which were implemented using simple inverter. Overall, Demultiplexer used 181 cells and 8 clock zones [18].

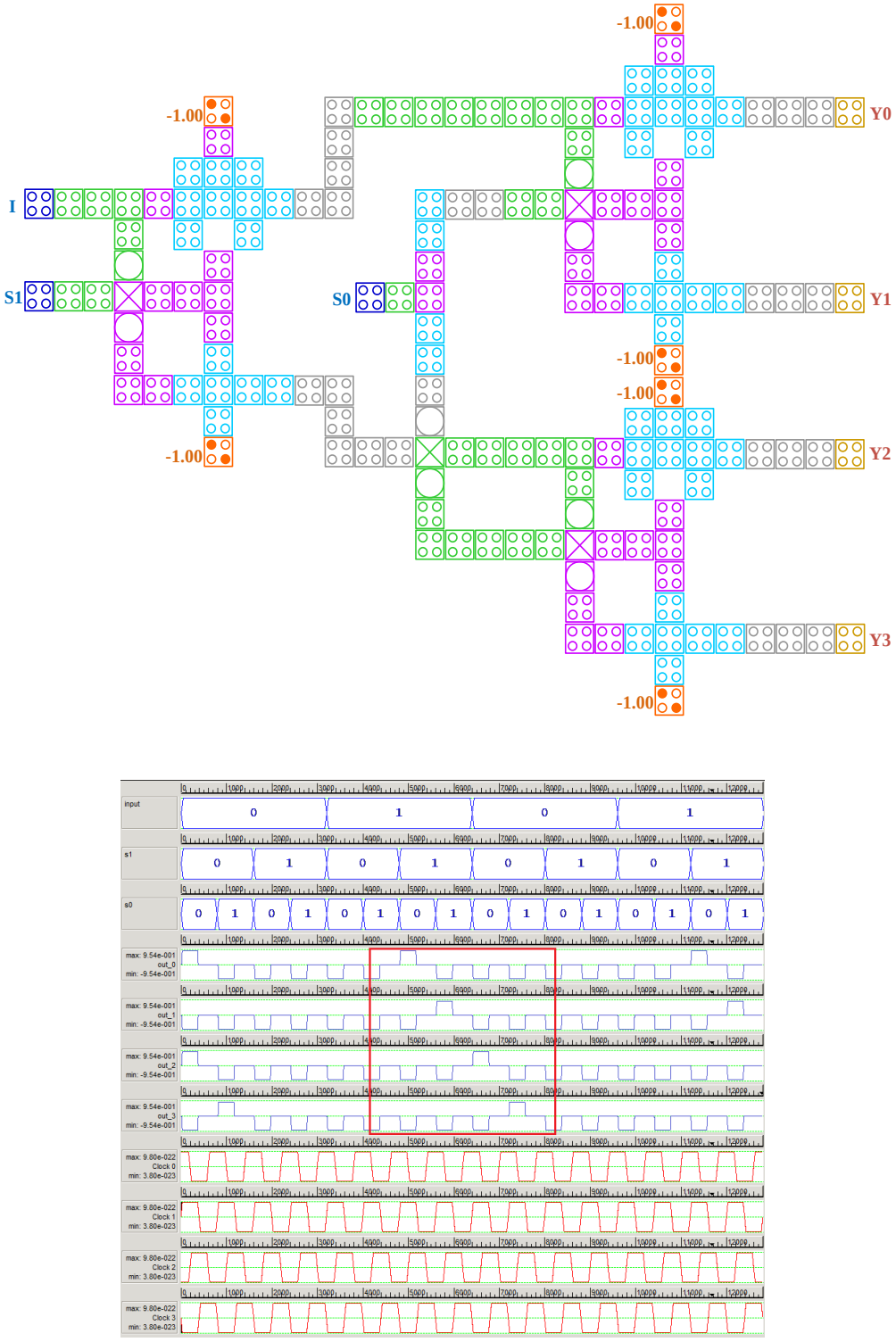


Figure 8. Layout of 1:4 Demultiplexer Design and Simulation in Paper [18]

4. Proposed Demultiplexer

The demultiplexer is a combinational circuit which receives one single input date and then switches it to many n number output lines. The below figure illustrates that how to design our proposed demultiplexer in QCA. Namely, a demultiplexer is used to convert the serial data to the parallel data.

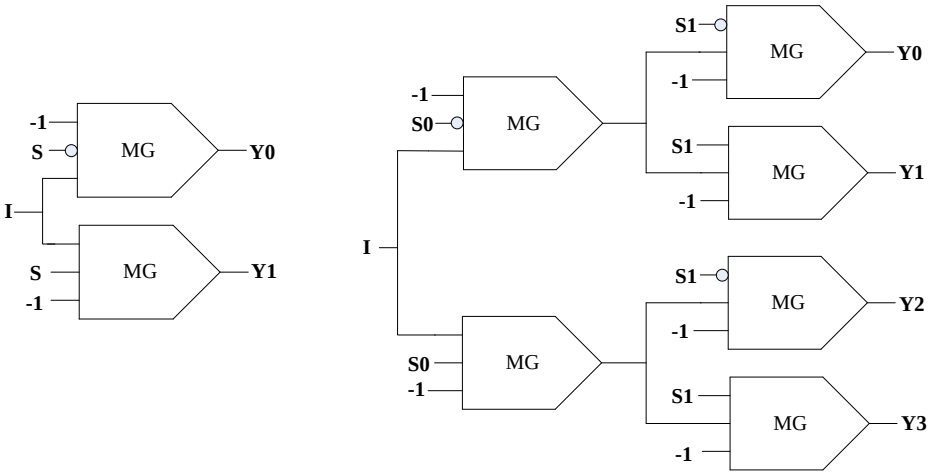


Figure 9. Proposed Diagrams of 1:2 and 1:4 Demultiplexer

4.1. 1:2 Demultiplexer

In this part we present an 1:2 demultiplexer in QCA. The block diagram of the 1:2 demultiplexer pattern is shown in Figure 5, where I is the demultiplexer input signal, S corresponds to the selector input and Y0 and Y1 are the demultiplexer output signals. Its truth table was presented in Table 1. The design and waveform of 1:2 demultiplexer is illustrated in Figure 8.

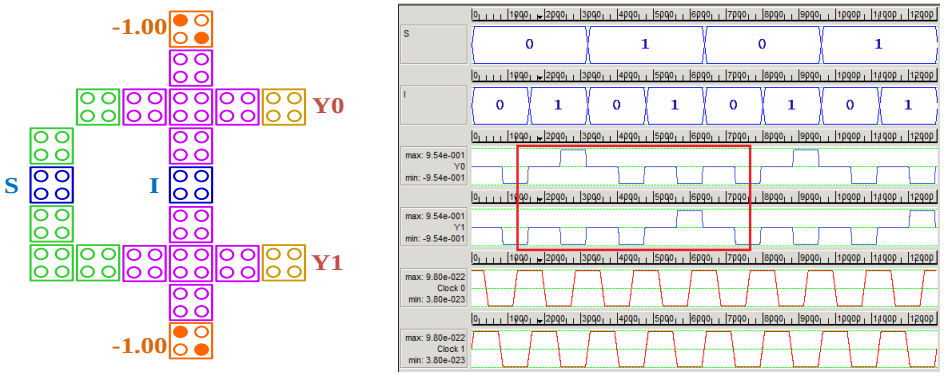


Figure 10. QCA 1:2 Demultiplexer Design with Its Simulated Waveform

4.2.1:4 Demultiplexer

There exist block diagrams and its truth table in Figure 9, Table 2 respectively, where S0 and S1 are select lines for routing the input date to the output lines which are Y0, Y1, Y2, and Y3. In this structure we can see ordering four clocking zones which is carrying out data at the same time without interaction. The main proposed method in this combinational circuit is using less wire-crossing technique to implement compact circuit.

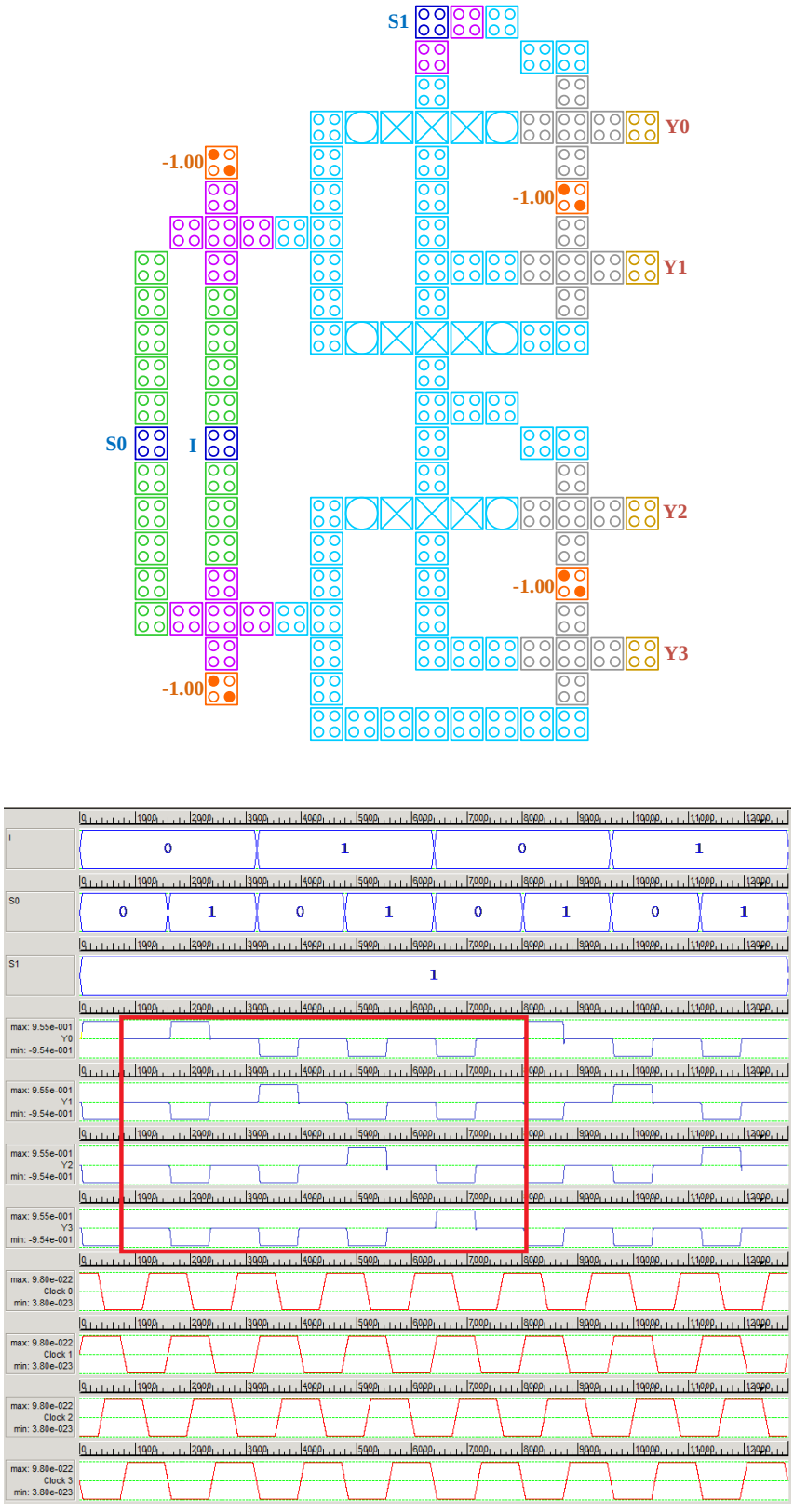


Figure 11. QCA 1:4 Demultiplexer Design with Its Simulated Waveform

5. Comparison and Analysis

In this part, comparison is made to other existing layout of demultiplexer which previous proposed combinational circuits by authors [17] and [18]. We have got simulation result using simulator program QCADesigner which is a design, layout and simulation tool for quantum-dot cellular automata. One of the most important design specifications is that other developers should be able to easily integrate their own utilities into this tool. It is accomplished by providing a standardized method of presenting information within the software [19]. These comparison results were analyzed between two demultiplexer designs and presented 1:2 demultiplexer in Table 3, 1:4 demultiplexer in Table 4. These results indicate the proposed design is denser, consume smaller area and also have lesser complexity. Comparison between both of proposed combinational logic circuits show that presented demultiplexers have significant advantages in terms of area and complexity.

Table 3. Comparison Result of 1:2 Demultiplexer

Structure	Parameters		
	Number of cells	Total Area (nm^2)	Clock
Iqbal *et al*. [17]	27	23,328	2
Ours	21	17,496	2

Table 4. Comparison Result of 1:4 Demultiplexer

Structure	Parameters		
	Number of cells	Total Area (nm^2)	Clock
Luiz *et al.* [18]	181	208,656	8
Ours	140	102,060	4

6. Conclusion

In this paper, we have presented two types of demultiplexer which is used in many integrated device. We have shown that a demultiplexer is simply designed and simulated. Above two tables summarized three important parameters of structures proposed in previous works and this paper. As is shown, our second design uses 140 cells whereas good design proposed in [18], uses 181 cells which means 23 percent improvement. The delay, defined as the clock phases needing to transfer the input signals to the output, and total area of the layout are also reduced until 50 percent. Finally, simulation results of 1:2 and 1:4 demultiplexer show that the proposed demultiplexer achieved significant improvements in QCA circuit as compared to previous design. The proposed designs lead to compact construction and consequently more efficient QCA circuits. These improvements have advantages in terms of low energy consumption, complexity reduction in nanoscale implementation of circuits, and a higher speed.

Acknowledgments

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