

Analysis of Controlling Strategy for Three Level Buck Convertor

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Abstract

In order to make a Three Level Buck DC-DC converter in ideal stable output and better dynamic performance, we design a fast terminal sliding mode controller to control the output voltage. By analyzing and verifying the effectiveness of the algorithm, we offer the time which the system reaches the sliding surface. In order to further improve the dynamic performance, we improved the topology of the traditional Buck Three Level DC converter, by combining the balance principle of capacitance charging, transient controller is designed. The correctness and effectiveness of the theory and the control method is verified by simulation test.

Keywords: *Buck DC-DC converter, terminal sliding mode, dynamic performance, transient controller.*

1. Introduction

Power converter is a vital device for processing and transforming of modern power of in the engineering design. For example, the Buck DC - DC switching converter, which is used as low voltage large current voltage regulator, has been widely applied to the microprocessor in the system. As the power supply system has higher standards for the power quality, it is needed to provide much more stable and accurate power when the power supply is in mobile state. Besides, the dynamic voltage is required to fluctuate in a small range when the power supply is in dynamic state.

Sliding mode control has excellent control performance for the system which is in external disturbance and parameter uncertainty. as a result, there are numbers of research about sliding mode control in switch converter system, and it won the excellent dynamic response [1-3]. while the traditional linear sliding mode surface is converged gradually, the error signal cannot be converged in a limited time. Terminal sliding mode can better solve the problem of effective convergence time, and can obtain faster convergence speed as well as reduce the jitter problem [5].

Three Level Buck DC-DC converters have excellent performance in the occasion of high power. This topology can reduce the voltage stress of switching tube, boost ripple frequency of inductor current, reduce the filter size, and offer much higher efficiency. Therefore, it's appealing in situation with low power [7].

This thesis provides to improve the output voltage of the Buck Multi-Level Inverters DC-DC Convertor with fast terminal sliding mode controller. Through the theoretical analysis and simulation experiment, its superior effectiveness robust performance and dynamic performance is verified. On the basis of the sliding mode control, in order to further improve its dynamic performance, we changed the topology of the traditional Buck Multi-Level Inverters DC-DC Convertor, using the principle of capacitor charge balance analyze and design the transient controller. In conclusion, the correctness and effectiveness of the theory and control method is verified.

2. Space Equation of Three Level Buck Converter

The circuit topology of Three Level Buck Converter is shown in figure 1:

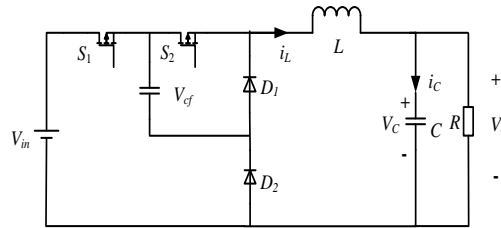


Figure 1. Traditional Topology Structure

Under the condition of continuous inductive current, plus the output voltage is below $v_{in}/2$, the state-space equation of Three Level Buck Converter is shown following:

$$\begin{cases} \dot{i}_L = \frac{v_{in}}{2L}u - \frac{v_o}{L} \\ \dot{v}_o = \frac{i_L}{C} - \frac{v_o}{RC} \end{cases} \quad (1)$$

Where i_L represents the inductive current, v_{in} represents input voltage, L represents inductance, C represents filter capacitor, u controls the input. When u equals 1, it shows that one of the switch tubes, S_1 and S_2 is closed. When u equals 0, it shows that switch tubes S_1 and S_2 are all cut off.

In order to get the voltage controlling value of convertor, we pick up the following state variable:

$$\begin{aligned} x_1 &= v_{ref} - v_o \\ x_2 &= \dot{x}_1 = \frac{v_o}{RC} + \int \left(\frac{v_o}{LC} - \frac{v_{in}}{2LC}u \right) dt \end{aligned} \quad (2)$$

v_{ref} represents the desired value of output voltage, the dynamic equation which is needed in controller design is listed:

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= \frac{-x_2}{RC} + \frac{v_o}{LC} - \frac{v_{in}}{2LC}u \end{aligned} \quad (3)$$

3. The Design of Sliding Mode Controller

3.1. The Design of Sliding Mode Surface

In order to fasten the convergence speed of the system and ensure it can be converged in a limited time, we design a kind of fast nonlinear sliding mode surface on the basis of reference^[5]:

$$S = \dot{x}_1 + \alpha x_1 + \beta |x_1|^p \text{sign}(x_1) + \gamma |x_1|^q \text{sign}(x_1) \quad (4)$$

$\alpha > 0, \beta > 0, \gamma > 0, p > 1, 0 < q < 1$ are the parameters. When the balance point of sliding track force is far away, and $|x_1|$ is larger, the sliding track tends to sliding mode surface at the rate of αx_1 and $\beta |x_1|^p \text{sign}(x_1)$, which increases the approaching speed. When sliding track tends to sliding mode surface, $|x_1|$ closes to zero, the nonlinear term $\beta |x_1|^q \text{sign}(x_1)$ plays a role of control. In the process of reaching, $\beta |x_1|^q \text{sign}(x_1)$ constantly decreases, and eventually stops at the origin.

In order to make sure that state trajectory is near sliding surface, the existing condition is required through the Lyapunov.

$$\lim_{S \rightarrow 0} S\dot{S} < 0 = \begin{cases} S \rightarrow 0^+, \dot{S} < 0 \\ S \rightarrow 0^-, \dot{S} > 0 \end{cases} \quad (5)$$

Two requirements are concluded according to formula (4) and (5):

$$S \rightarrow 0^+, u=1, \dot{S} < 0 \quad \left(\alpha + \beta p |x_1|^{p-1} + \gamma q |x_1|^{q-1} - \frac{1}{RC} \right) x_2 + \frac{v_o}{LC} - \frac{v_{in}}{2LC} < 0$$

$$S \rightarrow 0^-, u=0, \dot{S} > 0 \quad \left(\alpha + \beta p |x_1|^{p-1} + \gamma q |x_1|^{q-1} - \frac{1}{RC} \right) x_2 + \frac{v_o}{LC} > 0 \quad (6)$$

The existing condition of sliding model is shown:

$$0 < \left(\alpha + \beta p |x_1|^{p-1} + \gamma q |x_1|^{q-1} - \frac{1}{RC} \right) x_2 < \frac{v_{in}}{2LC} - \frac{v_o}{LC} \quad (7)$$

3.2. Robustness Analysis

When the system is on the sliding model surface, the equivalent amount of control u_{eq} can be calculated.

$$u_{eq} = \frac{2LC}{v_{in}} \left(\alpha + \beta p |x_1|^{p-1} + \gamma q |x_1|^{q-1} - \frac{1}{RC} \right) x_2 + \frac{2v_o}{v_{in}} \quad (8)$$

While, since the equivalent control cannot make the system get to the balance point in original state at any time, an additional penalty function $u_{sw}=k \text{ sign}(S)$ ($k > 0$) is added. The principle of terminal sliding model control is listed below.

$$u = \frac{2LC}{v_{in}} \left(\alpha + \beta p |x_1|^{p-1} + \gamma q |x_1|^{q-1} - \frac{1}{RC} \right) x_2 + \frac{2v_o}{v_{in}} + k \text{sign}(S) \quad (9)$$

(1) Accessibility

Considering the system disturbance $d(t)$, the formula (3) is changed as following.

$$\dot{x}_2 = \frac{-x_2}{RC} + \frac{v_o}{LC} - \frac{v_{in}}{2LC} u + d(t) \quad (10)$$

Lyapunov is defined as $V = \frac{1}{2} S^2$, thus we can get the result:

$$\dot{V} = S\dot{S} = S \left(\frac{-x_2}{RC} + \frac{v_o}{LC} - \frac{v_{in}}{2LC} u + d(t) + \alpha x_2 + \beta p |x_1|^{p-1} x_2 + \gamma q |x_1|^{q-1} x_2 \right) \quad (11)$$

Combining formula (10) and (11), we can get the following formula.

$$\dot{V} = S\dot{S} = -S \frac{kv_{in}}{2LC} \text{sign}(S) + Sd(t) < 0 \quad (12)$$

The result is fitted for $\frac{kv_{in}}{2LC} > |d(t)|$, $d(t)$ is the uncertain factor resulted from the parameter change in the system. according to formula (12), we can get the conclusion that whether

$S > 0$ or $S < 0$, $\dot{V}(t)$ is always being negative-definite. As a result, the system keeps approaching to be stable under the circumstance of disturbance, which shows that sliding model control has strong ability of anti-disturbance to the perturbation of system parameters.

(2) The limitations of time

When the system gets to the sliding model surface, $S=0$, the formula (4) can be changed as:

$$\dot{x}_1 = -\alpha x_1 - \beta |x_1|^p \text{sign}(x_1) - \gamma |x_1|^q \text{sign}(x_1) \quad (13)$$

Let's resume that under the primitive state, $x_1(0) > 1$, when the system gets to the balance point from $x_1(0)$, there are two main phases. When $x_1(0)$ get to the $x_1(t)=1$, the exponential term $\gamma |x_1|^q \text{sign}(x_1)$ is in low influence which can be ignored. The formula (13) is changed into:

$$\dot{x}_1 = -\alpha x_1 - \beta x_1^p \quad (14)$$

The formula (15) can be calculated according to formula (14):

$$t_1 = \frac{\ln(\alpha + \beta) - \ln[\alpha(x_1(0))^{1-p} + \beta]}{\alpha(p-1)} \quad (15)$$

When the system gets to the balance point from $x_1(t)=1$, the exponential term $\beta |x_1|^p \text{sign}(x_1)$ is in low influence which can be ignored. As a result, formula (13) can be changed into:

$$\dot{x}_1 = -\alpha x_1 - \gamma x_1^q \quad (16)$$

The formula (17) can be calculated according to formula (16):

$$t_2 = \frac{\ln \gamma - \ln(\alpha + \gamma)}{\alpha(q-1)} \quad (17)$$

When calculating the time of each process, the less influenced control terms are ignored. Thus the total time for the system approaching to the balance point from primitive state is listed as follows:

$$t < t_1 + t_2 = \frac{\ln(\alpha + \beta) - \ln[\alpha(x_1(0))^{1-p} + \beta]}{\alpha(p-1)} + \frac{\ln \gamma - \ln[\alpha + \gamma]}{\alpha(q-1)} \quad (18)$$

When the primitive state of system is in $x_1(0) < -1$, the method of derivation for the primitive state, $x_1(0) > 1$ is the same as for the system. Therefore, this sliding model surface can approach to the sliding model surface in limited time.

4. Dynamic Response Improvement

The higher the change rate of inductance current, the faster the speed of energy release and absorption, which means that increase the change rate of inductance current can improve dynamic response of the dc converter^[8]. However, since the change rate of inductance current is limited by the circuit inductance value in the converter and the voltage through the inductance, reducing the inductance value can increase the transformation rate of the inductor current, but also increase the Inductor current ripple and lead to higher consumption in stable period. The change for increasing and decreasing inductor current for traditional Buck tri-level dc converter while at work is listed as following:

$$\begin{aligned} \frac{di_L^+}{dt} &= \frac{0.5v_{in} - v_o}{L} \\ \frac{di_L^-}{dt} &= \frac{-v_o}{L} \quad (19) \end{aligned}$$

As for this, we design a kind of circuit diagram for Buck tri-level dc converter. It is shown in figure 2.

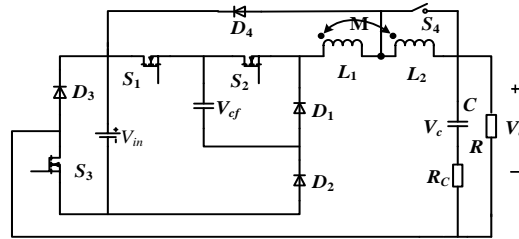


Figure 2. Improved Circuit Topology

Two auxiliary switches S3 and S4, two auxiliary diodes D3 and D4 are added in to the circuit. When the auxiliary switch S3 is closed, with the same circuit structure of traditional three level dc converters, the work and control mode are the same in the steady state period. Under transient conditions, when the load current increases, the auxiliary switch S3 and the main circuit switch is closed, while when the load current reduced, the auxiliary switch S3 and the main circuit switch is disconnected. The change rate of inductor current while increasing and decreasing is:

$$\begin{aligned} \frac{di_L^+}{dt} &= \frac{v_{in} - v_o}{L} \\ \frac{di_L^-}{dt} &= \frac{-v_{in} - v_o}{L} \end{aligned} \quad (20)$$

When the switch S4 is closed and cut off, the calculation formula of output filter inductance is listed as follows:

$$\begin{aligned} L_{on} &= L_1 - \frac{M^2}{L_2} \\ L_{off} &= L_1 + L_2 + 2M \end{aligned} \quad (21)$$

When transient situation occurs, closed switches S4 reduce the output inductor; when transient situation is at the end, disconnecting switches S4, the output inductor point get back to a larger value. Compared with the traditional structure, the change rate of inductance current is improved effectively.

Based on the theory of charging capacitor charge balance theory, we make an analysis to the topological structure in figure 2. When load current increases, the inductor current, capacitance current and the output voltage waveform under the capacitor charge balance control strategy is shown in figure 3. In order to get to the optimal state of satisfying the capacitor charge balance, during the period of the inductor current rising (t_1 - t_2), the primary switch and auxiliary switch need to be in a closed state. During the period of the inductance current declining (t_2 - t_3), primary switch and auxiliary switch needs to be disconnected.

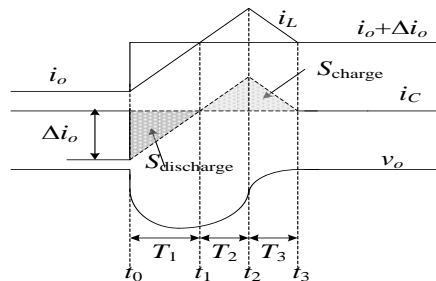


Figure 3. The Optimal Response Waveform Figure While Load Increases

According to figure 3 and formula (20), the expression of the transient capacitance current can be listed as follows:

$$i_c = \begin{cases} -\Delta i_o + \frac{v_{in} - v_o}{L} t, t \in [t_0, t_2] \\ -\Delta i_o + \frac{2v_{in}}{L} t_2 - \frac{v_{in} + v_o}{L} t, t \in [t_2, t_3] \end{cases} \quad (22)$$

As for time t_0 and t_3 , the capacitance current equals 0 ($i_c=0$), formula (23) can be listed according to formula (22).

$$t_1 = \frac{L\Delta i_o}{v_{in} - v_o}, \quad t_2 = \frac{v_{in} + v_o}{2v_{in}} t_3 + \frac{L\Delta i_o}{2v_{in}} \quad (23)$$

In the figure 3, the area of S_{charge} represents capacitance charging quantity, $S_{discharge}$ represents capacitance discharging quantity. Combing the formula (23), we can get the formula (24).

$$\begin{cases} S_{charge} = \frac{L\Delta i_o^2}{2(v_{in} - v_o)} \\ S_{discharge} = \frac{v_{in} + v_o}{4Lv_{in}(v_{in} - v_o)} \left[(v_{in} - v_o)^2 t_3^2 - 2L\Delta i_o(v_{in} - v_o)t_3 + (L\Delta i_o)^2 \right] \end{cases} \quad (24)$$

According to the balance principle of capacitor charge and discharge ($S_{charge}=S_{discharge}$), the static adjustment time t_3 while load current increases can be calculated as:

$$t_3 = \frac{L\Delta i_o}{\sqrt{2v_{in}(v_{in} + v_o)} - (v_{in} + v_o)} \quad (25)$$

Combing formula (24) and (23), the optimal time of switch tube t_2 from close to disconnect in the transient period can be calculated as:

$$t_2 = \frac{L\Delta i_o}{2v_{in} - \sqrt{2v_{in}(v_{in} + v_o)}} \quad (26)$$

When load current increases, the output voltage will decrease. The number of decreasing output voltage can be calculated through formula (27):

$$\Delta v_o = R_C \left(-\Delta i_o + \frac{v_{in} - v_o}{L} t \right) + \frac{1}{C} \int_0^t \left(-\Delta i_o + \frac{v_{in} - v_o}{L} t \right) dt \quad (27)$$

R_C represents parasitic capacitance resistance. Through the derivation calculation of formula (27) and presume it equals to 0, we can get the value point of time. Combing the formula (27), the decreasing number of maximum output voltage while load current increase can be calculated as:

$$\Delta v_o^{\max} = -\Delta i_o R_C - \frac{[CR_C(v_{in} - v_o) - L\Delta i_o]^2}{2LC(v_{in} - v_o)} \quad (28)$$

When load current is lower, the analysis method is same as when the load current is added. The change time of switch state t_4 , static adjustment time t_5 , and maximum output voltage error are:

$$t_4 = \frac{L\Delta i_o}{2v_{in} - \sqrt{2v_{in}(v_{in} - v_o)}} \\ t_5 = \frac{L\Delta i_o}{\sqrt{2v_{in}(v_{in} - v_o)} - (v_{in} - v_o)}$$

$$\Delta v_o^{\max} = -\Delta i_o R_C + \frac{[CR_C(v_{in} + v_o) - L\Delta i_o]^2}{2LC(v_{in} + v_o)} \quad (29)$$

According to formula (25) and (29), when the load changes, the static adjustment time is mainly limited to the variation of inductance and the load current, and changed with the load current variation. Therefore, if the inductance in the transient period is reduced, the static adjustment time can be reduced, which is consistent with the structure theory above.

5. Transient Control Design

According to the figure 3 and formula (22), the integral expression of capacitance discharge can be shown as:

$$S_{discharge} = \int_{t_0}^{t_1} i_C(t) - (-\Delta i_o) dt = \int_{t_0}^{t_1} \left(\frac{v_{in} - v_o}{L} t \right) dt = \iint_{T_1} \frac{v_{in} - v_o}{L} (dt)^2 \quad (30)$$

Capacitance charge quantity can be divided into $S_{charge1}$ and $S_{charge2}$. By combing formula (23), capacitance charge quantity $S_{charge1}$ during the period of T_2 can be shown as:

$$S_{charge1} = \int_{t_1}^{t_2} \left(-\Delta i_o + \frac{v_{in} - v_o}{L} t \right) dt = \iint_{T_2} \frac{v_{in} - v_o}{L} (dt)^2 \quad (31)$$

According to figure 3, we can get the proportional relation between $S_{charge1}$ and $S_{charge2}$. By combing the formula (23), (25) and (26), we get the following formula:

$$\frac{S_{charge2}}{S_{charge1}} = \frac{t_3 - t_2}{t_2 - t_1} = \frac{v_{in} - v_o}{v_{in} + v_o} \quad (32)$$

Concluding the above analysis, we can get the formula of total change quantity:

$$S_{charge} = S_{charge1} + S_{charge2} = \iint_{T_2} \frac{v_{in} - v_o}{L} (dt)^2 + \frac{v_{in} - v_o}{v_{in} + v_o} \iint_{T_2} \frac{v_{in} - v_o}{L} (dt)^2 \quad (33)$$

The relation expression can be acquired according to the capacitor charge balance:

$$S_{charge} - S_{discharge} = \iint_{T_1} \frac{v_{in} - v_o}{L} (dt)^2 - \frac{2v_{in}}{v_{in} + v_o} \iint_{T_2} \frac{v_{in} - v_o}{L} (dt)^2 = 0$$

$$\iint_{T_1} (v_{in} + v_o) (dt)^2 - \iint_{T_2} 2v_{in} (dt)^2 = 0 \quad (34)$$

When the load current decrease, the analysis method is the same as when the load current increases. The relation expression can be listed as:

$$\iint_{T_4} (v_{in} - v_o) (dt)^2 - \iint_{T_5} 2v_{in} (dt)^2 = 0 \quad (35)$$

According to formula (34), we can know that when the load current is increased, by using a double integrator between the period from t_0 to t_1 to integrate $(v_{in} + v_o)$ doubly, integrate $(-2v_{in})$ doubly in the period of t_1 , , we get the conclusion that the time when the value of double integrator close 0 is the time under the principle of capacitor charge balance time t_2 . The output of double integrator output is shown in figure 4. According to this relationship, the time t_2 can be calculated through the two integrator.

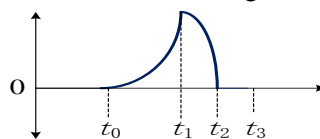


Figure 4. Output of Double Integrator

Capacitive current i_C ripple is small under steady state, the average value is zero. When load current is increased suddenly moment (t_0), capacitive current will decrease to a great extent. Therefore, the design of the lower limit of capacitance current detection threshold $-i_{C-th}$ (its value should be greater than the i_C ripple under steady-state) leads to the resulting time t_0 . The capacitive current is zero in t_1 time, the online threshold is designed as 0, and thus we can obtain t_0 to t_1 moment.

The analysis for output voltage detection is the same as capacitive current. The setting of the threshold value tests the t_0 moment. When the output voltage gets back to the reference voltage output voltage (t_3), we get the t_0 to t_3 moment. When the load current decreases, the analysis method is the same as the above. The final control block diagram is as shown in figure 5.

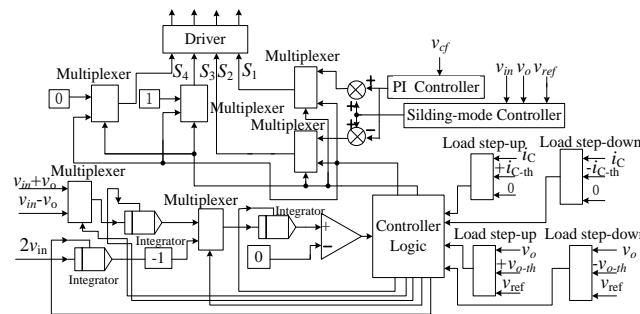


Figure 5. Control Frame Diagram

6. Simulation Test

As for the Buck Three level DC-DC converter, selected parameters are listed as follows: for: reference voltage is 20v, the input voltage 50 v, flying capacitor 60 uF, the output capacitance 60uF. The parameters for the designed terminal sliding mode controller are shown as follows: $k=38.72$, $\beta=8000$, $\gamma=3000$, $p=2$, $q=0.15$. The PI controller is used to effectively control the flying capacitor voltage v_{ref} , its parameters are $k_p=0.73, k_i=0.02$.

Figure 6 and 7 is the simulation comparison of traditional sliding mode control and fast terminal sliding mode control. The figure shows the fast terminal sliding mode control put forwards above can make the output voltage enter into stable state smoothly and quickly at the initial state with no voltage overshoot. When load disturbance appeared, the traditional model control reduces the voltage drop and the overshoot to a certain extent, and shortens the time of the system restoring to the steady state. Besides, since the other traditional sliding mode surface output voltage is affected by the change of the load, it will produce larger steady-state error.

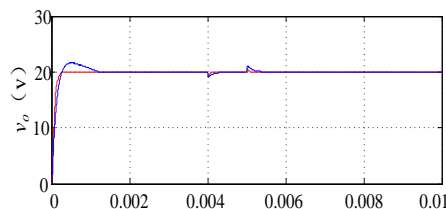


Figure 6. Output Voltage Simulation Image

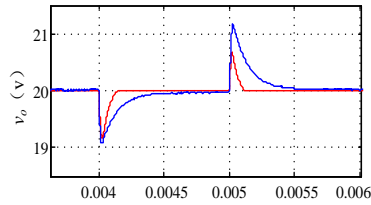


Figure 7. Partial Enlarged Drawing of Figure 6

The curve a in Figures 8 and 9 represents the output voltage under dynamic simulation graph of fast terminal sliding mode control under traditional structure. The transient control based on the capacitance charging balance is added into curve b on the basis of the former. It shows that a better dynamic response can be acquired under the sliding model control through the capacitor charge balance strategy. When the load current decreases, it has less reducing influence on output voltage overshoot. Curve c represents the output voltage of dynamic simulation graph for improving topology after combining the above control method. it can be seen that the voltage overshoot and steady adjustment time is improved to a great extent.

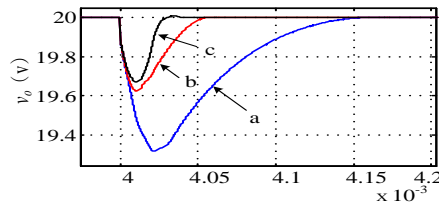


Figure 8. Output Voltage Dynamic Simulation Image with Increase Load

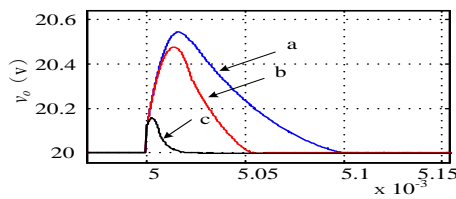


Figure 9. Output Voltage Dynamic Simulation Image with decrease Load

With Buck DC-DC converter circuit topology being improved, under the capacitor charge balance control strategy, the load point mutations in 0.004 seconds and 0.005 seconds. The output of the double integrator is as shown in figure 10. Flying capacitor voltage simulation waveform is shown in figure 11, due to the short period of transient state, it has less influence on the flying capacitor voltage in the transient period, which can quickly return to a stable state (half of the input voltage 25 V).

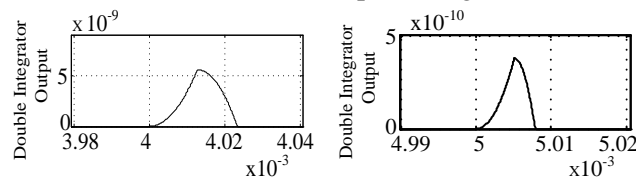


Figure 10. The Output Simulation Image of Double Integrator

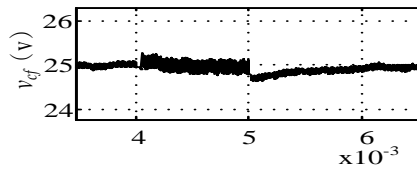


Figure 11. Flying Capacitor Voltage Simulation Image

7. Conclusion

In this thesis, we design a fast double exponential reaching law of sliding mode surface. We proved that the system can approach to the balance point from any point of the sliding surface in a limited time. Compared with the traditional linear sliding mode surface, our design has a faster approaching speed and also can improve the dynamic quality of the system. We offer a improved topology structure of Three level Buck DC-DC converter. A transient control strategy is designed by combining the transient capacitance charging balance. We have proved that this kind of method is featured with faster dynamic response quality by simulation test. It also provides reference meaning for the Multi-level dc transform which is applied in high-power occasion.

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