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# High Performance and High Range Design of 100Gb/s Optical Differential Phase Shift keying Transmitter

M.F.L Abdullah[1], Bhagwan Das[1*], Mohd Shah Nor Shahida[1], Siti Nurul Sharina Mat Yaccob[1], Nurul Nadiah Shamsuddin[1] and Pardeep Kumar[2]

[1]*Universiti Tun Hussein Onn Malaysia (UTHM)*
*Quiad-e-Awam University of Engineering, Science & Technology*
**Corresponding author: engr.bhagwandas@hotmail.com*

***Abstract***

*The need of high performance and high range devices is increasing drastically as rapid growth is accumulating in Information and communication technology (ICT). In Gb/s transmission system high speed optical transmitter requires high power for transmitting information at long distance. The high power transmitters consumes enormous power and exhibits heating effect in devices, leakage power problems as well due to that the device response became slower. In this work, high performance and high range design of 100Gb/s optical DPSK transmitter is designed in 20 nm Field Programming Gate Array (FPGA) using multiple IO standards. The high performance and high range design is achieved using proposed technique by integrating the two IO Standards one is Pseudo Open Drain (POD) and other is Point- to- Point Differential Signaling (PPDS). The POD IO standards is consuming less power feature, while PPDS IO Standard provides the faster response time. It is determined that using proposed technique the 95% power consumption is recorded with 85% improved efficiency in response time for mid-range infrared frequencies such as 200 GHz, 500 GHz, 90 GHz, 5 THz and 20 THz. The designed energy efficient optical transmitter can be assimilate with further optical components in optical communication systems to high performance and high range future generation networks.*

***Keywords****: Differential Phase Shift Keying; Optical transmitter; Field Programming Gate Array; IO Standard; Power consumption; Response time*

## 1. Introduction

In optical communication systems, exchange of information is initiated by transmitting high power signal using optical transmitter [1]. Optical transmitter consist data signal to be transmitted, electrical signal generator to generate the equivalent signal for data signal, laser signal as a carrier and modulator to combine the electrical data signal and laser signal. Optical transmitter are designed mainly using external modulation or direct modulation [1]. However, in transmission rate of more than Gb/s transmission system, the first choice of optical modulation is preferred [1]. Optical transmitter designed using external modulation use electrical sequence, laser signal and modulator to produce optical signal for electrical signal [1] using modulation schemes such as; Non-Return-to-Zero (NRZ) and Return-to-Zero (RZ), On-Off Keying (OOK) schemes with modulation formats *i.e.* amplitude, (OOK) or phase format, Phase Sift keying (PSK) [1]. From these modulation schemes the PSK format with NRZ scheme is widely used due to, its resilience to noise nature at 3 dB sensitivity of receiver [1]. There is plenty of research is ongoing for designing optical transmitter, which generates high power signal for high speed and long haul transmission at low power consumption with high performance and high range output and till now, in real this goal is achieved somehow [1]. The term high

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performance represents, the minimum power consumption at high frequency input. The term high range means high device can quickly respond means response time. But high performance and high range design of optical transmitter is still struggling with high power consumption challenges, when producing Gb/s data rate at frequencies more than 10 GHz at different modulation formats [2] with slow response time. There are several techniques have been reported high performance and high ranges devices *e.g.* by compensating CD in frequcny domain [3-4], optimizing optical modulation amplitude [5], green routing [5], IP forwarding [5], energy efficient network access [5], high-speed current controllers [5], sleep mode techniques and others [5]. Through these techniques power reduction can be achieved for only few GHz operating frequency and at Gb/s data rate [6]. Nevertheless, more than this frequency range, some other techniques need to be developed for reducing optical transmitter power. Various energy efficient systems are acknowledged that are designed using Very Large Scale Integration (VLSI) in FPGA chip [7]. For instance, 100Gb/s Ethernet systems [7], power optimization of pseudo noise based optical transmitter [8]. These system are utilizing different power reduction techniques such as; clock gating [9], voltage scaling [9], variable frequency [9]. Moreover, variable power supply [9], multiplied threshold [9], chip reduction and packaging size [9], design improving techniques [9], power management techniques [9] and others in [9]. Recently, using IO Standard available on different FPGA devices are widely utilized to reduce power consumption and provides high range of frequency operation for different devices [10], [11]. To the best of this study still the high performance and high range design of Gb/s transmission optical transmitter design are not reported at operating frequency of more than 40 GHz.

In this work, high performance and high range design of 100Gb/s optical DPSK transmitter is demonstrated using Field Programming Gate Array (FPGA) multiple IO Standards concept. 100Gb/s optical DPSK transmitter is realized using proposed multiple IO Standards available on UltraScale FPGA device.

## 2. High Performance and High Range Design of 100Gb/s Optical DPSK Transmitter

The research design flow of high performance and high range design of 100 Gb/s Optical DPSK transmitter is described in Figure 1. In first design stage, 100 Gb/s optical transmitter is designed in FPGA using vhdl language along with Register Transfer Logic (RTL) schematic design of designed optical transmitter using Xilinx Suite 14.7.

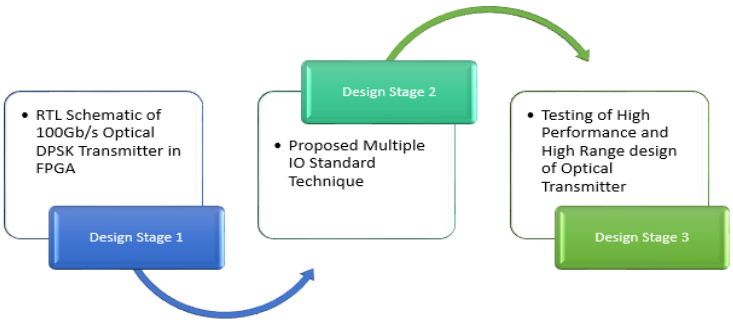


**Figure 1. Research Flow Deign of Proposed High Performance and High Range Design 100Gb/S Optical DPSK Transmitter**

In second design stage, the designed optical transmitter is realized using proposed multiple IO Standard that will produce high performance and high range design for optical transmitter. In third design stage, the high performance and high range design of optical transmitter is tested over different high mid-infrared frequencies such as; 200

 

GHz, 500 GHz, 5 THz and 20 THz for investigation of high performance and high range design of optical transmitter.

## 3. RTL Schematic of 100Gb/s Optical DPSK Transmitter in Xilinx

100Gb/s optical DPSK transmitter is modeled using external modulation scheme. Optical transmitter is designed by defining the 100Gb/s Pseudo Random Binary Sequences (PRBS), Fabry-Perot laser diode and NRZ modulator. The output of 100Gb/s electrical signal and laser signal is modulated together using NRZ modulation. Figure 2 describes model for 100Gb/s optical DPSK transmitter.

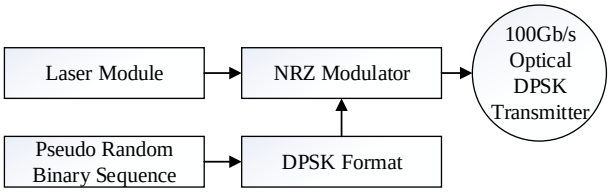


**Figure 2. 100Gb/s Optical DPSK Transmitter Model**

RTL schematic is developed for 100 Gb/s optical DPSK modulator. The top view of designed 100Gb/s optical DPSK transmitter of RTL schematic in FPGA is shown in Figure 3.

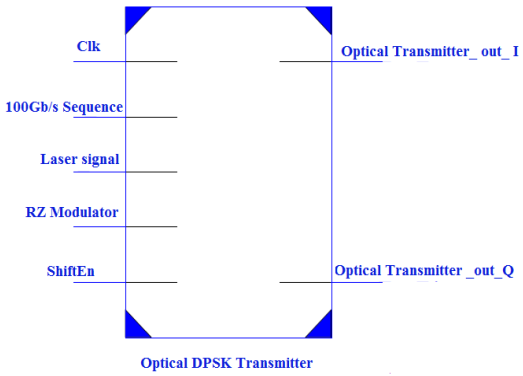


**Figure 3. 100Gb/s Optical DPSK Transmitter RTL Schematic Top View**

RTL schematic diagram of 100Gb/s optical DPSK transmitter consist five inputs Clk pulse of 500 MHz; 100Gb/s DPSK signal as generated; laser signal generated; NRZ modulated signal generated; shiftEn pulse of enabling and disabling the modulation operation. The FPGA design of 100Gb/s optical DPSK transmitter has two outputs; one is amplitude signal optical transmitter_output_I and other is quadrature signal optical transmitter_output_Q. However, both signal can be combined to produce unified 100Gb/s optical DPSK signal. The inside layout of RTL diagram as described in Figure 4 is very complicated and composed of several components that includes input output buffer, shift registers and memory blocks due to complexity the diagram may not visible clearly. In next stage, proposed multiple IO Standard technique is applied to reduce the power consumption for target device.

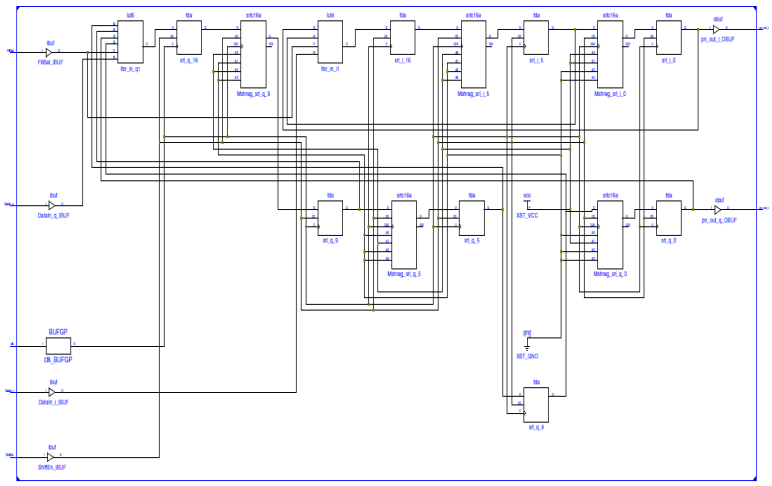

**Figure 4. Complete RTL Schematic of 100Gb/s Optical DPSK Transmitter**

## 4. Apply Proposed IO Standard Technique for High Performance and High Range Operation of FPGA Based 100Gb/S Optical DPSK Transmitter

In this work, 100Gb/s optical DPSK transmitter is operated at multiple IO Standards. These IO Standards are available on FPGA are categorized to achieve high performance and high range design for the target device [13]. There are several IO Standard are available for target device each IO standard is to be selected for different applications that depends upon the device requirement. In this work, major focus is on high performance and high range in terms of power and response time. In this work, we have utilized two IO Standards to overcome power and response time issues. Pseudo Open Drain (POD) standards are proposed for high performance applications because it utilize the high memory RAM interface for designed application [12]. These memories includes DDR4, DDR4L, and LLDRAM3, that can provide high performance application for wide range of frequency [13]. The POD IO standard can be used by varying the VREF available on FPGA [13]. Due to high impedance in POD IO standards the power consumption of the target is extremely high and cannot provide high ranges for operating the target device at high frequencies [13]. There are other IO Standard that are compatible with POD IO standard to increase the high range for high performance IO Standards. These high range IO standards are Point-to-Point Differential Signaling (PPDS) IO Standards. PPDS inputs require a parallel-termination resistor, either through the use of a discrete resistor on the PCB, or by using logical attributes of FPGA to enable internal termination [13]. In this work, the POD and PPDS IO Standards are used integratedly to design the high performance and high range optical transmitter. The high performance and high range designed optical transmitter consumes less power and produce fast response time than others. In this work, the device performance is also compared with and without proposed IO standards. We have determined that the proposed design is significantly reducing the power consumption and improving the response time of the optical transmitter. The following script of program is used to configure the multiple IO attributes for 100Gb/s optical DPSK transmitter.

```
INST <I/O_BUFFER_INSTANTIATION_NAME> POD IO STANDARD="<10>";
INST <I/O_BUFFER_INSTANTIATION_NAME> PPDS IO STANDARD="<10>";
INST <I/O_BUFFER_INSTANTIATION_NAME> IBUF_LOW_PWR=[TRUE|FALSE];
INST <I/O_BUFFER_INSTANTIATION_NAME> SLEW = "<SLEW_VALUE>";
```

 

## 5. Testing of Designed High Performance and High Range Design of Optical Transmitter With and Without Proposed IO Standards

The designed 100Gb/s optical DPSK transmitter is tested over different mid-range infrared frequencies such as 200 GHz, 500 GHz, 900 GHz, 5 THz, 10 THz and 20 THz. The designed is tested with and without proposed technique.

### 5.1. Testing of 100Gb/s Optical DPSK Transmitter Performance at 200 GHZ

100Gb/s optical DPSK transmitter is operated at 200 GHz using default design implemented on FPGA and proposed design using multiple IO Standards. It is determined that using proposed design high performance and high range design of 100Gb/s optical DPSK transmitter is consuming less power and providing faster response than non-proposed design of optical transmitter. Table 1 describes the performance analysis of optical DPSK transmitter using with and without proposed technique.

**Table 1. Performance Analysis of 100Gb/S Optical DPSK Transmitter With and Without Proposed IO Standard Technique At 200 Ghz**

| Parameters for Analysis | Without Proposed design | With proposed design |
|---|---|---|
| Power Consumption | 4.2 W | 0.1 W |
| Reponses time | 7.2 μs | 2 μs |

It is noticed that proposed design consuming 97% less power and also provides the 72% faster response time than contrary. The proposed technique is consuming is very less power and provides faster response due to the characteristic of combining two IO standard. POD IO standard falls in high performance IO bank that has several fast low power memory interconnection and low impedance termination as compared any other IO standards such as LVCMOS, LVTTL, HSTL and others. PPDS IO standard is fastest signaling IO standards that provides the fast point to point signaling with low power consumption than other IO standard such as LVDS and RSDS IO Standards.

### 5.2. Testing of 100Gb/s Optical DPSK Transmitter Performance at 500 GHZ

100Gb/s optical DPSK transmitter is tested at 500 GHz using with and without proposed IO Standard technique. It is extracted that using proposed IO standard based design of 100Gb/s optical DPSK transmitter is consuming 95% less power and providing 77% faster response than non-proposed design of optical transmitter as shown in Table 2.

**Table 2. Performance Analysis of 100Gb/S Optical DPSK Transmitter With and Without Proposed IO Standard Technique at 500 Ghz**

| Parameters for Analysis | Without Proposed design | With proposed design |
|---|---|---|
| Power Consumption | 6.2 W | 0.3 W |
| Reponses time | 10 μs | 2.3 μs |

### 5.3. Testing of 100Gb/s Optical DPSK Transmitter Performance at 900 GHZ

When 100Gb/s optical DPSK transmitter is verified at 900 GHz, it is analyzed that 95% power consumption is reduced with improvement of 84% response time in comparison with and without proposed technique for 100Gb/s optical transmitter as described in Table 3.

**Table 3. Performance Analysis of 100Gb/s Optical DPSK Transmitter With and Without Proposed IO Standard Technique at 900 Ghz**

| Parameters for Analysis | Without Proposed design | With proposed design |
|---|---|---|
| Power Consumption | 8.2 W | 0.4 W |
| Reponses time | 17 μs | 2.7 μs |

### 5.4. Testing of 100Gb/s Optical DPSK Transmitter Performance at 5 THZ

100Gb/s optical DPSK transmitter is tested at 5 THz using with and without proposed IO Standard technique. It is extracted that using proposed design consumes 95% less power and provides the 86% faster response time as shown in Table 4.

**Table 4. Performance Analysis of 100Gb/s Optical DPSK Transmitter With and Without Proposed IO Standard Technique at 5 Thz**

| Parameters for Analysis | Without Proposed design | With proposed design |
|---|---|---|
| Power Consumption | 11.3 W | 0.6 W |
| Reponses time | 22 μs | 2.9 μs |

### 5.5. Testing of 100Gb/s Optical DPSK Transmitter Performance at 20 THZ

It is analyzed that when 100Gb/s optical DPSK transmitter is tested at 20 THz, the 95% power consumption is reduced and 90% faster response is achieved using proposed technique as mentioned in Table 5.

**Table 5. Performance Analysis of 100Gb/s Optical DPSK Transmitter With and Without Proposed IO Standard Technique at 20 Thz**

| Parameters for Analysis | Without Proposed design | With proposed design |
|---|---|---|
| Power Consumption | 20.1 W | 1.05 W |
| Reponses time | 36.3 μs | 3.46 μs |

## 6. Results and Discussion

The proposed high performance and high range design of 100Gb/s optical transmitter is designed proposed IO Standard technique. It is determined that the proposed technique is significantly reducing the power consumption and provides the faster response time for all mid-range infra-red frequencies. In the proposed technique is designed by combing the two IO Standards. The two IO standards are POD and PPDS. The characteristics of combining the both IO Standards is giving and advantage to produce low power consumption output and faster response time for 100Gb/s optical DPSK transmitter.

Figure 5 describes the high performance analysis for with and without using proposed technique. It is observed that using proposed technique the 100Gb/s optical transmitter is considered as high performance design that consumes very minimum power for all infra-red frequency ranges. Figure 6 illustrates the high range analysis in terms of response for 100Gb/s optical DSPK transmitter. It is defined that proposed design of optical transmitter has very fast response for all input frequency ranges.

 

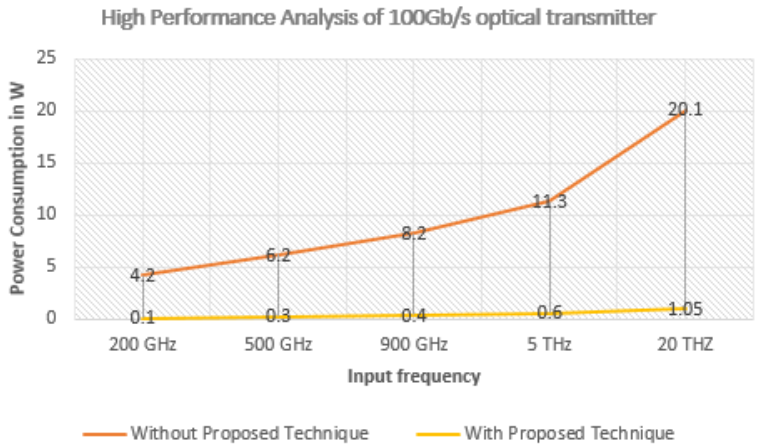


**Figure 5. High Performance Analysis Of 100Gb/s Optical Transmitter Suing With and Without Proposed Technique**

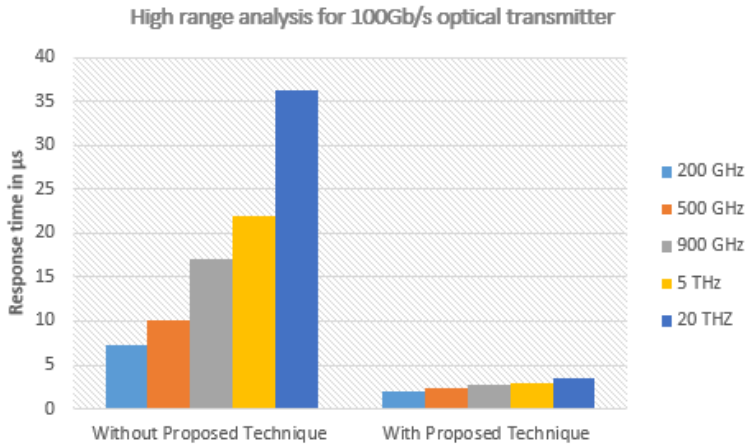


**Figure 6. High Range Analysis of 100Gb/S Optical Transmitter Suing With and Without Proposed Technique**

## 7. Conclusion

In this work, high performance and high range design of 100Gb/s optical DPSK transmitter is proposed using integrating the two IO Standards such as POD and PPDS. It is determined that the propose technique is efficiently producing the high performance and high range design of 100Gb/s optical DPSK transmitter. It is concluded that significant power reduction is achieved using proposed design for 100Gb/s optical DPSK transmitter along with faster response time for mid-range infrared frequencies. Using the proposed design almost 95% power is saved and averagely more than 85% response time is improved. The proposed design of 100Gb/s optical DPSK transmitter is producing the high performance and high range energy output. The proposed design is consuming very nominal power at mid-infrared frequency range (30 GHz to 30 THz) and produce high range output for mentioned operating frequency. It is also determined that the power consumption of proposed design is also very less as compared to traditional devices mentioned in []. The designed optical transmitter can be integrate with components in existing optical communication to produce high performance and high range output for the future generation networks.

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