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SSTL I/O Based Current Optimized Thermal Energy Efficient ROM Design on 28nm FPGA

Kashish Bansal[1], Itanshu[2], Sabia Chawla[3], Simran bhalla[4] and Tanmeet Kaur[5]

[1-5]Gyancity Research Lab, Gurgaon, India
[1]kashishbansal2719@gmail.com, [2]itanshuahuja@gmail.com,
[3]sabiachawla95@gmail.com,
[4]simranbhalla1996@gmail.com, [5]tanu.has12@gmail.com

Abstract

In this work, energy efficient ROM is being designed using Kintex 7 which is able to scale down the circuit to 28 nm. For Testing the ROM compatibility, ROM is operated on operating frequencies (10GHz, 15GHz, 20GHz, 25GHz) .Whenever capacitance is scaled down from 15pf to 5pf, there is I/O power and total power reduction but it is observed that there is no reduction in Clock power, and a very small reduction in leakage power. FPGA is an Integrated Circuit that comprises of input/output buffer, programmable interconnect structure and an array of configurable logic blocks, which featurisms fast prototyping and consumer configurability which gives the advantage of short turnaround time(i.e. time required from start of process till a functional chip is obtained).10MBits of on chip Memory is being provided on Xilinx FPGA in 36Kbits blocks, which supports dual port operation. Stub Series Terminated Logic (SSTL) is an Input/output standard which is selected because it avoids the transmission lie reflection and overall power dissipation. The purpose of Voltage scaling is to reduce leakage power. When capacitance of output load is scaled from 50pF to 5pF, there are 32-37% saving in I/O Power, 0-0.1% Leakage Power saving, there will be a 1-5% saving in Total Power. This design is implemented on Kintex-7 FPGA using Xilinx ISE & Verilog. The technique of Frequency Scaling has been used to reduce the leakage power consumption within the range of 80% to 44.8%, consumption in total power in range of 45.8% to 21.36% and the reduction in Junction temperature range is from 3.5% to 1.6% for 10GHz frequency.

Keywords*: Low Power;Frequency Optimization; Capacitance Optimization; Power Optimization; Field Programmable Gate Array,RTL*

1. Introduction

The purpose of ROM is to store the definitions pertained to the execution ability of opcodes. The energy efficient ROM is used to store the addresses permanently. When the power of ROM is removed then data does not get lost (non volatile). In a ROM design we have SSTL code of 32 bits and performed various synthesizing Operations. In this work Optimization of Frequency and Capacitance is done in ROM design to save power and junction temperature .Kintex-7 is favorable because it has high end fabric and interface speeds and it has high signal processing ratios. Energy Efficient SSTL I/O standard is selected among different varieties of SSTL logic families in FPGA which plays a vital role in achieving efficiency of energy in design under test. Here DUT is ROM, which is a integral part of processor. In the present paper ROM is being optimized by frequency and capacitance scaling. Frequency Scaling is a technique in which total power consumption change is being analyzed at different frequencies so as to achieve performance gains

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whereas capacitance scaling is the technique which is being used for energy saving(*i.e.* lesser power consumption for DAC) and power optimization for pipeline A to D.

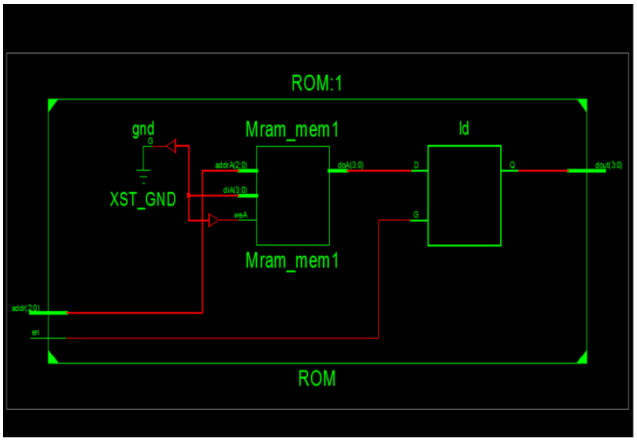

Figure 1. Rtl Rom Design

High level representation of ROM is created in hardware description language(HDL) so that the lower level represntation and actual wiring can be derived from the digital circuit design.This RTL is generated .

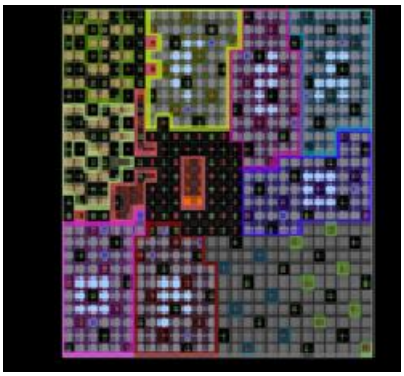

Figure 2. Package Design of ROM

2. Literature Review

In this paper we are going to discuss the energy efficiency of ROM through SSTL I/O based current optimization technique. [1] Effectiveness of 28 nm based FPGA technology is compared to Artix-7 40nm FPGA, which is being analyzed by voltage optimization, hence voltage and frequency scaling on Image ALU is applied for power reduction on 28nm technology. In [2], Design of Energy Efficient Image Inverter is analyzed by capacitive and frequency scaling. Paper [3] is written upon virtuosity of FIR filter whose designing is done using 28nm Kintex-7. Paper [4] describes the voltage calibration of FPGAs used commercially. In [5] Voltage Optimization is performed on 28nm FPGA for the purpose of ALU Designing. Paper [6] is upon vile check plan of ROM and present work also tells the mean control design of ROM. In [7] this book, analysis of various programmable arrays are being discussed. In paper [8] thermal energy efficiency is being examined by frequency and voltage scaling. Paper [9] is based on the capacitive scaling of output load in low Power RAM Design. Paper [10] is based on usage of switching standard implemented in CMOS transistors. In paper [11], Energy efficient memory circuit on 28nm FPGA is being designed and the dependency of the circuit on different

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LVCMOS standards is discussed. In paper [12] 3 different ROM topologies are investigated & compared for ultra-low voltage operation. In [13] the internal programming of FPGA is being discussed. Paper [14] tells the reduction of static power and 50% increase in performance over previous FPGA's and the management of dynamic power. Paper [15] gives the idea of thermal awareness and reduction in various parameters if we change the airflows which are measured in linear feet per minute.

3. Results of Frequency Scaling

Reduction in effective & total power dissipation and junction temperature of target design.ALU is operated with different frequencies of 10GHz, 15GHz, 20GHz, and 25GHz.

A. ROM Operating Frequency is 10GHz

Table 1. Operating Frequency is 10GHz on 28nm FPGA

F=10Ghz C = 5pf				
V	**Lp**	**JT**	**Qc**	**Qp**
1.8	0.352	28	0.184	0.372
1.6	0.198	27.6	0.11	0.299
1.4	0.015	27.3	0.067	0.253
1.2	0.071	27.2	0.041	0.229

With 1GHz operating frequency, there is 88.9%,81.9%,68.9% and 44.8% reduction in Leakage power, 46.8%,41.81%,33.99% and 21.36% reduction in Total Power, 4.982%,4.626%,3.558% and 2.13% reduction in Junction Temprature,when Voltage ranges from 1.8V-1.2V with step size of 0.2V.

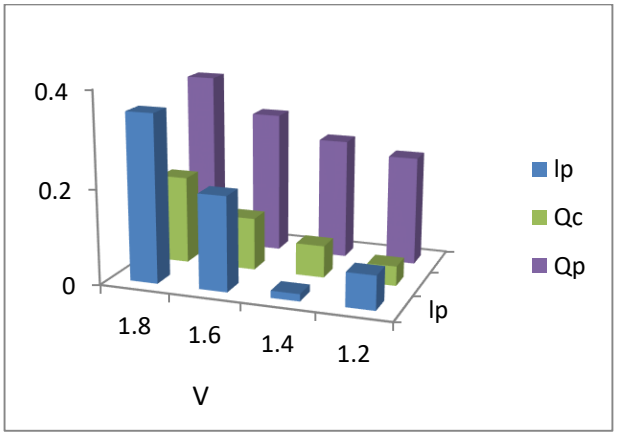

Figure 3. Quiescent Power and Leakage Power at F = 10GHz

B. ROM Operating Frequency is 15GHz

Table 2. Operating Frequency is 15GHz on 28nm FPGA

F=15GHz,C=5pf				
V	**LP**	**JT**	**Qc**	**Qp**
1.8	0.366	29	0.192	0.38
1.6	0.205	28.5	0.115	0.303
1.4	0.119	28.2	0.069	0.257
1.2	0.072	28	0.042	0.23

When 15 GHz is operating frequency and FPGA is 28nm, there is 90.4%,83.5%, 70.78% and 46.3% reduction in leakage power, 23.85%,20.5%,16.0% and 9.72%, reduction in total power, and 8.31%, 7.27%,5.71% and 3.37%, reduction in junction temperature when Voltage ranges from 1.8V-1.2V with step size of 0.2V.

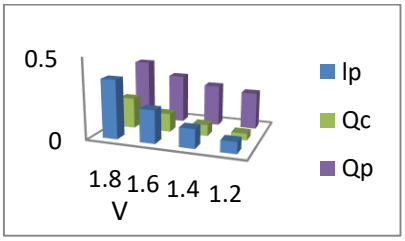

Figure 4. Quiescent Power and Leakage Power at F = 15GHz

C. ROM Operating Frequency is 20 GHz

Table 3. Operating Frequency is 20GHz on 28nm FPGA

F=20GHz,C=5pf				
V	**LP**	**JT**	**Qc**	**Qp**
1.8	0.38	29.9	0.199	0.388
1.6	0.212	29.5	0.119	0.307
1.4	0.122	29.1	0.072	0.26
1.2	0.074	28.9	0.043	0.232

On 15 GHz operating frequency, there is 92.4%, 86.1%, 73.6% and 49.1% reduction in leakage power, 19.99%, 17.38%, 13.8% and 8.58% reduction in total power and 11.89%, 10.28%, 8.19% and 5.78%, reduction in junction temperature when Voltage ranges from 1.8V-1.2V with step size of 0.2V.

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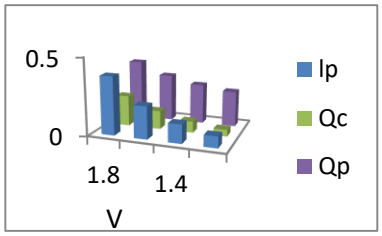

Figure 5. Quiescent Power and Leakage Power at F = 20GHz

D. ROM Operating Frequency is 25 GHz

Table 4. Operating Frequency is 25GHz on 28nm FPGA

F=25GHz C = 5pf				
V	**LP**	**JT**	**Qc**	**Qp**
1.8	0.395	30.9	0.207	0.395
1.6	0.22	30.4	0.124	0.312
1.4	0.126	30	0.074	0.263
1.2	0.076	29.8	0.045	0.233

When ROM operate with 25 GHz frequency on 28nm FPGA, there is 93.98%, 88.35%, 76.94% and 53.19%, reduction in leakage power, 24.5%, 21.9%, 18.1% and 11.8% reduction in total power and 17.7%, 15.8%, 13.1% and 8.6% reduction in junction temperature when Voltage ranges from 1.8V-1.2V with step size of 0.2V.

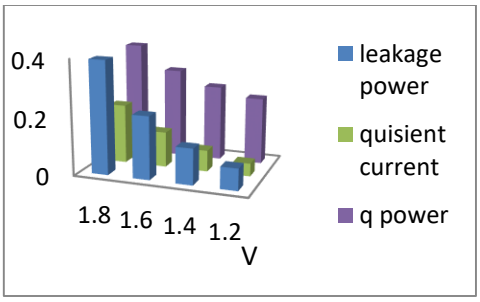

Figure 6. Quiescent Power and Leakage Power at F = 25GHz

E. Junction Temperature for Frequency Scaling

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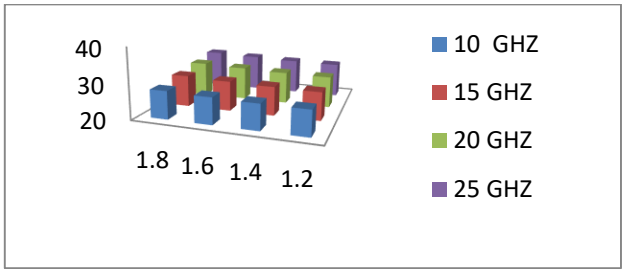

Figure 7. Junction Temperature of all four frequencies

4. Capacitive Scaling

A. ROM Operating capacitance is 5pF

Table 5. Operating Capacitance is 5pF on 28nm FPGA

C = 5pf F=10Ghz				
Voltage	**LP**	**JT**	**Qc**	**Qp**
1.8	0.352	28	0.184	0.372
1.6	0.198	27.6	0.11	0.299
1.4	0.115	27.3	0.067	0.255
1.2	0.071	27.2	0.041	0.229

When ROM operates at 2 volts, there is total of 43.75%,67.32%,79.82% reduction of leakage power, 19.62%,31.45%,38.44% reduction of total power and 1.42%,2.5%,2.8% reduction of junction temperature as shown in Table 5 and Figure 8.

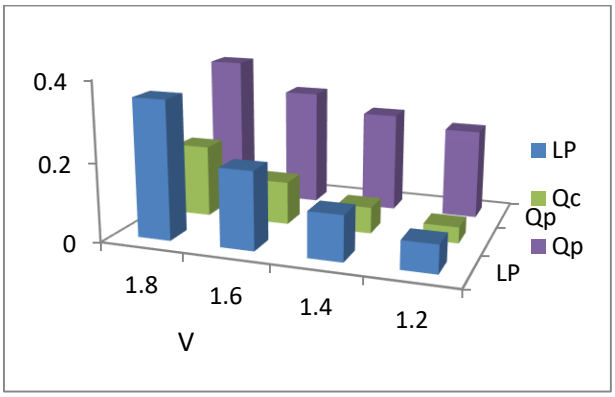

Figure 8. Quiescent Power and Leakage Power at C=5pf

B. ROM Operating capacitance is15pf.

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Table 6. Operating Capacitance is 15pf on 28nm FPGA

C=15pf,F=10Ghz				
V	**LP**	**JT**	**QC**	**Qp**
1.8	0.36	28.3	0.19	0.4
1.6	0.2	27.9	0.11	0.3
1.4	0.12	27.6	0.07	0.3
1.2	0.07	27.2	0.04	0.2

When ROM operates at 1.8 volts, there is total of 43.82%, 67.41%, 82.5% reduction of leakage power, 38.71%, 31.55% reduction of total power and 1.41%, 2.47%, 3.88% reduction of junction temperature as shown in Table 6 and Figure 9.

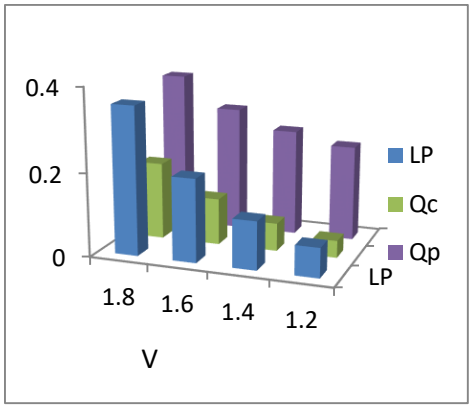

Figure 9. Quiescent Power and Leakage Power at 15pf

C. ROM Operating Capacitance is 20 picofarads..

Table 7. Operating Capacitance is 20pfs on 28nm FPGA

C=20pf F=10Ghz				
V	**LP**	**JT**	**Qc**	**Qp**
1.8	0.358	28.4	0.187	0.372
1.6	0.201	28	0.112	0.3
1.4	0.117	27.8	0.068	0.256
1.2	0.072	27.6	0.041	0.229

When ROM operates at 1.6 volts , there is total of 43.85%,67.31%,79.88% reduction of leakage power, 40.10%,63.63%,78.07% reduction of total power and 19.35% , 31.18%, 38.44% reduction of junction temperature as shown in Table 7 and Figure 10.

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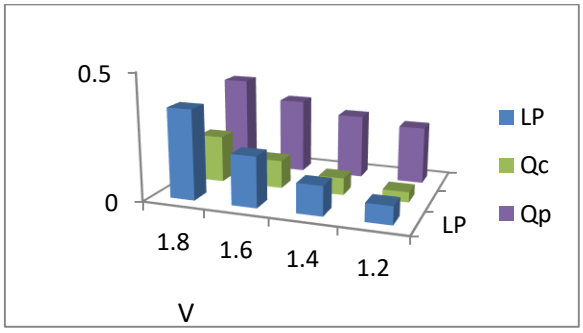

Figure 10. Quisient Power and Leakage Power at Capacitance 20pfs

D. ROM Operating Capacitance is 50picofarads

Table 8. Operating Capacitance is 50pf on 28nm FPGA

C=50pf F=10GHz				
V	**LP**	**JT**	**Qc**	**Qp**
1.8	0.37	29.2	0.194	0.382
1.6	0.207	28.8	0.116	0.304
1.4	0.12	27.8	0.068	0.256
1.2	0.073	28.4	0.043	0.231

When ALU operates at frequency = 10GHz, there is total of 44.05%,67.56% and 80.27% reduction of leakage power, 20.41%,32.98%,33.56% reduction of total power and 3.42%,4.79% reduction of junction temperature as shown in Table 8 and Figure 11.

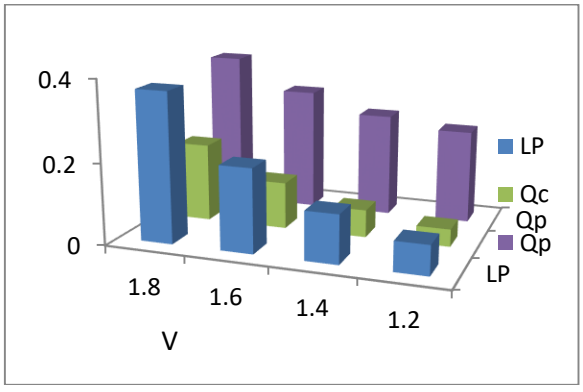

Figure 11. Quiescent Power and Leakage Power at C = 50

Junction Temperature For Capacitive Scaling

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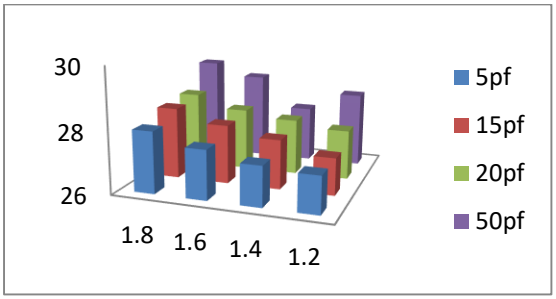

Figure 12. Junction Temperature of all four frequencies

5. Conclusion

28nm Technology based FPGA is power and energy aware FPGA. With Frequency scaling, as the frequency decreases from 25GHz to 10GHz, the reduction in leakage power is 79.82% at 10GHZ, 80.3% at 15GHZ, 80.5% at 20GHZ and 80.8% at 25GHZ. Similarly, the reduction in junction temperature is, 4.982% at 10 GHz, 8.31% at 15 GHz, 11.89% at 20 GHz and 17.7% at 25 GHz.

With Capacitive Scaling, as the voltage decreases from 1.8 Volts to 1.2 Volts the reduction in leakage power is 79.82% at 5pf, 82.5% at 15pf, 79.88% at 20pf, 80.27% at 50pf.Similarly the reduction in junction temperature is 2.8% at 5pf, 3.88% at 15pf, 4.9% at 50pf .

6. Future Scope

In future, it can be designed on 64 bit ROM which will be more thermal efficient and the basic elemental characteristics will be more optimized such as capacitance, frequency then there will be wide scope to reimplement said work on 16nm and 7nm depending on the availability of Future FPGA

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Authors

Kashish Bansal, he is pursuing B.E. in ELECTRONICS AND COMMUNICATION from Chiktkara University, rajpura and is currently in 5th semester.

Simran Bhalla, she was born at Amritsar, Punjab in India and is pursuing B.E. in ELECTRONICS AND COMMUNICATION from Chitkara University, rajpura. She is currently in her 3rd semester and an active member of IETE. The areas of her interest are semiconductor physics along with digital circuits.

Tanmeet kaur, she was born in town named Banur,Punjab and is pursuing B.E. in ELECTRONICS AND COMMUNICATION from Chitkara University, rajpura. She is an active member of IETE and in 3rd semester of her degree. The areas of her interest are semiconductor physics along with digital circuits.

Sabia Chawla, she is pursuing B.E. in ELECTRONICS AND COMMUNICATION from Chiktkara University, rajpura is currently in 5th semester.

Itanshu Ahuja is pursuing B.E. in ELECTRONICS AND COMMUNICATION from Chiktkara University, rajpura is currently in 5th semester.

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