International Journal of Control and Automation
Vol. 8, No. 9 (2015), pp. 291-302
http://dx.doi.org/10.14257/ijca.2015.8.9.28

Design of Acoustic Emission Data Acquisition System of Wood Damage

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Abstract

The acoustic emission (AE) signal of wood damage is a kind of weak and high-frequency signal. Hardware circuit design and software programming are necessary for the acoustic emission data acquisition. In order to carry out further analysis, it needs to be preprocessed. The preprocessing hardware system consists of preamplifier, filtering circuit, main amplification circuit and AD converting circuit. FPGA is considered as the main controller of the entire system in order to gather signals at a high speed. Data from AD convertor are written into FIFO (First In First Out) which is designed in FPGA in advance. Therefore, data can be kept in cache instead of losing them. Meanwhile, wireless transmission is applied to the system for distant detection. To sum up, the entire system can achieve the goal of distant detection of wood damage by gathering the acoustic emission signal whose frequency is from 100KHz to 300KHz and transmitting the processed data at a rate of 1MHz with wireless transmission module.

Keywords: *Wood damage, Acoustic emission signal, Amplification, Filtering*

1. Introduction

The acoustic emission of the wood damage is the sign of the rupture of the wood structure, which can identify the damage degree of the wood structure. It is one of the latest dynamic nondestructive inspections. The damage mode can be identified with the parameters of wood damage. In that way, the related departments can take some protective measures. The paper is based on the acoustic emission signals. And the acoustic emission data acquisition system is composed of hardware design and software design.

2. Proposal of the Entire Design of Acquisition System

In the acoustic emission signals acquisition system of the wood damage, the acoustic emission sensors are installed on the surface of the wood to gather AE signals. Then the signals are processed by pre-amplifier, filter, main amplifier and AD converter, and conveyed to the FPGA system. The data from the signals can be caught by FIFO registers. Finally, the wireless transmission module conveys signals to upper machines. The flow chart of the acquisition system is given in Figure 1.

3. Design of the Hardware Circuit Main Title

3.1. Acoustic Emission Sensors (AE sensors)

The frequency of the AE signals is related to the specific features of the materials. It ranges from infrasonic wave and ultrasonic wave, which can only be detected by particular sensors [1]. This research focuses on AE signals of wood damage. According to other reference documentation, the frequency bandwidth of this AE signal ranges from 100KHz to 300KHz. In that case, the ultrasonic sensor is

ISSN: 2005-4297 IJCA

chosen, whose frequency width is from 60KHz to 400KHz with a 150KHz center frequency. In this research, bandwidth-limited circuit whose frequency is from 100KHz to 300KHz is designed for better effect.

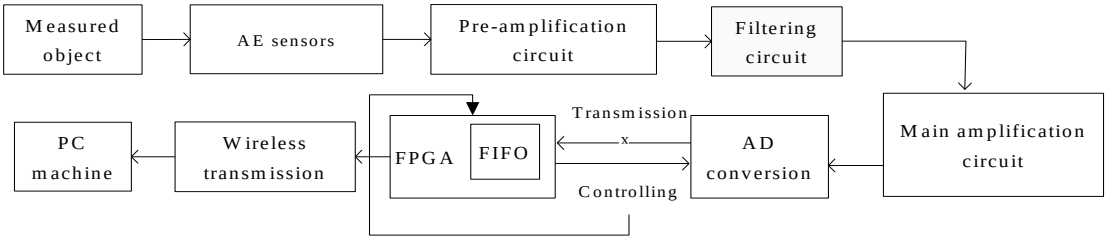

Figure 1. Flow Chart of AE Data Acquisition System

3.2. Pre-amplifier Circuit

In Figure 1, AE sensors can only acquire weak high-frequency microvolt signals. Noise ratio which is not good for analysis must be reduced after long-distance transmission. Hardware circuit can amplify the weak signal and reduce noise disturbance. Therefore, the hardware circuit design of the acquisition system is essential and directly influences post processing and analyzing results.

3.2.1. Chip selecting of the amplification circuit: Amplification circuit can be composed of discrete components and select frequency with RC filtering circuit. However, it may bring about self-excitation and disturb AE signals amplification, which leads to severely distortion. Compared with discrete components, integrated operational amplifier can magnify signals more and have better precision. In that case, the pre-amplification circuit is supposed to be composed of IOA (Integrated Operational Amplifier). Two properties are considered in chip selecting: impedance matching and gain-bandwidth product. Once transistors and circuit parameters are confirmed, the amplification and the product of frequency band can also be determined, which is called gain-bandwidth product. Because of the weak electric charge from AE sensors, input impedance of the pre-amplifier should be large enough to avoid charge leakage. In other ways, AE signals are high frequent, which means only large gain-bandwidth product can ensure stable amplification.

Chip AD620, which has 8MHz unit gain bandwidth and 10GΩ input impedance is chosen to compose our AD620 amplification circuit. It is widely used for its adjustable gain range and low noise.

3.2.2. Schematic of Pre-amplification circuit: The amplification circuit consists of two AD620 chips and each of them can enlarge 10 times. According to AD620 gain formula 1, formula 2 could be gotten.

$$G = 49.4\text{k}\,\Omega / R_G + 1 \quad (1)$$

$$R_G = 49.4\text{k}\,\Omega /(G - 1) \quad (2)$$

When gain G is 100, R_G is 5.49KΩ. So 5.49KΩ resistance can be used in the circuit. The schematic is shown in Figure 2.

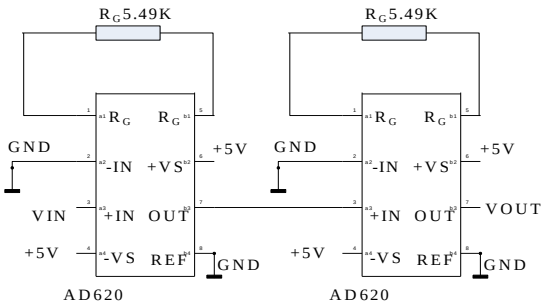

Figure 2. Schematic of Pre-Amplification Circuit

3.3. Filtering Circuit

3.3.1. Chip selecting of filtering circuit: As is known, the frequency bandwidth of wood damage AE signals is from 100KHz to 300KHz. The filtering circuit consists of high-pass circuit in series with low-pass circuit. The cut-off frequency of the low-pass circuit is 300KHz and which of the high-pass circuit is 100KH. Amplification resistance and capacities are used in the band-pass filter which is composed of IOA OP27. OP27 is a kind of bipolar operational amplifier and has low noise and low offset voltage. When the temperature is 25℃, the main offset voltage is 10 uV. The offset voltage drift is 2 uV/℃. The input bias current is 5nA and the gain-bandwidth product is 8MHz.

The filtering circuit also has magnification to ensure signals ranging from 100KHz to 300KHz can pass through the system without any loss, while signals above 300KHz or below 100KHz decay at a rate of -40dB every 10 times frequency.

3.3.2. Schematic of high-pass filtering circuit: The cut-off frequency of high-pass circuit is 100KHz. Schematic of the circuit is given in Figure 3. According to formula 3:

$$A(S) = \frac{A_0 S^2}{S^2 + \frac{S\omega_C}{Q_0} + \omega_C^2} \tag{3}$$

To be more specific:

$$\omega_C = \frac{1}{R_1 C_1}$$

$$A_0 = 1 + \frac{R_4}{R_2}$$

$$Q_0 = \frac{1}{3 - A_0}$$

$$\omega_C = 2\pi f$$

When f is 100KHz and R_2 is 1 KΩ, C_2 is 1600pF.

3.3.3. Schematic of low-pass filtering circuit: The cut-off frequency of low-pass circuit is 300KHz. Schematic of the circuit is given in Figure 3. According to formula 4:

$$A(S) = \frac{A_0 S^2}{S^2 + \frac{S\omega_C}{Q_0} + \omega_C^2} \tag{4}$$

To be more specific:

$$\omega_C = \frac{1}{R_1 C}$$

$$A_0 = 1 + \frac{R_4}{R_2}$$

$$Q_0 = \frac{1}{3 - A_0}$$

$$Q_0 = \frac{\omega_C}{2\pi f} = \frac{2\pi f}{3 - A_0}$$

$$\omega_C = 2\pi f$$

When f is 300KHz and R_2 is 1 KΩ, C_2 is 470pF.

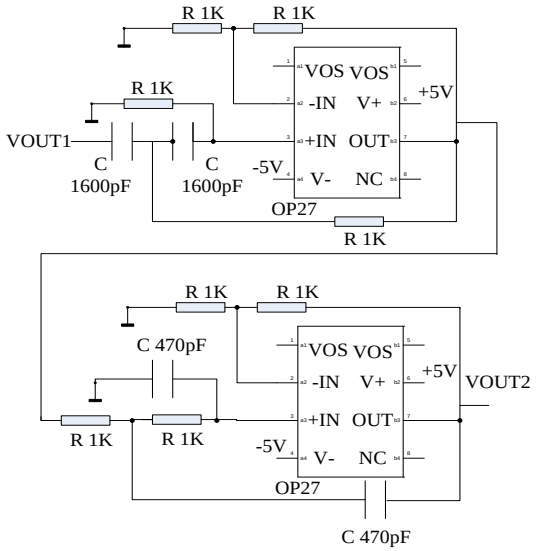

Figure 3. Schematic of Filtering Circuit

3.4. Main Amplification Circuit

The original microvolt signals are magnified to millivolt through pre-amplification and filtering circuit. The main amplification circuit can magnify millivolt signals to volt level.

3.4.1. Schematic of main amplification circuit: The circuit consists of 2 AD620 chips and each of them can magnify 15 times. Value of the resistance can be acquired by formula 2. In this circuit, RG is 3.48K. Schematic is given in Figure 4.

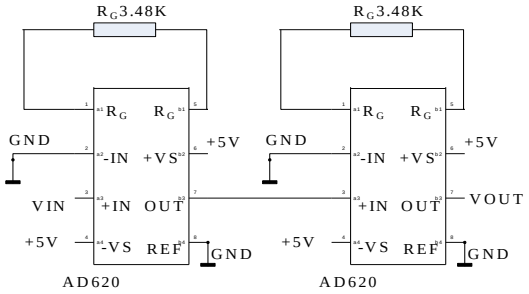

Figure 4. Schematic of Main Amplification Circuit

3.4.2. Simulation results: Multism, a kind of simulation software can make simulation diagrams and test the accuracy of the circuit design. When inputting sinusoidal wave, whose frequency is 300KHz and whose peak-to-peak volt is 5mV, we can get following results which is given in Figure 5. Channel B shows input signal whose peak-to-peak volt is 5mV. Channel A shows output signal whose peak-to-peak volt is 1V. So, the magnification is 200 times the original signals acquired from AE sensors.

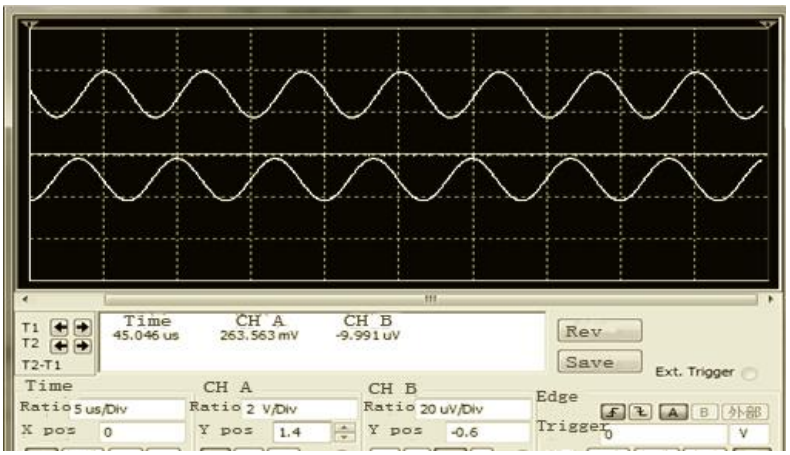

Figure 5. Schematic of Main Amplification Circuit Simulation

3.5. AD converting Circuit

AD converting circuit can convert AE signals into digital signals, which is good for data storage and transmission.

There are many types of AD converters: integral converters, parallel comparators, voltage frequency converters(VFC) and successive approximation converters. To be more specific, the conversion accuracy of the integral converters depends on integration time, so its conversion rate is low. The parallel comparators have a high speed of conversion but it has a large circuit structure and it's very expensive. VFC has high resolution, low power and low price. Nevertheless, it can't work without outer counting circuits. Successive approximation converter consists of a comparator and a DA convertor. It compares input voltage with output signal acquired sequently from DA converters and finally outputs digital signals after several comparisons. Successive approximation converters have many advantages and are used in our conversion system.

According to the features of AE signals and request of acquisition system, 12-bit ADC chip AD7893 is used to transform AE signals to digital form in consideration of conversion accuracy and acquisition speed. AD7893 processes signals in a serial

manner. VDD pin is connected to high-level voltage and REFVIN pin is connected to ground through resistance. AGND and DGND share the ground. Conversion starting signals are given from input pins while conversion ending signals are given from output pins. The schematic is given in Figure 6.

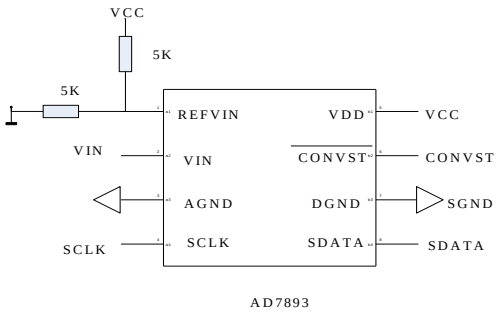

Figure 6. Schematic of AD Converting Circuit

3.6. FPGA Controlling Chip

FPGA （Field-Programmable Gate Array） is based on PAL,GAL,CPLD and other programmable devices. It not only makes up the deficiency of designed circuits, but also solves problems of limited programmable device gates.

FPGA EP3C25Q240C8 has 24624 logic units and 608256 bit internal RAM. In the system, AD conversion is controlled by FPGA. The processed data are conveyed to internal FIFO(first in first out) memory and are cached by FIFO registers to avoid data loss. Acquiring data from FIFO memory is controlled by FPGA either. Data from FIFO are transmitted to upper machines by wireless transmission module.

3.7. Wireless Transmission Module

Wireless transmission is cheaper than wired communication and has better expansibility. In this acquisition system, wired communication is replaced by wireless transmission.

Wireless transmission module RF100 has small size, high sensibility, long transmission distance and many other features. It can modify serial communicating rate, emission power and different parameters by upper machines. RF100 has UART ports, including TXD(send) and RXD(receive). Different data forms and baud rate can be set by programming. The connective schematic between RF100 and FPGA is shown in Figure 7.

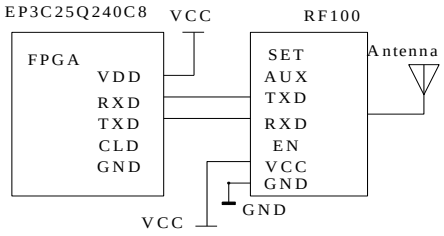

Figure 7. Connective Schematic between Wireless Transmission Module and FPGA

4. Software Design

In this system, FIFO module design, programs design (to control AD conversion and to cache data by FIFO registers) and data wireless transmission design are included in the software design.

4.1. Introduction of Hardware Description Language

The acquisition system design is supposed to write programs under Quartus II software system by using Verilog hardware description language to perform different logic functions.

4.2. AD conversion Module

AD conversion module controls AD7893 to start, delay and end AD conversion.

4.2.1. Block diagram of AD conversion programs: The block diagram of AD conversion programs is shown in Figure 8. In Figure 8, sclk is a input signal whose clock frequency is 50MHz. Sign data_o is a conversion output signal. Signal clk1M is the timing frequency of the output signal. Sign convst_n is the signal to judge whether the conversion ends. Sign out_en is the serial conversion output data enable signal. Whats more, serial data must be converted into parallel data before data are cached by FIFO registers.

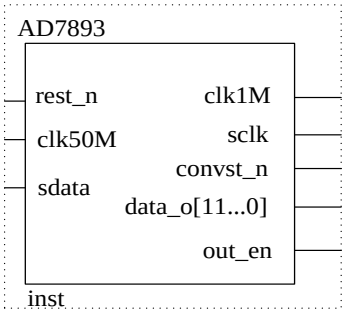

Figure 8. Block Diagram of AD Conversion Programs

4.2.2. Timing simulation of AD conversion: Timing simulation diagram is shown in Figure 9.

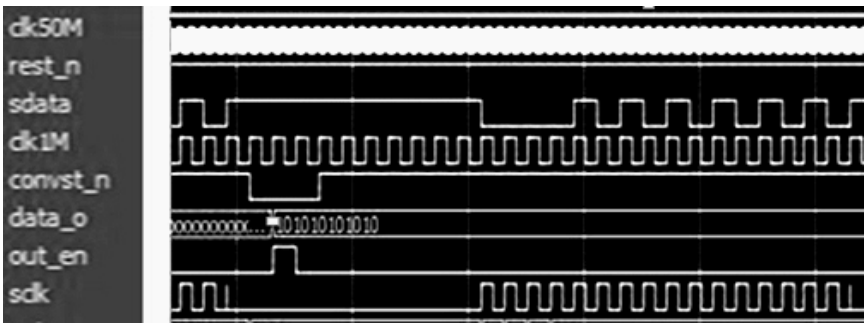

Figure 9. Timing simulation of AD Conversion

In Figure 9, clk1M whose frequency is 1MHz is divided from clk50M whose frequency is 50MHz. AD conversion starts when convst_n is high-level voltage and the converting time is 6us. Valid output signals can be acquired when sclk is high-

level voltage. Every time one-bit data transmission is over, next AD conversion starts after 600us. Meanwhile, out_en becomes high-level voltage and outputs series-parallel conversion data after every AD conversion. Among the 16-bit output data, the leading 4-bit data are 0, the other 12-bit data are valid converting results. In Figure 9, sdata is the input signal which is high-low level alternating and data_o outputting 1010 can prove the correctness of the conversion.

4.3. FIFO Design

The high speed AD conversion output data is still very high after deceleration from FPGA. In that case, it is impossible to communicate with upper machines. So, FIFO registers are used to cache data in order to communicate with upper machines.

4.3.1. Principle of FIFO: There are a number of available pins in FPGA. The acquisition data can be read in specific pin of FPGA from Pin sdata in AD. The AD converting results are stored in asynchronous FIFO. The capacity of asynchronous FIFO should be suitable for the acquired analog signals and way of hard disk storage. Every FIFO register can store 128 16-bit data, which is 256B. In this system, only one FIFO is used , so the entire capacity is 256B.

In this system, LPM(Library of Parameterized Modules) module is used in FIFO memory design which allows system to write data when FIFO is not full and to read when FIFO is not empty. And PLL(Phase Locked Logic) module is used to double frequency. When external input signal and internal oscillator signal synchronized, the system can acquire data accurately. So it is essential to double frequency by PLL module to unify clock signals. In this system, it is unnecessary to double frequency because both external and internal frequency is 50MHz.

4.3.2. Block diagram of FIFO programs: The block diagram of FIFO programs is shown in Figure 10. In Figure 10, sign clock is a clock signal. Sign q[15...0] is the output signal. Sign data [15...0] is the output converting data. The entire capacity of this synchronous FIFO is 256B.

4.3.3. Diagram of FIFO simulation: The diagram of FIFO simulation is shown in Figure 11. In Figure 11, when rdreq is 1, FIFO starts to output data. Output data from q port is 10, 20, 30 and so on which means FIFO design is accurate.

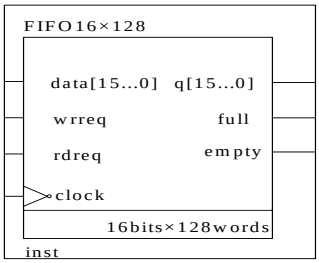

Figure 10. Block Diagram of FIFO Programs

Figure 11. Diagram of FIFO Simulation

4.4. UART Design

In this system, UART module is used to send data. There are only two modules in UART: clock module and sending module.

4.4.1. Clock and sending module: Asynchronous communication is used in this system because UART module has only data line without clock. Both communication sides confirm one specific clock frequency before UART sends data. But there must be some errors without initial time of every bit from both sides. Therefore, the system has to acquire data with high magnification clock cycles. In this system, data is acquired every 8 clock cycles and baud rate is set as 9600bps.

In sending module, data from FIFO are regarded as transmitted data. It sends one data every 8 clock cycles. The transmission begins when the first bit is 0 and ends when the last bit is 1. The block diagram of UART clock and sending module is given in Figure 12.

The input parallel data TX_Data[15...0] are output one by one through TX_Pin_Out. TX_Done_Sig gives transmission ending signals while TX_En_Sig gives transmission enable signals. When TX_En_Sig is high-level voltage, the system begins to send data.

4.4.2. Timing simulation of UART module: Diagram of UART timing simulation is given in Figure 13.

In Figure 13, input data are transmitted to TX_Data. TX_Done_Sig gives a high-level voltage pulse when data transmission ends. Meanwhile, TX_En_Sig becomes low-level voltage. And data are output through TX_Pin_Out when TX_En_Sig is high-level voltage.

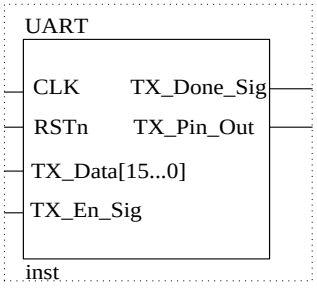

Figure 12. Block Diagram of UART Clock and Sending Module Programs

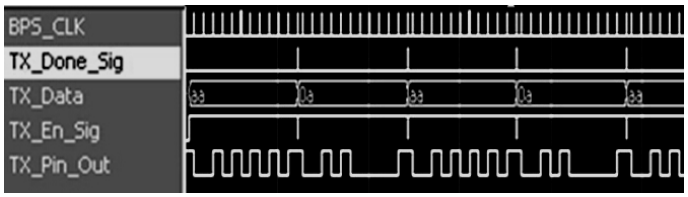

Figure 13. Timing Simulation of UART Module

4.5. Design of the Entire System

AD controlling, FIFO storage and UART transmission programs are included in the entire programs. Diagram of the entire system program is shown in Figure 14.

In Figure 14, convst_n can give 16 pulsing signals and wrreq writes 16 times when sign full is low-level voltage. Sign full becomes high-level voltage when FIFO is full. Sign convst_n gives a converting signal once rdreq signal is valid and sign

full becomes low-level voltage. Finally, TX_Pin_Out sends data at a rate of 9600bps.

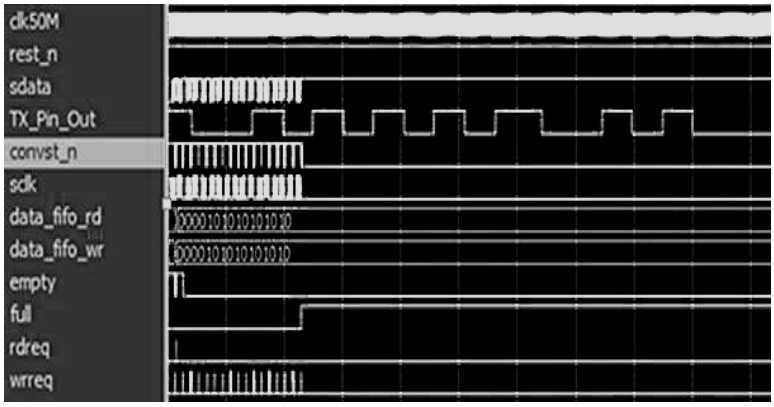

Figure 14. Timing Simulation of the Entire Software System

5. Conclusions

The acquisition system can magnify microvolt signals to volt signals and acquire AE signals ranging from 100KHz to 300KHz. The processed signals are transmitted to AD module and converted into digital form. Then data from AD conversion is read in 16-bit FIFO whose capacity is 256B at a rate of 1MHz. When FIFO is full, data are transmitted to UART in wireless transmission module and received by wireless receiving module set on the upper machines. Then upper machines analyze the receiving data and identify wood damage modes. Therefore, the whole system can detect wood damage and identify damage mode in long distance.

6. Conflict Declare

The authors declare that there is no conflict of interests regarding the publication of this article.

Acknowledgements

This Paper is supported by the Fundamental Research Funds for the Central Universities (Grant No:YX2013-24) and Beijing Forestry University Scientific And Technological Innovation Project(Grant No:S1310022036) , which are greatly acknowledged by the authors.

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