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HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA

Shivani Madhok[1], Bishwajeet Pandey[2] and Amanpreet Kaur[3], Mohamed Hashim Minver[4] and D M Akbar Hussain[5]

[1,2,3]Chitkara University Research and Innovation Network
Chitkara University
Chandigarh, Punjab
[4]Addalaichenai National College of Education, Sri Lanka
[5]Department of Energy Technology
Aalborg University, Denmark
shivanimadhok0@gmail.com[1], bishwajeet.pandey@chitkara.edu.in[2], amanpreet.kaur@chitkara.edu.in[3], mhminver@gmail.com[4], akh@et.aau.dk[5]

Abstract

In this paper we have designed an energy efficient multiplier using Nikhilam Navatashcaramam Dashatah Vedic technique. Vedic mathematics consists of 16 sutras and these sutras were used by our ancient scholars for doing there calculation faster, when there were no computers and calculators. Nikhil~~am~~ Navatasaman is a Sanskrit word which menas "all from 9 and the last from 10". In today's work the demand is high speed, efficiency and should take lesser time. Appling these Vedic techniques reduces the system complexity, execution time, area, power and is stable and hence is efficient method. In this paper we have designed an energy efficient multiplier that consists of three inputs and one output. The temperature has been kept constant that is 25 degree Celsius. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD. In order to achieve speed and high performance in addition to energy efficiency, HSTL IO standard is used. HSTL family consists of HSTL _I, HSTL_II, HSTL_I_18 and HSTL_II_18, HSTL_I_12 and the analysis has been done on these IO standards. Frequency scaling is one of the best energy efficient techniques for FPGA based VLSI design and is used in this paper. At the end we can conclude that we can conclude that there is 23-40% saving of total power dissipation by using SSTL IO standard at 25 degree Celsius. The main reason for power consumption is leakage power at different IO Standards and at different frequencies. In this research work only FPGA work has been performed not ultra scale FPGA.

Keywords: *Nikhilam Navatashcaramam Dashatah, Vedic mathematics, FPGA, energy efficient, multiplier*

1. Introduction

Ancient mathematics is known as Vedic mathematics [1-2].Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas) [3]. Vedic Mathematics offers a new holistic approach to mathematics [4]. Vedic mathematics is mainly based on sixteen Sutras [7]. These sutras can be used to solve problems in any branch of Mathematics in a faster way [9]. This Vedic mathematics can be used to solve algebra easily [10]. A lot of research work is being carried out these days on Vedic mathematics as these are the oldest mathematical techniques and require little time in solving problems and hence are

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efficient. Vedic mathematics is helpful in many fields. Many researchers have done research in this field. Multiplier and square architecture had been proposed [3]. Digital Signal Processing (DSP) operations are very important part of engineering as well as medical discipline [8].Vedic mathematics has also been implemented in field of DSP [8].A paper was published which includes DSP operations based on ancient Vedic mathematics using Vedic Urdhava-Triyagbhayam multiplication sutra [11]. A design of an 8 bits fixed point, asynchronous Vedic DSP processor core has also been studied [12]. Implementation of 4*4 multiplier using Urdhva-Tiryakbhyam in 45nm technology [13], another division architecture using different Vedic technique known as `Dhwajam'[14]. Vedic multiplier has been designed earlier using different Vedic formulas but this design using Nikhilam Navatashcaramam Dashatah vedic formula is completely a fresh work and is quite efficient [20-21].In this paper we have designed an energy efficient multiplier that consists of three inputs and one output. The inputs are x, y and clock. x and y are 8 bits numbers to be multiplied and clock is given as input for triggering. Result is the output and the multiplication of two 8 bits numbers will result into large numbers so output is considered to be 16 bit output as shown in Figure 1. The schematic diagram of multiplier using Nikhilam Navatashcaramam Dashatah is shown in Figure 2. Nikhilam Navatashcaramam Dashatah is a Sanskrit word which menas “all from 9 and the last from 10”.The design discussed in this paper uses Nikhilam Navatashcaramam Dashatah Vedic mathematics technique for its designing and implementation. Nikhilam Navatashcaramam Dashatah technique is used to multiply those numbers that can be obtained by either adding or subtracting from 10s, 100s or 1000s. The numbers are written and there right hand sides (RHS) are multiplied and left hand side (LHS) are added and subtracted from either 10, 100 or 1000. Then both the LHS and RHS are concatenated and that will result in the multiplication of the 2 numbers or as a final output.

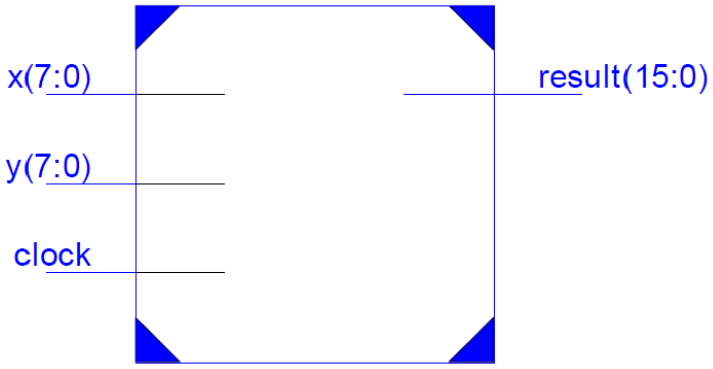

Figure 1. Symbol of Nikhilam Navatashcaramam Dashatah

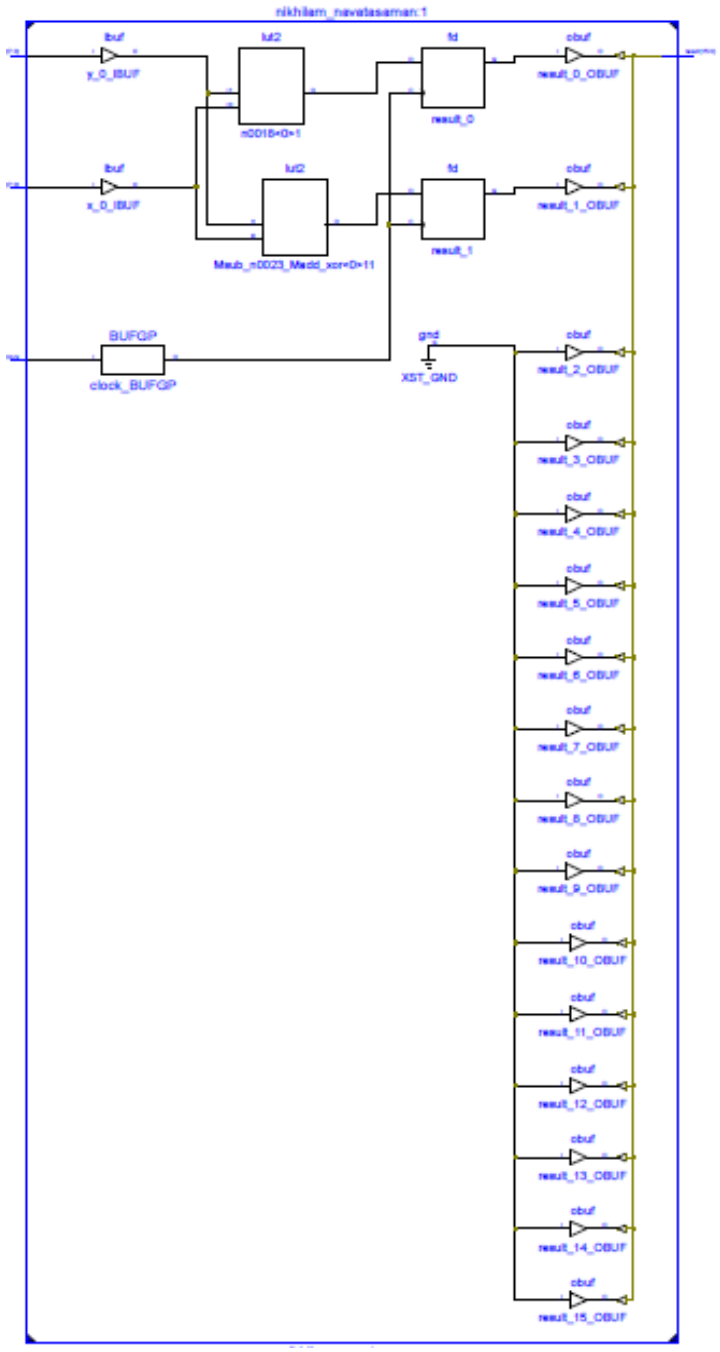

Figure 2. Schematic of Nikhilam Navatashcaramam Dashatah

The temperature has been kept constant that is 25 degree Celsius. Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [5]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD. The operating voltages of class I in case of HSTL it is 1.2V and for class II it is either 1.5V or 1.8V. In our research paper we have used HSTL _I (1.2V), HSTL_II (1.5V), HSTL_I_18 (1.8V) and HSTL_II_18 (1.8V), HSTL_I_12 (1.2V). HSTL I/O standard is used to make this design more energy efficient [6]. In order to achieve speed and high performance in addition to energy efficiency, HSTL IO standard is used. Frequency scaling is one of the best energy efficient techniques for FPGA based VLSI

design and is used in this paper as shown in Table 2. There are also different types of techniques like capacitance scaling technique [15], thermal scaling [17], clock gating [18], various design goals [19], impedance matching with different logic family, scalable implementation scheme [16] and mapping.

Table 1. Different Parameters in Kintex-7 FPGA

IO pins	676
LUT Elements	101400
Flip Flop	202800
DSPS	600
Available IOBS	400
Gb transceiver	8
Block RAM	325
GTXE2 Transceiver	8
PCI Buses	1.1
MMCMS	8
Min operating temperature	0 degree Celsius
Reference operating temperature	85 degree Celsius
Maximum operating Temperature	85 degree Celsius
Minimum operating voltage	0.97V
Reference operating Voltage	0.97V
Maximum operating Voltage	1.03V
Temperature Grade Letter	C

The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. And the device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. Table 1 shows different parameters in kintex-7 FPGA.

Table 2. Set of Frequencies Taken In Consideration

Frequency	**Mobile set**
1400MHz	Nokia Lumia 710
1.2GHz	Samsung Galaxy Core
2100MHz	I phone6
1700MHz	HTC/T
1800MHz	Micromax X091
2.2GHz	Sony Xperia Z1

2. Power Analysis

A. Power Analysis for HSTL_I IO STANDARD

Table 3. Power Analysis for HSTL_I IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.175
1.2GHz	0.156
2100MHz	0.248
1700MHz	0.207
1800MHz	0.219
2.2GHz	0.258

There is 32.53% saving in total power dissipation with 1.2 GHz when compared with 2.2 GHz as shown in Figure 3 and Table 3.

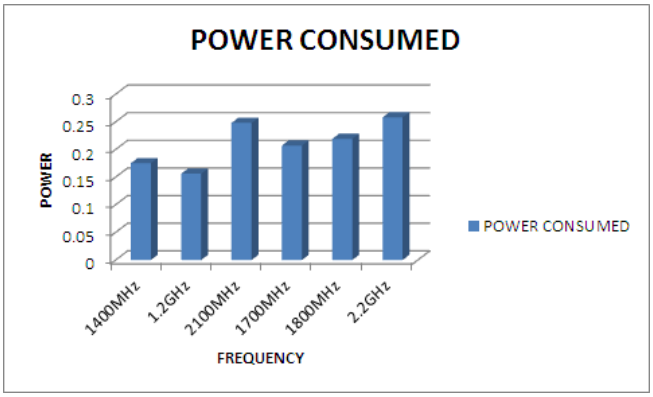

Figure 3. Power Analysis For HSTL_I IO STANDARD

B. Power Analysis for HSTL_II IO STANDARD

Table 4. Power Analysis for *HSTL_II IO* STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.194
1.2GHz	0.182
2100MHz	0.240
1700MHz	0.215
1800MHz	0.222
2.2GHz	0.246

There is 26.01% saving in total power dissipation with 1.2 GHz when compared with 2.2 GHz as shown in Figure 4 and Table 4.

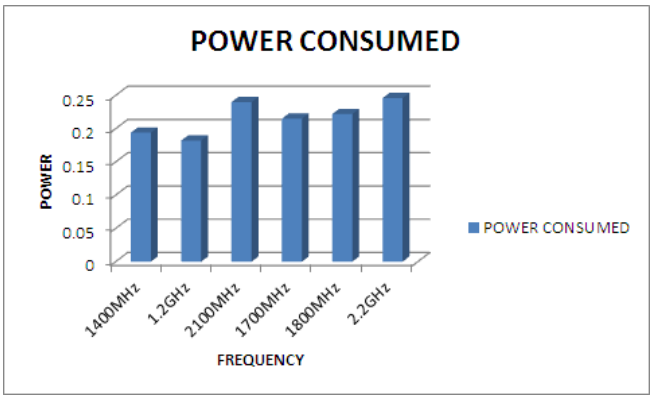

Figure 4. Power Analysis for *HSTL_II* IO STANDARD

C. Power Analysis for HSTL_I_18 IO STANDARD

Table 5. Power Analysis for *HSTL_I_18* IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.209
1.2GHz	0.187
2100MHz	0.299
1700MHz	0.249
1800MHz	0.264
2.2GHz	0.310

There is 39.67% saving in total power dissipation with 2.2 GHz when compared with 1.2 GHz as shown in Figure 5 and Table 5.

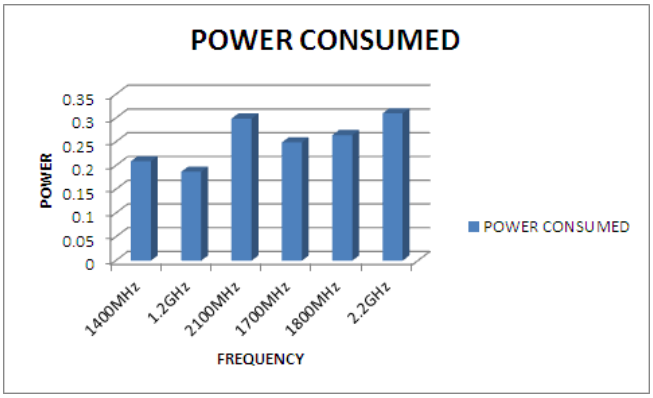

Figure 5. Power Dissipation for HSTL_I_18 IO STANDARD

D. Power Analysis for HSTL_II_18 IO STANDARD

Table 6. Power Analysis For HSTL_II_18 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.238
1.2GHz	0.225
2100MHz	0.289
1700MHz	0.260

1800MHz	0.269
2.2GHz	0.295

There is 23.72% saving in total power dissipation with 2.2 GHz when compared with 1.2 GHz as shown in Figure 6 and Table 6.

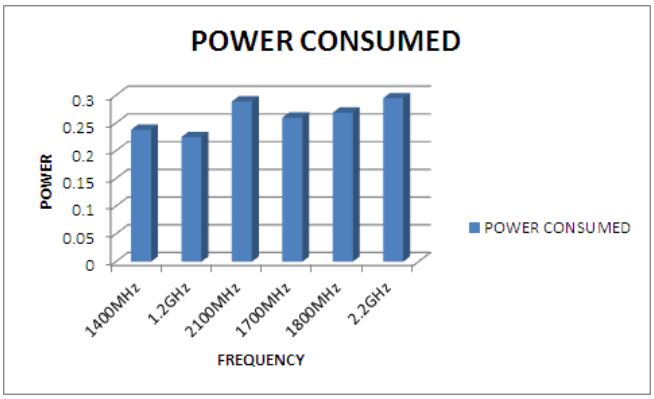

Figure 6. Power Analysis for HSTL_II_18 IO STANDARD

E. Power Analysis for HSTL_I_12 IO STANDARD

Table 7. Power Analysis for HSTL_I_12 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.125
1.2GHz	0.115
2100MHz	0.163
1700MHz	0.142
1800MHz	0.148
2.2GHz	0.168

There is 31.54% saving in total power dissipation with 2.2 GHz when compared with 1.2 GHz as shown in Figure 7 and Table 7.

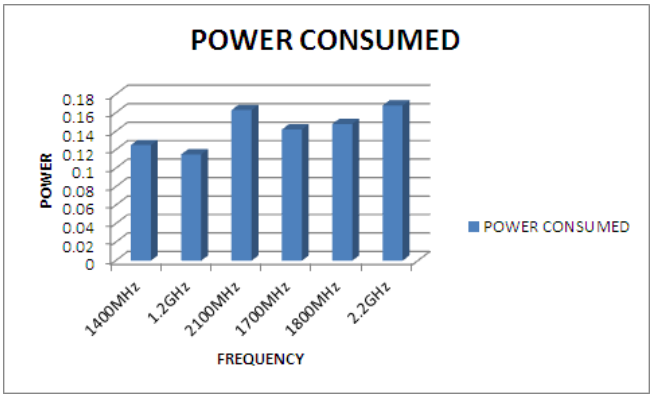

Figure 7. Power Analysis for HST_I_12 IO STANDARD

F. Power Analysis for Different IO Standard with Different Frequencies

Table 8. Power Analysis for HSTL Family at Different Frequencies

IO STANDARD	1400 MHz	1.2 GHz	2100 MHz	1700 MHz	1800 MHz	2.2 GHz
HSTL_I	0.175	0.156	0.248	0.207	0.219	0.258
HSTL_II	0.209	0.187	0.299	0.249	0.264	0.310
HSTL_I_18	0.194	0.182	0.240	0.215	0.222	0.246
HSTL_II_18	0.238	0.225	0.289	0.260	0.269	0.295
HSTL_I_12	0.125	0.115	0.163	0.142	0.148	0.168

From Table 8 and Figure 8 we can say that maximum power is consumed with HSTL_II and minimum power consumption is with HSTL_I_12.

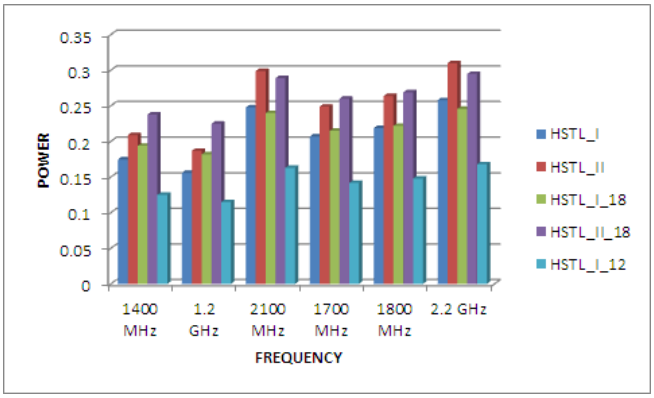

Figure 8. Power Analysis for HSTL Family at Different Frequencies

3. Conclusion

In this paper we have designed an energy efficient multiplier that consists of three inputs and one output. The inputs are x, y and clock. x and y are 8 bits numbers to be multiplied and clock is given as input for triggering. Result is the output and the multiplication of two 8 bits numbers will result into large numbers so output is considered to be 16 bit output. The temperature has been kept constant that is 25 degree Celsius. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD. Frequency scaling is one of the best energy efficient techniques for FPGA based VLSI design and is used in this paper. We can conclude that there is 23-40% saving of total power dissipation by using SSTL IO standard at 25 degree Celsius. Maximum power is consumed with HSTL_II and minimum power consumption is with HSTL_I_12.

4. Future Scope

The future scope of "HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA" is that we can also implement this design on 22nm or 18 nm FPGA. We can also use different FPGA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E. Here, we are using frequency scaling in which we are

changing the operating frequency of a device and analyzing its power. We can redesign this Vedic multiplier with other energy efficient technique like capacitance scaling, thermal scaling, clock gating, various design goals, impedance matching with different logic family, and mapping. Analysis has been done with different frequencies like 1400 MHz, 1.2 GHz, 2100 MHz, 1700MHz, 1800MHz, 2.2GHz. We can use any other frequency range and test our design on that also. The temperature has been kept constant that is 25 degree Celsius so if needed it can also be varied. Air flow can also be varied when required.

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