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Modeling and Implementation of a Self-Reference Voltage Pre-Regulator

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Abstract

The paper proposes a novel self-reference voltage pre-regulator for LED driver chip. The system modeling of the self-reference voltage pre-regulator is established, which is composed of pre-regulator circuit and reference voltage generating circuit. The reference voltage generating circuit generates a reference voltage, in which the circuit returns the reference voltage as the reference voltage of pre-regulator circuit, therefore, the pre-regulator outputs a stable voltage for the LED driver chip. In this paper, the circuit implementation is described in detailed, in order to enhance the stability of the system, the miller compensation is used to the circuit, which makes the system more stable. Simulations of the circuit show that the pre-regulator not only can output a stable voltage for the chip, but also the load regulation, line regulation and power support ripple rejection of the pre-regulator exhibit high performance.

Keywords: *The Self-Reference Voltage Pre-Regulator, System Modeling, Circuit Implementation, Stable Output Voltage*

1. Introduction

As the progress of light emitting diode (LED) technology, the LED lighting is becoming as a promising illumination solution and a more and more popular choice consider in general[1-4]. There are many advantages of LED lighting, such as high efficiency, longer life time, fast response, low power, smaller size and less pollution, these make LED lighting is widely used in residential lighting , traffic lighting , flash lighting and so on[5-9].

However, the LED driver chip has a power supply question. AC line is rectified, and is connected to an output capacitor of chip. Therefore, an instantaneous input and output power difference exists in a half line cycle when the charge and discharge action in every half line cycle, as shown in [10], this makes the power supply of LED driver chip is unstable. Traditional design uses a zener diode in the chip, which provides power for the chip. However, if there is not zener diode in the process, or the process has zener diode, but the voltage of zener diode is not needed for the chip, therefore, using zener diode is not suitable.

In order to provide a stable voltage for the LED driver chip, a novel self-reference voltage pre-regulator is designed. Using the feedback mechanism, the pre-regulator not only can output stable voltage for the LED driver chip, but also the reference voltage is generated by it-self.

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2. Modeling of the Pre-Regulator

2.1. System Modeling of the Pre-Regulator

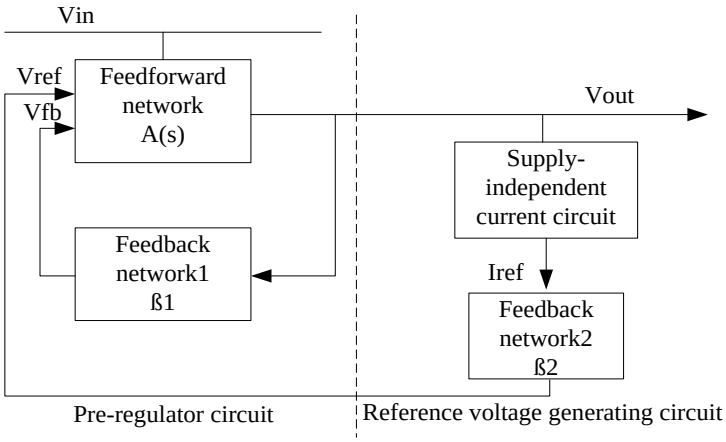


Figure 1: System Modeling of the Pre-Regulator

The system modeling of pre-regulator is shown in Figure 1. The voltage V_{in} is power supply, which comes from outside of the chip. Pre-regulator is composed of the pre-regulator circuit and reference voltage generating circuit. Pre-regulator circuit outputs a stable output voltage V_{out}, which is used to power for the other blocks of chip and is returned by feedback network1 as the feed-forward network input voltage V_{fb}. Reference voltage generating circuit is powered by the output voltage V_{out} and outputs reference current I_{ref}, which is independent of the output voltage V_{out}. The feedback network2 senses the reference current I_{ref} and returns a reference voltage V_{ref}, which can be written as:

$$V_{ref} = \beta_2 I_{ref} \qquad (1)$$

Where, β_2 is feedback factor of the feedback network2, because the reference current I_{ref} is independent of the output voltage V_{out}, so the reference voltage V_{ref} is also independent of the output voltage V_{out}.

As shown in figure 1, the output voltage V_{out} can be expressed by the following equation:

$$V_{out} = \frac{A_{op}(s)}{1 + A_{op}(s)\beta_1} Vref \qquad (2)$$

Where, $A_{op}(s)$ is the open loop transfer function of the feed-forward network, β_1 is feedback factor of the feedback network1. The equations of (1) and (2) exhibit that output voltage V_{out} is independent of the power supply V_{in}.

2.2. Structure Modeling of the Pre-regulator

Figure 2 shows a structure modeling of the pre-regulator. Feed-forward network is composed of error amplifier, buffer and power output stage. Error amplifier senses and amplifies the feedback errors, so the accuracy is vital parameter in the

design of error amplifier, and error amplifier must respond quickly to restrain the errors of output voltage V_{out} which are caused by the rapid load changes and power supply ripple.

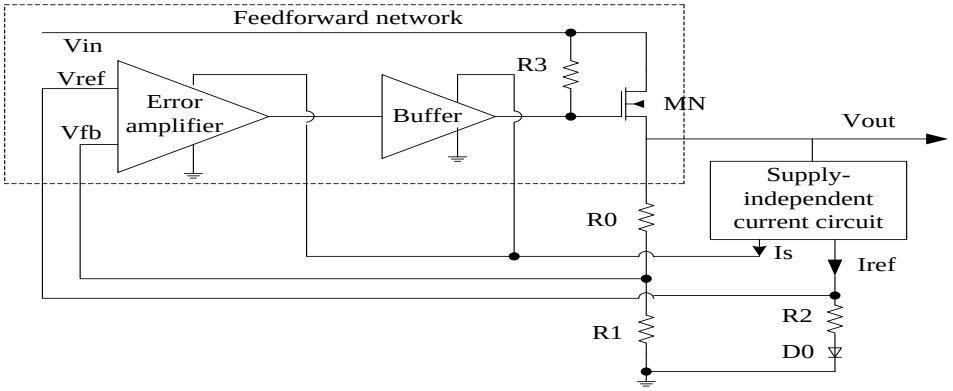


Figure 2: Structure Modeling of the Pre-Regulator

The buffer is necessary for the pre-regulator circuit. Because the output voltage of error amplifier is powered by supply-independent current circuit as shown in Figure ure 2, so the power supply of error amplifier is low, which causes the output voltage of error amplifier is low, but the power output switch MN is a n-type MOSFET, which gate requires high voltage to drive, therefore, buffer shifts the output voltage of error amplifier and the input voltage of the power output stage to make the circuit work better. And there are large parasitic capacitances in the power output switch MN, in order to make power output switch response quickly, buffer is necessary, because buffer can provide sufficient current and voltage for the power output switch.

The power output stage can provide stable voltage for load. Using the n-type MOSFET as the power output switch is that power output stage is a source follower, which exhibits a small impedance approximately the reciprocal of the transconductance of the power output switch MN, this means that power output stage can respond quickly when load changed rapidly, therefore, the n-type is selected.

The feedback network1 is a resistive divider as shown in Figure ure 2, which is a frequency-independent quantity. The feedback factor can be calculated as following equation:

$$\beta_1 = R_1/(R_0 + R_1) \qquad (3)$$

Therefore, the feedback voltage V_{fb} can be expressed by the following equation:

$$V_{fb} = \beta_1 V_{out} \qquad (4)$$

Hence, a fraction of the output voltage V_{out} is sensed by feedback network1 and compared with the input of error amplifier, generated an error term. Thus, in a well-designed feedback system, the error term is minimized.

As shown in Figure 2, supply-independent current circuit outputs current I_s and I_{ref}, which are independent of the output voltage V_{out}. The current I_s provides power supply for error amplifier and buffer, current I_{ref} flows through the resistor R_2 and diode D_0 to generate the reference voltage V_{ref}, therefore, the V_{ref} can be calculated as:

$$V_{ref} = \beta_2 I_{ref} = R_2 I_{ref} + V_{diode} \qquad (5)$$

Where, voltage V_{diode} is threshold voltage of diode D_0.

3. Circuit Implementation

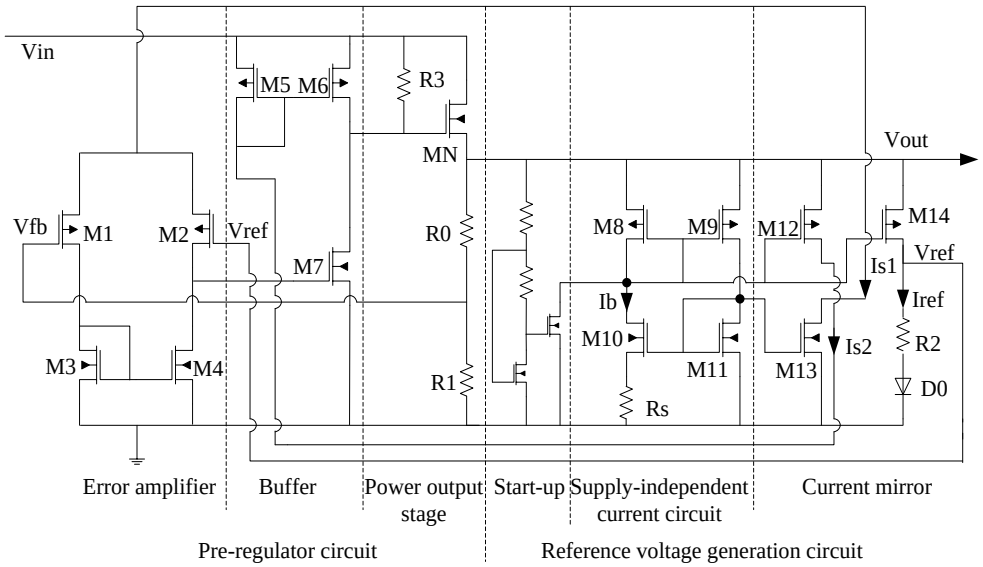


Figure 3: Circuit Implementation

Error amplifier is a double-end input single-end output differential amplifier, which is composed of MOSFET $M_1 \sim M_4$. The input signals of error amplifier are voltage V_{ref} and V_{fb}, the output signal of error amplifier is connected to buffer, power supply is the current I_{s1} of reference voltage generation circuit as shown in figure 3. The low-frequency gain $A_{(EA)}(0)$ of the error amplifier can be expressed as following equation:

$$A_{(EA)}(0) = g_{m(M1)} R_{out(EA)} \qquad (6)$$

Where, $g_{m(M1)}$ is the transconductance of M1, $R_{out(EA)}$ is the output resistance of the error amplifier, $R_{out(EA)}$ can be calculated as:

$$R_{out(EA)} = r_{o(M2)} // r_{o(M4)} \qquad (7)$$

Where, $r_{o(M2)}$ is the output resistance of M2, $r_{o(M4)}$ is the output resistance of M4.

Buffer is a common-source operational amplifier which is composed of MOSFET M5, M6 and M7. M7 converts an error amplifier output change $\Delta V_{out(EA)}$ to a drain current change $g_{m(M7)} \Delta V_{out(EA)}$, hence the buffer has an output voltage change $g_{m(M7)} R_{out(buffer)} \Delta V_{out(EA)}$, so the low-frequency gain $A_{(buffer)}(0)$ of the buffer is expressed as following equation:

$$A_{(buffer)}(0) = -g_{m(M7)} R_{out(buffer)} \qquad (8)$$

Where, $g_{m(M7)}$ is the transconductance of M7, $R_{out(buffer)}$ is the output resistance of the buffer, $R_{out(buffer)}$ can be calculated as following equation:

$$R_{out(buffer)} = r_{o(M6)} // ro_{(M7)} // R_3 \qquad (9)$$

Where, $r_{o(M6)}$ is the output resistance of M6, $ro_{(M7)}$ is the output resistance of M7, R_3 is resistor, which can provide a bias voltage for power output switch MN.

The power output stage is source follower, so the low-frequency gain $A_{(power\_output)}(0)$ of output power state is approximate 1. R_{out} is the output resistance of power output stage, which can be calculated as:

$$R_{out} = (R_0 + R_1) // (1/g_{m(MN)}) \approx 1/g_{m(MN)} \qquad (10)$$

$g_{m(MN)}$ is the transconductance of power output switch MN.

Thus, the low-frequency open loop gain $A_{op}(0)$ of pre-regulator circuit can be expressed as following equation:

$$\begin{aligned} A_{op}(0) &= A_{(EA)}(0)A_{(buffer)}(0)A_{(power\_output)}(0) \\ &= -(g_{m(M1)}R_{out(EA)}g_{m(M7)}R_{out(buffer)}) \end{aligned} \qquad (11)$$

From equation (2), the low-frequency power output voltage V_{out} can be obtained:

$$V_{out} = \frac{A_{op}(0)}{1 + A_{op}(0)\beta_1} Vref = [\frac{1}{\beta_1}(1 - \frac{1}{1 + A_{op}(0)\beta_1})]Vref \qquad (12)$$

Equation (12) implies that increasing the value of the low-frequency gain $A_{op}(0)\beta_1$, the error of the low-frequency power output voltage V_{out} can be reduced.

The supply-independent current circuit generates current I_b as depicted in figure 3. The current I_b can be calculated as:

$$I_b = \frac{2}{\mu_n C_{ox}(W/L)_{M11}} \frac{1}{R_s^2}(1 - \frac{1}{\sqrt{K_1}})^2 \qquad (13)$$

Where, $\mu_n C_{ox}$ is the device transconductance parameter of the n-type MOSFET, $(W/L)_{M10}$ and $(W/L)_{M11}$ are the width to length ratio of M10 and M11, K_1 is given as:

$$K_1 = \frac{(W/L)_{(M10)}}{(W/L)_{(M11)}} \qquad (14)$$

Equations (13) and (14) imply that the current I_b is independent of the output voltage V_{out}. Reference current I_{ref} can be calculated as:

$$I_{ref} = K_2 I_b \qquad (15)$$

Where, K_2 is written as:

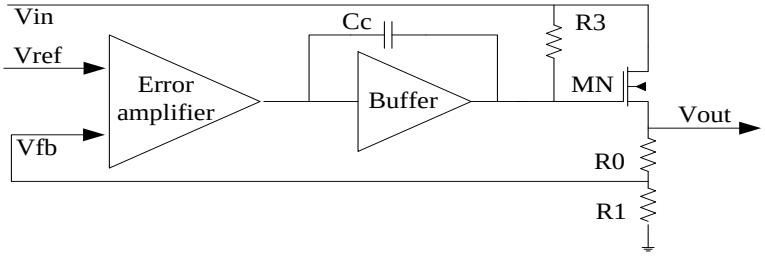
$$K_2 = \frac{(W/L)_{(M14)}}{(W/L)_{(M8)}} \qquad (16)$$

Thus, the output voltage V_{out} can be obtained from equations (2), (5), (13) and (15),

$$V_{out} = \frac{A(s)}{1+A(s)\beta_1}\beta_2 K_2 \frac{2}{\mu_n C_{ox}(W/L)_{M11}} \frac{1}{R_s^2}(1-\frac{1}{\sqrt{K_1}})^2 \qquad (17)$$

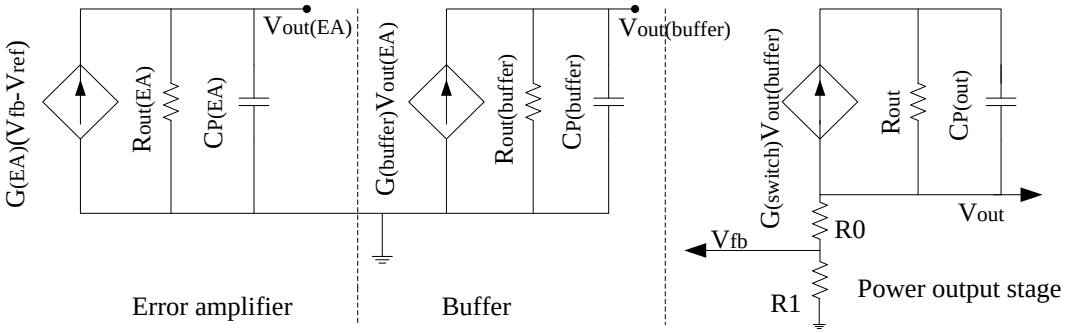
4. Stability Analysis and Frequency Compensation

Because the reference voltage V_{ref} is independent of the out voltage V_{out}, the reference voltage V_{ref} does not affect the stability of the circuit. Therefore, that only analyses the pre-regulator circuit, which is a negative feedback network. Figure ure 4 (a) shows the structure modeling of the pre-regulator circuit, and Figure ure 4 (b) shows the small-signal equivalent circuit of the pre-regulator circuit. As shown in figure 4 (b), where, $G_{(EA)}$ is the transconductance of the error amplifier, $R_{out(EA)}$ is the output resistance of the error amplifier, $C_{P(EA)}$ is the output terminal parasitic capacitance of the error amplifier. $G_{(buffer)}$ is the transconductance of the buffer, $R_{out(buffer)}$ is the output resistance of the error buffer, $C_{P(buffer)}$ is the output terminal parasitic capacitance of the buffer, $G_{(switch)}$ is the transconductance of the power output stage, R_{out} is the output resistance of the power output stage, $C_{P(out)}$ is the output terminal parasitic capacitance of power output stage.



(a) The Structure Modeling Of Pre-Regulator Circuit

(b)



(b) The Small-signal Equivalent Circuit of the Pre-regulator Circuit.

Figure 4: The Pre-Regulator Circuit Topology

Before compensation, there are three poles in the circuit as shown in figure 4 (b), which can be calculated as:

$$P_{out(EA)} = -\frac{1}{R_{out(EA)}C_{P(EA)}} = -\frac{1}{(r_{o(M2)} // r_{o(M4)})C_{P(EA)}} \quad (18)$$

$$P_{out(buffer)} = -\frac{1}{R_{out(buffer)}C_{P(buffer)}} = -\frac{1}{(r_{o(M6)} // r_{o(M7)} // R_3)C_{P(buffer)}} \quad (19)$$

And

$$P_{out} = -\frac{1}{R_{out}C_{P(out)}} = -\frac{g_{m(MN)}}{C_{P(EA)}} \quad (20)$$

Where, $P_{out(EA)}$ is an output terminal pole of error amplifier, $P_{out(buffer)}$ is an output terminal pole of buffer, P_{out} is an output terminal pole of power output stage. The value of the $R_{out(EA)}$, $R_{out(buffer)}$ and R_{out} can be obtained from equations (7), (9) and (10). From the equations (18), (19) and (20), the three poles relation can be expressed as:

$$P_{out(EA)}, P_{out(buffer)} \le P_{out} \quad (21)$$

Therefore, the output terminal pole P_{out} of power output stage is a high-frequency pole, which does not affect the stability of the circuit, so the pole P_{out} can be ignored.

Because the relative position of $P_{out(EA)}$ and $P_{out(buffer)}$ is relatively close, hence, the circuit exhibits two dominant poles, so the phase approaches -180 °. In other words, the phase margin of the circuit maybe close to zero, this makes the system suffer from instability.

In order to enhance the stability of the system, Miller compensation is used for frequency compensation. The Miller capacitor C_c is connected from the output to the input of the buffer as shown in figure 4 (a). After compensation, the pole $P_{out(EA)(Miller)}$ can be expressed as:

$$P_{out(EA)(Miller)} = -\frac{1}{R_{out(EA)}[C_{P(EA)} + (1 + A_{(buffer)}(0))C_C]} \quad (22)$$

Where, C_c is the Miller capacitor.

The pole $P_{out(buffer)(Miller)}$ can be written as:

$$P_{out(buffer)(Miller)} = -\frac{g_{m(M7)}}{C_{P(buffer)}} \quad (23)$$

Where, $g_{m(M7)}$ is the transconductance of M7. Comparing $P_{out(EA)(Miller)}$ with the $P_{out(EA)}$, Miller compensation moves the $P_{out(EA)}$ closer to the origin of complex frequency plane, and comparing the $P_{out(buffer)(Millor)}$ with the $P_{out(buffer)}$, Miller compensation moves away the $P_{out(buffer)}$ from the origin of the complex frequency plane, the frequency compensation improves the phase margin as shown in figure 5.

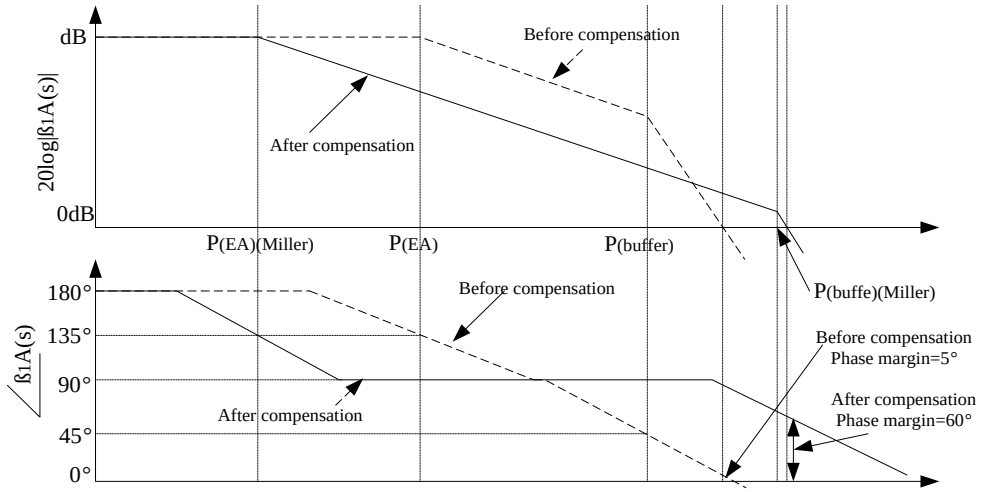


Figure 5: Bode Plots of Before Compensation and After Compensation

5. Simulation and Analysis

The circuit is simulated based on BCD350 process. Because the pre-regulator acts in the chip, and the range of input voltage V_{in} is 8~30V, therefore, the output voltage V_{out} must be stabilized within the range of input voltage V_{in}. As the shown in figure 6, when the input voltage V_{in} is 7.2V, the output voltage is 4.99914V, and when the input voltage V_{in} is 30V, the output voltage is 5.00119V, there is only a difference of 2.05mV.

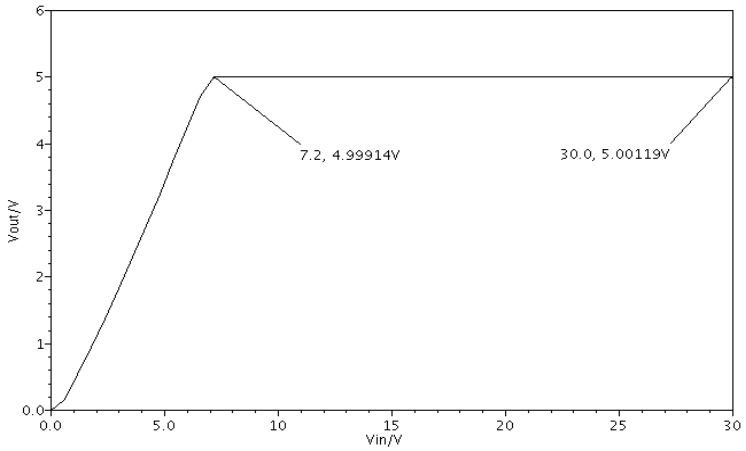


Figure 6: DC of Simulation of Input Voltage

Load regulation (LDR) is an important performance for pre-regulator, which reflects a change of output voltage V_{out} variation resulting from the load current I_{load} variation. The LDR can be expressed as following equation:

$$LDR = \frac{\Delta V_{out}}{\Delta I_{load}} \qquad (24)$$

Where, ΔV_{out} is variation of the output voltage V_{out}, ΔI_{load} is the variation of the load current I_{load}. Figure ure 7 shows the waveforms of the LDR, when the load current from

zero to 100mA, the input voltage is 11V, 12V and 13V. Table 1 shows the LDR of the pre-regulator.

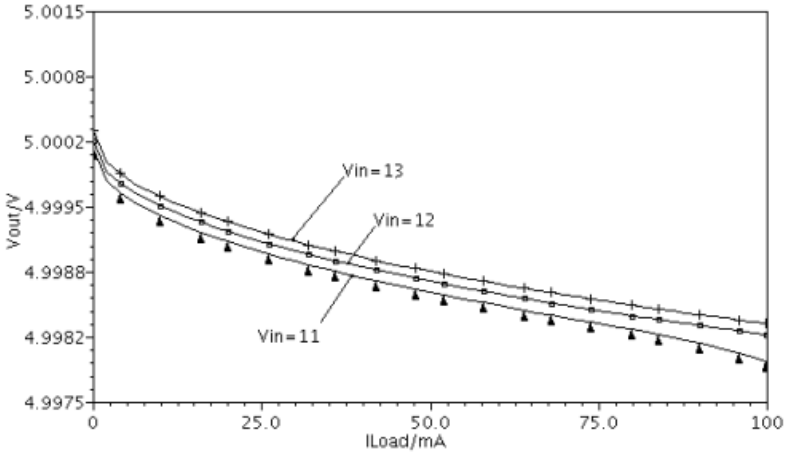


Figure 7: The Waveforms of LDR

Table 1: LDR ,When The Load Current From 0 To 100ma, Input Voltage Is 11V, 12V And 13V

V_{in}	ΔV_{out}	LDR
$V_{in}=11V$	$\Delta V_{out}=5.00008V-4.99791V=2.17mV$	$LDR=2.17mV/100mA$
$V_{in}=12V$	$\Delta V_{out}=5.00018V-4.99819V=1.99mV$	$LDR=1.99mV/100mA$
$V_{in}=13V$	$\Delta V_{out}=5.00027V-4.9983V=1.99mV$	$LDR=1.97mV/100mA$

Line regulation (LNR) is also a vital performance, which describes the output voltage V_{out} variation arising from change in the input voltage V_{in}, which can be expressed as:

$$LNR=\frac{\Delta V_{out}}{\Delta V_{in}} \qquad (25)$$

Where, ΔV_{out} is variation of the output voltage V_{out}, ΔV_{in} is the variation of the input voltage V_{in}. Table2 shows the LNR, when input voltage V_{in} from 11V to 12V, load current I_{load} is 1mA, 10mA and 100mA, the waveforms of LNR are shown in figure 8.

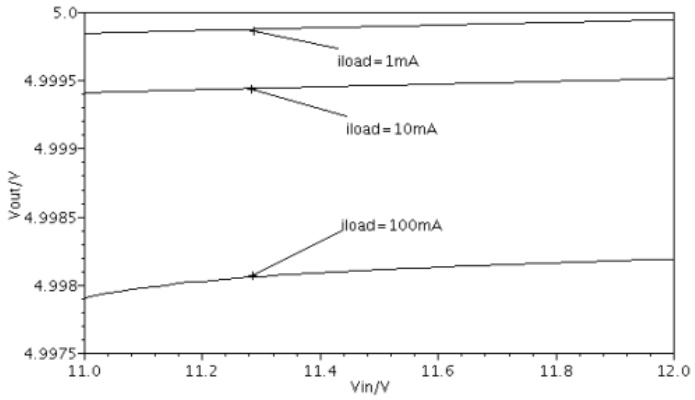


Figure 8: The Waveforms of LNR

Table 2: LNR, When Input Voltage from 11V to 12V, Load Current Is 1ma, 10ma and 100ma

I_{load}	ΔV_{out}	LNR
$I_{load} = 1mA$	$\Delta V_{out} = 4.999943V - 4.99984V = 0.103mV$	$LDR = 0.103mV/V$
$I_{load} = 10mA$	$\Delta V_{out} = 4.999511V - 4.99941V = 0.101mV$	$LDR = 0.101mV/V$
$I_{load} = 100mA$	$\Delta V_{out} = 4.998188V - 4.99791V = 0.278mV$	$LDR = 0.278mV/V$

Power supply ripple rejection (PSRR) refers broadly to the ability of the circuit to regulate its output voltage V_{out} against small-signal variation in the input voltage V_{in}. The figure 9 shows the waveform of PSRR. As the shown in figure 9, when the frequency is 10 KHz, the PSRR is -58dB.

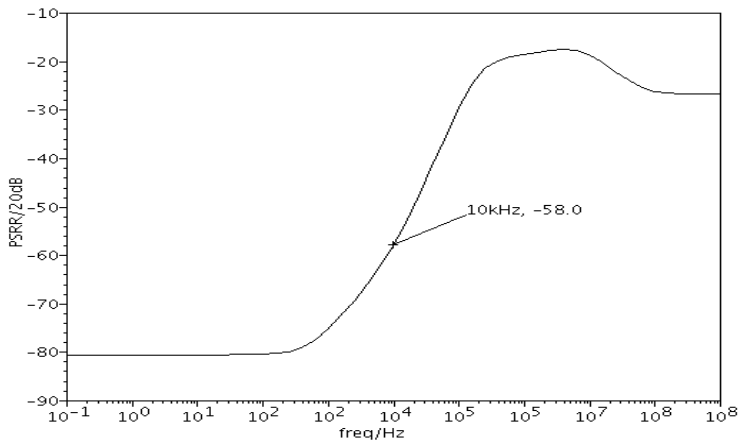


Figure 9: The Waveform of PSRR

6. Conclusion

In this paper, a self-reference voltage pre-regulator is proposed for LED driver chip. In order to provide stable voltage for LED driver chip, the pre-regulator circuit and reference

voltage generating circuit are designed. Using feedback mechanism, the reference voltage is generated by the reference voltage generating circuit and is returned as a reference of the pre-regulator circuit, the pre-regulator circuit outputs a stable voltage for the LED driver chip.

The system modeling and structure modeling is established for the pre-regulator, circuit implementation is described in detail. In order to enhance the stability of system, the Miller compensation is used for frequency compensation.

The results of simulation show that the load regulation, line regulation and power supply ripple rejection are better.

Acknowledgments

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