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Super-Threshold Adiabatic SRAM Based On PAL-2N Operating In Medium Strong Inversion Region

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Abstract

The SRAM (static random access memory) extensively used in computers, embedding hardware, and other digital systems is a main source of power dissipations. In order to reduce the increasing power dissipation of the SRAM, a low-power adiabatic SRAM is introduced. The proposed SRAM is realized by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) to reduce its dynamic energy consumption. The GLB (gate-length biasing) and DTCMOS (dual-threshold CMOS) techniques are used to reduce its leakage consumption. An improved storage cell is used to reduce the power dissipation of the storage array. The proposed SRAM based on PAL-2N with GLB and DTCMOS techniques is investigated with different source voltages in terms of energy dissipation and maximum operating frequency. All circuits are simulated with HSPICE using SMIC 130nm CMOS technology. The results show that the proposed SRAM attain 80% energy saves compared with the static SARM at 1.2V source voltage. In addition, the simulation results also show that the super-threshold adiabatic SRAM operating in medium strong inversion regions achieves low energy dissipation with reasonable operating speed.

Keywords: *Adiabatic computing; computer hardware; super-threshold computing; SRAM; PAL-2N*

1. Introduction

The SRAM (static random access memory) is extensively used in computers, embedding hardware, and other digital systems. It is reported that the SRAM is a main source of power dissipations [1, 2]. The energy consumption is composed by two components: dynamic consumption and static consumption [3]. Dynamic energy consumption contains switching energy consumption and short energy consumption. The adiabatic circuits can reduce the switching energy consumption by using the AC power-supply instead of the DC power-source. When completing a charge and discharge process for the load capacitance, the formula of energy consumption of the adiabatic circuits in a cycle with the AC power-supply is

$$E = 2(\frac{RC_L}{T}) * C_L V^2 \quad (1)$$

It is concluded that the E and T are proportional to the inverse ratio. When the T is large, the E becomes small. It is the adiabatic manner.

Although the dynamic energy consumption occupies the major portion of the energy consumption, the proportion of leakage consumption is gradually rising with the size scaling down of MOS transistors. In low-power circuits design, reducing leakage consumption is becoming more and more important [4]. In order to reduce the leakage

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consumption, the gate-length biasing and DTCMOS techniques are used to design the near-threshold PAL-2N SRAM [5].

Gate-length biasing technology can reduce the leakage consumption by using long gate-length transistor in the non-critical paths. Leakage consumption is caused by leakage current of MOS device: sub-threshold leakage, gate leakage and reverse-biased drain-substrate junction band to band tunneling leakage. The sub-threshold leakage has an exponential dependence on gate-length, gate leakage is linearly proportional to gate-length, and drain-substrate leakage does not depend on gate-length [6]. It has been proved that, the 8nm biasing of gate-length can effectively reduce leakage consumption up to 30% with less than 5% delay penalty with the SMIC 130nm [7].

The application of DTCMOS techniques leads to a reduction of the sub-threshold leakage [8]. This will reduce the leakage energy consumption [9]. The high-threshold transistor is used in the non-critical paths to reduce the leakage current. The low-threshold transistor is used in the critical paths to guarantee the performance of the whole circuit. A 32×32 SRAM is designed using the PAL-2N circuits to reduce the dynamic consumption. The gate-length and DTCMOS techniques are used in the PAL-2N SRAM to reduce the leakage consumption.

This paper uses 8T (eight CMOS transistors) storage cell to design the storage cell array. The storage cell is composed by two back-gate transistor in the read path to improve the stability of the SRAM.

In addition, a simple and effective way to reduce energy consumption is to scale down the supply voltage. The dynamic energy consumption and the leakage consumption are decreased significantly as voltage scaling down. Scaling voltage to the near-threshold region (threshold voltage VTH) can greatly reduce the dynamic energy consumption. The near-threshold circuit works in a moderate inversion [10-12].

In this paper, a low-power adiabatic SRAM is introduced to reduce the energy consumption of the SRAM. The proposed SRAM is realized by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) circuits to reduce its dynamic energy consumption. The GLB (gate-length biasing) and DTCMOS (dual-threshold CMOS) techniques are used to reduce its leakage consumption. An improved storage cell is used to reduce the energy consumption of the storage array. The PAL-2N SRAM with GLB and DTCMOS techniques is investigated with different source voltages in terms of energy dissipation and maximum operating frequency. All circuits are simulated with HSPICE using SMIC 130nm CMOS technology. The simulation results show that the super-threshold adiabatic SRAM operating in medium strong inversion regions achieves low energy dissipation with reasonable operating speed.

2. PAL-2N Circuits

PAL-2N circuits consist of two main parts: the logic assignment circuit and energy recovery circuit. Figure 1(a) is the PAL-2N buffer/inverter schematic, and the layout of the PAN-2N buffer/inverter. The logic assignment circuit is composed by two NMOS logic transistors: N3 and N4. The energy recovery circuit is composed by P1 and P2. The energy of the output node is recovered to the *CLK* through the P1 and P2. The transistor N1 and N2 muzzle the output node voltage, making it not hung up. PAL-2N circuits use non-overlapping four-phase sinusoid. The design of the power-clock generating circuits is very simple.

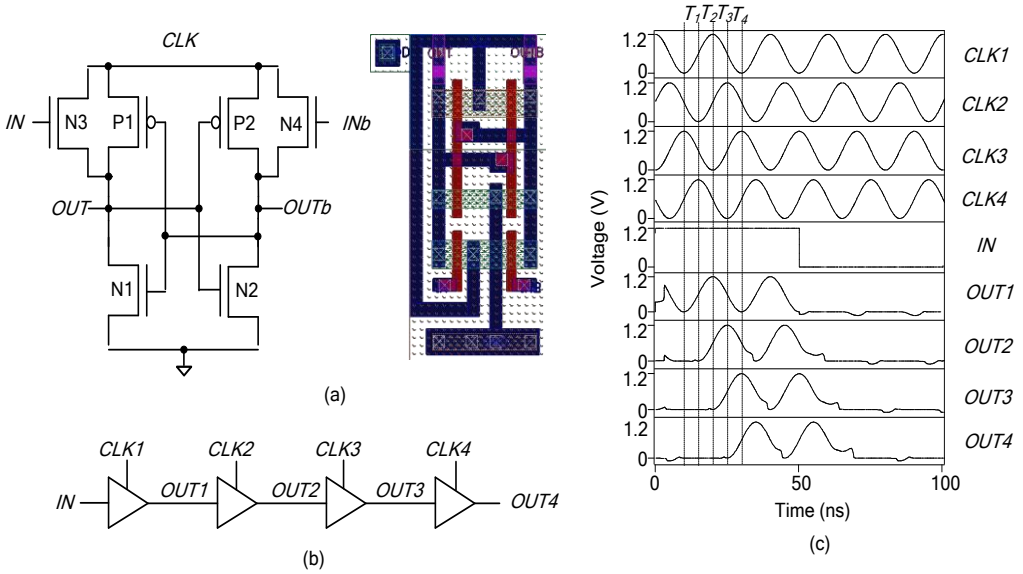


Figure 1. Basic Gate Of PAL-2N. (A) CPAL Buffer/Inverter And Its Layout, (B) Buffer Chain, And (C) Simulation Waveforms

Figure 1 (b) is the fourth buffer chain schematic. Figure 1 (c) shows the simulation waveform of the PAL-2N buffer chain and four-phase sinusoid. The four-phase power-clock as the ideal power-clock on adiabatic SRAM is used in this paper. Complex logic circuits can be derived simply by replacing the NMOS pass transistor trees with the corresponding logic function blocks [3].

3. SRAM BASED on PAL-2N Circuits

In the design of PAL-2N SRAM, all circuits (the word-line decoder and the read/write driver) use the PAL-2N circuits except the storage cell array. The PAL-2N SRAM can reduce the overall energy consumption. The following introduces the composition of PAL-2N SRAM schematics and the storage cell in detail.

The PAL-2N SRAM schematic structure is as same as the conventional CMOS SRAM structure. The structure of the PAL-2N SRAM schematic is shown in Figure 2. The conventional SRAM circuit consumes more energy than the adiabatic one.

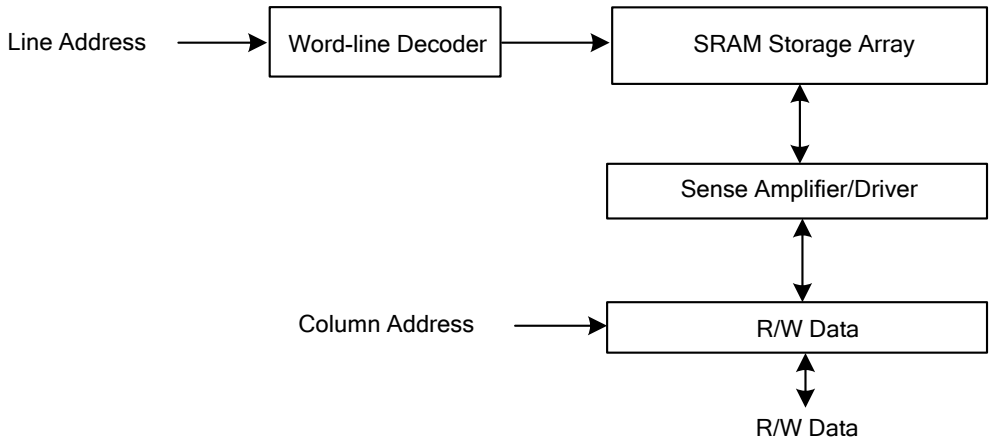
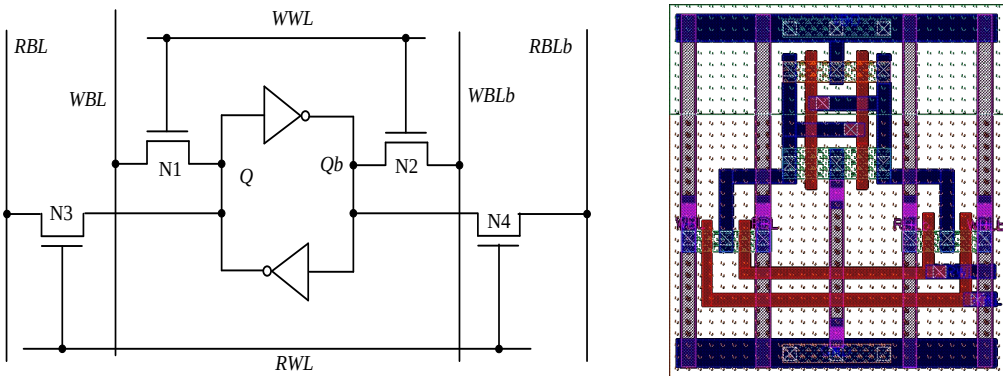


Figure 2. SRAM Structure Based On PAL-2N Circiuts

3.1. Storage Cell

Conventional storage cell and its improved design are shown in Figure 3 and Figure 4.



(a) Conventional storage cell

(b) The layout of the storage cell

Figure 3. Conventional Storage Cell

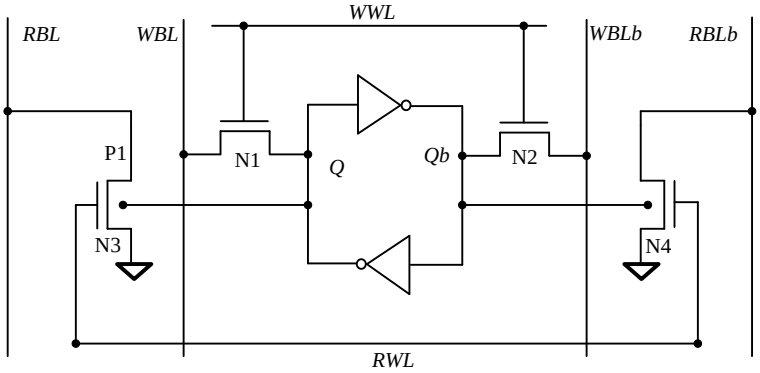


Figure 4. Improved Storage Cell

3.2 Word-Line Decoder

The word-line decoder schematic is shown in Figure 5. It is a secondary decoder like the traditional one. The pre-decoder is realized by 5-bit address decoder and the secondary decoder is realized by 32 NAND gates, which can generate the *WL0* … *WL31*. Then the read/write signal (*RE* and *WE*) contacts the output of the second decoder though NAND gates, which can generates *RWL0* … *RWL31* and *WWL0* … *WWL31*. The Figure 6 shows the energy consumption of the PAL-2N word-line decoder and conventional word-Line decoder. From the simulation result, we can conclude that: the PAL-2N word-line decoder consumes less energy than the conventional word-line decoder.

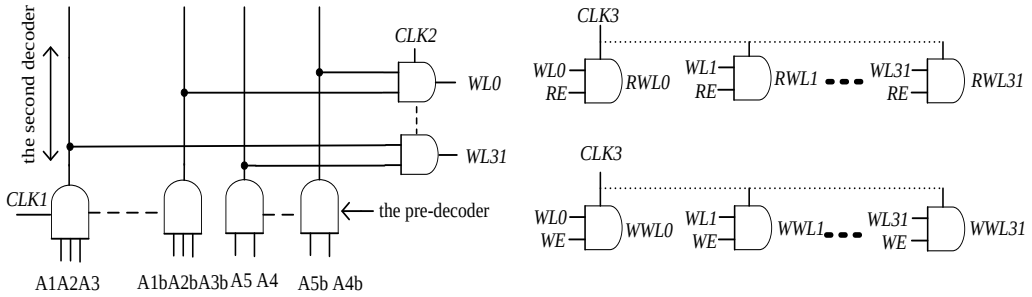


Figure 5. Word-Line Decoder Based On PAL-2N Circiuts

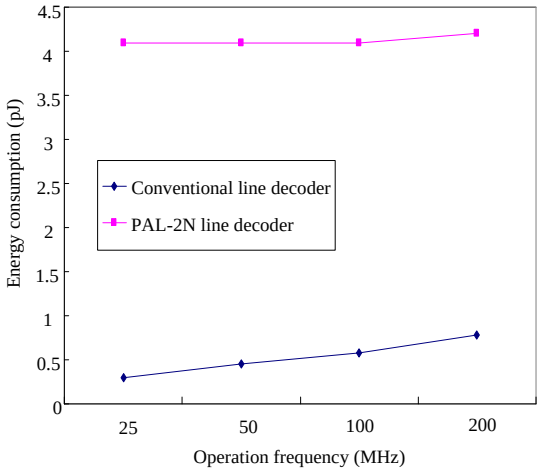
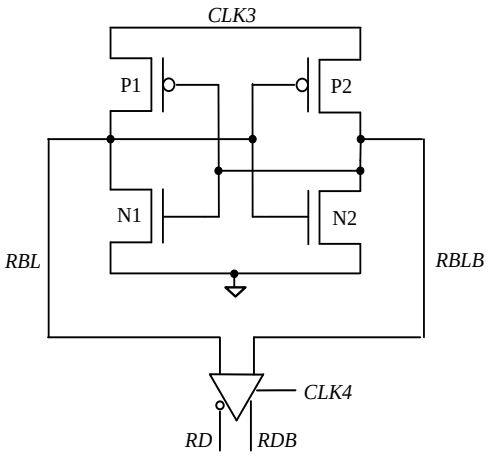


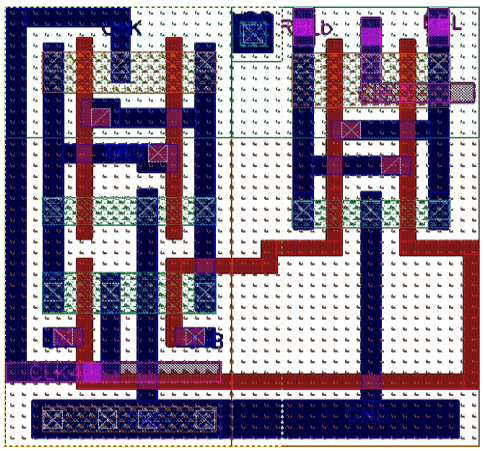
Figure 6. Energy Consumption Of PAL-2N Word-Line Decoder And Conventional Word-Line Decoder

3.3 Read/write Driver and Sense Amplifier

The read and write driver schematic use the PAL-2N structure. The write driver can write the contents in the form of the PAL-2N buffer as shown in Figure 1(a), which can generate *WBL0 WBL31* (write bit line). When the voltage of the write word line is 1.2V, the data is written to the storage cell. The read driver circuit uses the same topology as write driver circuit. The sense amplifier circuit is Figure 7. It is composed by two back to back inverters. When the voltage of the read word line is 1.2V, the sense amplifier schematic can amplify the potential difference between the RBL and RBLB, and generating *RD* and *RDB*.



(a) Sense amplifier



(b) Layout of the read driver

Figure 7. Sense Amplifier Schematic And Layout

4. PAL-2N SRAM with Leakage Reduction Techniques

4.1 PAL-2N SRAM with Gate-Length Biasing Technique

The formula (2) is the leakage current equation. We can conclude that increasing the gate length of the CMOS transistor can lower the leakage current and then lower the leakage energy consumption. The leakage current decreases exponentially while the delay increases linearly with appreciably increasing gate length.

$$I_d = \frac{\mu C_{OX}}{2}(\frac{W}{L})(V_{GS} - V_T)^2(1+\lambda V_{DS}) \quad (2)$$

The application of the gate-length (L) technique can lower the leakage energy consumption in an acceptable performance range. In this paper, the gate-length biasing technique is applied in the cell-level, which uses the same gate-length biasing in a cell circuit. The gate length of the transistor uses 138nm with the SMIC 130nm technology in this paper.

The PAL-2N buffer with the gate-length biasing technology only needs to substitute the N1 and N2 in Figure 1(a) for long gate-length CMOS transistor. The basic PAL-2N NAND XOR NOR gates also substitute the N1 and N2 for long gate-length CMOS transistor. The PAL-2N SRAM with gate-length biasing technique uses the same structure as the basic PAL-2N SRAM.

4.2 PAL-2N SRAM with DTCMOS Technique

The DTCMOS technique is to uses high-threshold transistor on the non-critical path of the schematic and low-threshold transistor on the critical path of the schematic. Formula 5.2 is the sub-threshold leakage current (I_{sub}). From formula 5.2, it can be concluded that V_T (threshold voltage) and I_{sub} is inversely proportional. Therefore, the application of DTCMOS technology can reduce the leakage consumption. The PAL-2N buffer with the DTCMOS technology only needs to substitute the P1 and P2 in Figure 1(a) for high-threshold CMOS transistor. The basic PAL-2N NAND/XOR/NOR gates also substitute the P1 and P2 for high-threshold CMOS transistor. The PAL-2N SRAM with DTCMOS technique uses the same structure as the basic PAL-2N SRAM.

$$I_{sub} = \frac{W}{L}\mu V_T^2 C_{sth} \exp\left(\frac{V_{GS} - V_{th} + \eta V_{DS}}{nV_T}\right) \times \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (3)$$

4.3 PAL-2N SRAM with Gate-Length Biasing and DTCMOS Techniques

The PAL-2N buffer with gate-length biasing and DTCMOS techniques substitute the N1 and N2 for long gate-length transistor and the P1, P2 for the high-threshold transistor in Figure 1(a). The basic PAL-2N NAND/XOR/NOR gates have the same structure. The layout of the 32×32 IPAL-2N (improved PAL-2N) SRAM designed with cadence is shown in Figure 8.

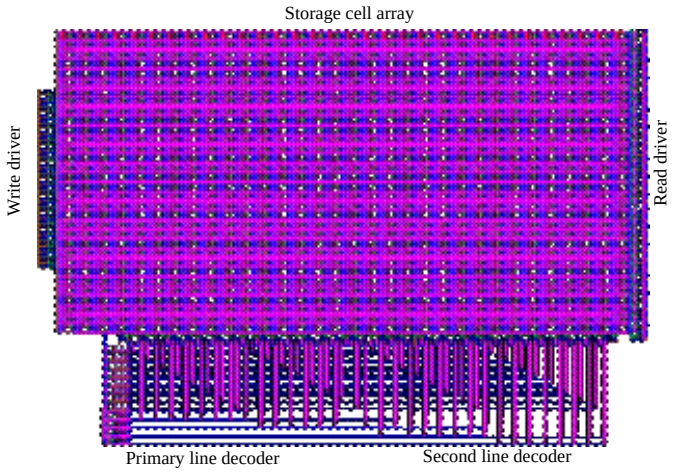


Figure 8. Layout Of PAL-2N SRAM

The layout is composed by the read/write schematic, line decoder and storage array. Firstly, design rule checking is used to the layout. Secondly, layout versus schematic is matched. Finally, parasitic capacitance and resistance is extracted by PEX. The area of the IPAL-2N SRAM layout is 207.96um×158.6um. Three layers metal (metal1, metal2 and metal3) is used in the design of the layout. Metal1 and metal2 is used in design of the cell circuits. Meatal3 is used in the connecting of the whole circuit. The route of the layout is horizontal and vertical.

The post-simulation is carried out by HSPICE. Figure 9 and Figure 10 show the functional waveform and energy consumption. The functional waveform of the IPAL-2N SRAM is shown in Figure 9. On the period of the line decoder, the write operation is ready to start. When the voltage of WWL is high, the WBL is ready for write data to the storage cell. In the working of the line decoder, the voltage of *RWL* starts to be high, and the *RBL* and sense amplifier reads the data stored in the storage cell then getting the RD. The topology of the PAL-2N SRAM with gate-length biasing and DTCMOS techniques is as the basic PAL-2N SRAM.

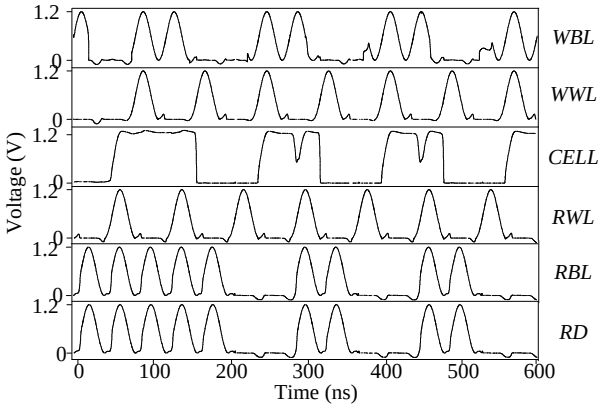


Figure 9. Simulated Waveforms PAL-2N SRAM With DTCMOS

From Figure 10, the energy consumption of IPAL-2N SRAM reduces 5% compared with the basic PAL-2N SRAM at 100MHz. Compared with the IPAL-2N SRAM, the energy consumption of the IPAL-2N SRAM with gate-length biasing reduces 10% at 100MHz.

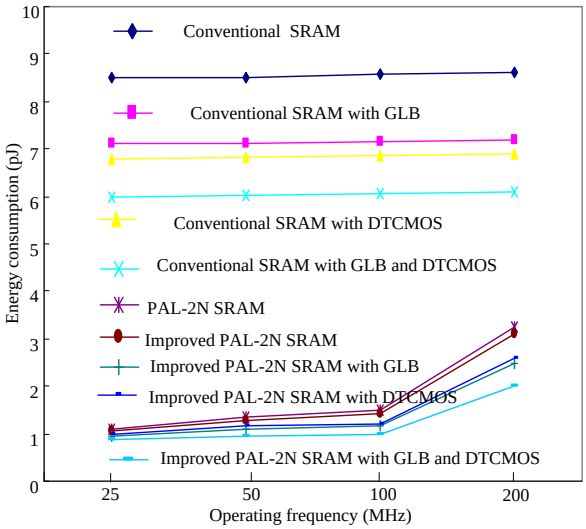


Figure 10. Energy Consumption Of The Conventional SRAM, Conventional +GLB SRAM, Conventional +GLB+DTCMOS SRAM, PAL-2N SRAM, IPAL-2N

SRAM, IPAL-2N+GLB SRAM, IPAL-2N+DTCMOS SRAM And The IPAL-2N +GLB+DTCMOS SRAM From 25 To 200 Mhz

The adiabatic SRAM consumes less energy than the conventional SRAM, and the IPAL-2N SRAM with gate-length biasing consumes less energy than the conventional SRAM with gate-length biasing. Compared with the IPAL-2N SRAM, the energy consumption of the IPAL-2N SRAM with DTCMOS technique reduces 15% at 100MHz. The IPAL-2N SRAM with DTCMOS technique consumes less energy than the conventional SRAM with DTCMOS technique. Compared with the IPAL-2N SRAM, the energy consumption of the IPAL-2N SRAM with gate-length biasing and DTCMOS technique reduces 22% at 100MHz. The IPAL-2N SRAM with gate-length biasing and DTCMOS technique consumes less energy than the conventional SRAM with gate-length biasing and DTCMOS technique. Conventional +GLB SRAM are the conventional SRAM with gate-length biasing.

Conventional +DTCMOS SRAM are the conventional SRAM with DTCMOS technique. Conventional+GLB+DTCMOS SRAM are the conventional SRAM with gate-length biasing and DTCMOS technique. IPAL-2N+GLB SRAM is the IPAL-2N SRAM with gate-length biasing. IPAL-2N+DTCMOS SRAM is the IPAL-2N SRAM with DTCMOS technique. IPAL-2N+GLB+ DTCMOS SRAM is the IPAL-2N SRAM with gate-length biasing and DTCMOS technique.

Tabel 1 is energy consumption of the storage cell, read driver circuit and write circuit of PAL-2N SRAM, PAL-2N+GLB SRAM, PAL-2N+DTCMOS SRAM, PAL-2N+GLB+DTCMOS SRAM and conventional SRAM at 100MHz. From Table 1, we can conclude that the energy consumption of the IPAL-2N SRAM storage cell is less than the PAL-2N SRAM. The application of the gate-length biasing and DTCMOS technique reduces the leakage consumption then reducing the overall energy consumption.

Table 1. Energy Consumption of SRAM at 100mhz (Pj)

SRAM	Storage cell	Read driver	Write driver
PAL-2N	0.0651	0.25	0.21
IPAL-2N	0.062	0.25	0.21
IPAL-2N+GLB	0.062	0.221	0.187
IPAL-2N+DTCMOS	0.0618	0.205	0.172
IPAL-2N+GLB+DTCMOS	0.062	0.174	0.157
Conventional	0.078	2.27	2.03

5. Super-threshold Computing for SRAM

The PAL-2N SRAM with gate-length biasing and DTCMOS technique operating in medium strong inversion regions and strong inversion regions is simulated. Figure 11 shows the maximum frequency and the corresponding energy dissipations at different working voltage. From Figure 11, we can conclude that the maximum frequency of SRAM is 50MHz-150MHz in 0.9V – 1.1V. When the SRAM operates in 0.9V-1.1V, it can not only make SRAM works correctly, but also reduce the energy consumption. The energy consumption reduces 57% at 1.0V. The super-threshold adiabatic SRAM operating in medium strong inversion regions fits for mid-performance with low energy dissipation.

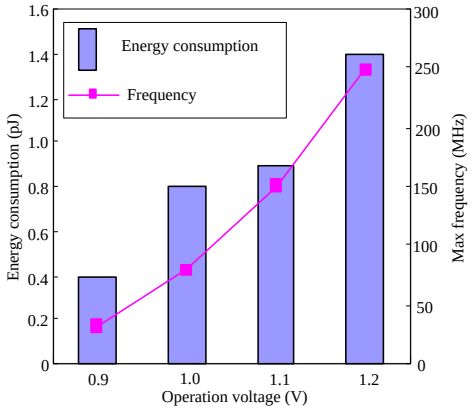


Figure 11. Energy Consumption Per Cycle At Max Frequency With Different Operation Voltage Of PAL-2N SRAM

Figure 12 is the energy consumption of conventional SRAM at 500MHz. We can conclude that although the performance of conventional SRAM is better than the PAL-2N SRAM operating in the super-threshold region, the energy consumption of PAL-2N SRAM is less than the conventional SRAM.

The super-threshold technique needs not particular manufacturing process, and without any supplementary circuits. It is very convenient to use the super-threshold technique by changing the working voltage. Because the supply voltage is provided by external interface, the voltage is selected by the requirement of the circuits and the parameter characteristic of the different working voltage of the PAL-2N SRAM. The robustness of the super-threshold circuits must be considered. The correctness of read and write operation and the correctness of the access data of the storage cell can be guaranteed by changing the width to length ratio to increase the drive of the circuit.

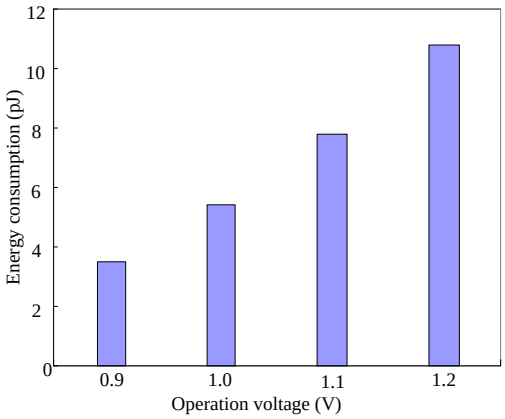


Figure 11. Energy Consumption Per Cycle At 500mhz With Different Operation Voltage Of Conventional SRAM

6. Conclusion

A low-power adiabatic SRAM has been introduced. The proposed SRAM is realized by PAL-2N to reduce its dynamic energy consumption. The GLB (gate-length biasing) and DTCMOS (dual-threshold CMOS) techniques are used to reduce its leakage consumption. An improved storage cell is used to reduce the power dissipation of the storage array. The proposed SRAM based on PAL-2N with GLB and DTCMOS techniques has been investigated with different source voltages in terms of energy dissipation and maximum operating frequency. The results show that the proposed SRAM attain 80% energy saves

compared with the static SARM at 1.2V source voltage. In addition, the simulation results also show that the super-threshold adiabatic SRAM operating in medium strong inversion regions achieves low energy dissipation with reasonable operating speed.

Acknowledgements

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