International Journal of Control and Automation
Vol. 8, No. 7 (2015), pp. 47-54
http://dx.doi.org/10.14257/ijca.2015.8.7.05

HSTL IO Standard Based Energy Efficient FIR Filter Design on 28nm FPGA

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Abstract

In this research paper, we have designed an energy efficient FIR Filter that is very much useful in digital signal processing (DSP). FIR is a finite impulse response (FIR) filter is a filter whose impulse response is of finite duration. In this paper we have aimed to design a FIR Filter that consists of three inputs and one output. The three inputs are input data that is 8 bit or 1 byte (finite), clock and reset. The output is 18 bits (finite) wide. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. The design has been tested on Kintex-7. Power analysis has been done at different operating frequencies. In this paper we have done frequency scaling technique to obtain energy efficient design. The temperature has been kept constant that is 25 degree Celsius. Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [12]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD. HSTL family consists of HSTL _I, HSTL_II, HSTL_I_18 and HSTL_II_18, HSTL_I_12 and the analysis has been done on these IO standards. We can conclude that there can be 23-33% saving of total power dissipation by using frequency scaling technique.

Keywords*: HSTL, FIR, Filter, FPGA, energy efficient, Frequency Scaling*

1. Introduction

In Digital signal processing, a finite impulse response (FIR) filter is a filter whose impulse response is of finite duration [1]. Such type of response is called finite because it settles to zero in finite time [1]. The response is also to any finite length input. In this paper we have aimed to design a FIR Filter that consists of three inputs and one output. The three inputs are input data that is 8 bit or 1 byte (finite), clock and reset. The output is 18 bits (finite) wide as shown in Figure 1. The schematic of FIR filter can be seen in Figure 2. Finite Impulse Response (FIR) Filter can be designed as per our requirements by formulation of specifications [2]. We can design FIR Filter as low pass[3], high pass filter[4], bandpass [5], bandstop [4] filter according to our specifications and requirements. The 1D FIR optimal bandstop filters are based on Zolotarev polynomial [14]. FIR Filter can be two-dimensional (2-D) [7].

ISSN: 2005-4297 IJCA

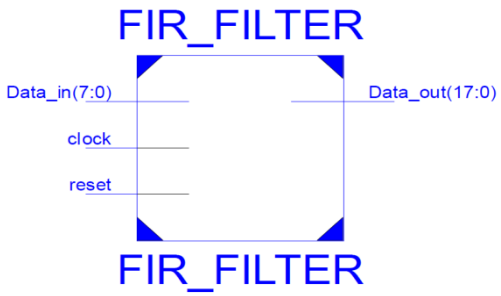

Figure 1. Symbol of FIR Filter

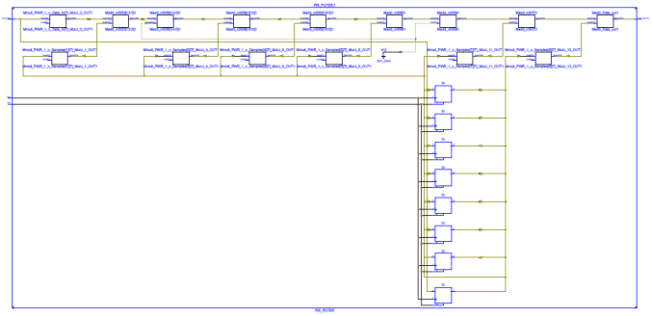

Figure 2. Schematic of FIR Filter

Table 2. Set of Frequencies Taken in Consideration

Frequency	Mobile set
1400MHz	Nokia Lumia 710
1.2GHz	Samsung Galaxy Core
2100MHz	I phone6
1700MHz	HTC/T
1800MHz	Micromax X091
2.2GHz	Sony Xperia Z1

The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. The design has been tested on Kintex-7 and the device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. Table 3 shows different parameters in kintex-7 FPGA.

Table 2. Different Parameters in Kintex-7 FPGA

IO pins	676
LUT Elements	101400
Flip Flop	202800
DSPS	600
Available IOBS	400
Gb transceiver	8
Block RAM	325
GTXE2 Transceiver	8
PCI Buses	1.1
MMCMS	8
Min operating temperature	0 degree Celsius
Reference operating	85 degree Celsius

temperature	
Maximum operating Temperature	85 degree Celsius
Minimum operating voltage	0.97V
Reference operating Voltage	0.97V
Maximum operating Voltage	1.03V
Temperature Grade Letter	C

Power analysis has been done at different operating frequencies listed in Table 2. Different sets of mobile phones operate at different frequencies and these frequencies are considered for designing an energy efficient device. In this paper we have done frequency scaling technique to obtain energy efficient design. There are different types of techniques like capacitance scaling technique [6], thermal scaling [9], clock gating [10], various design goals [11], impedance matching with different logic family, scalable implementation scheme [8] and mapping. The temperature has been kept constant that is 25 degree Celsius.Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [12]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. IO Standards has been varied in order to achieve an energy efficient device. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD.HSTL family consists of HSTL _I, HSTL_II, HSTL_I_18 and HSTL_II_18, HSTL_I_12 and the analysis has been done on these IO standards. HSTL I/O standard is used to make this design more energy efficient [13].

3. Power Analysis

A. Power Analysis for HSTL_I IO STANDARD

Table 3. Power Analysis for HSTL_IIO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.311
1.2GHz	0.283
2100MHz	0.407
1700MHz	0.352
1800MHz	0.366
2.2GHz	0.422

There is 32.93% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 3 and Table 3.

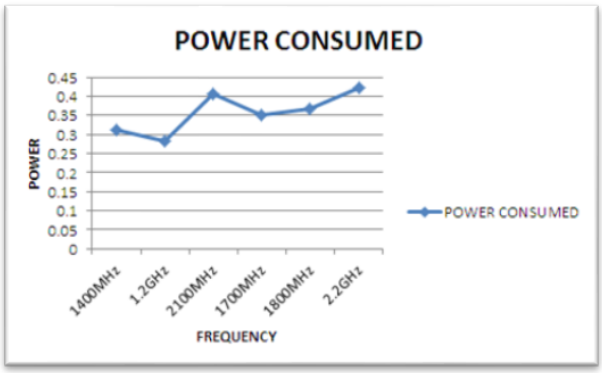

Figure 3. Power Analysis for HSTL_IIO STANDARD

B. Power Analysis for HSTL_II IO STANDARD

Table 4. Power Analysis for HSTL_II IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.303
1.2GHz	0.283
2100MHz	0.370
1700MHz	0.332
1800MHz	0.342
2.2GHz	0.381

There is 25.72% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 4 and Table 4.

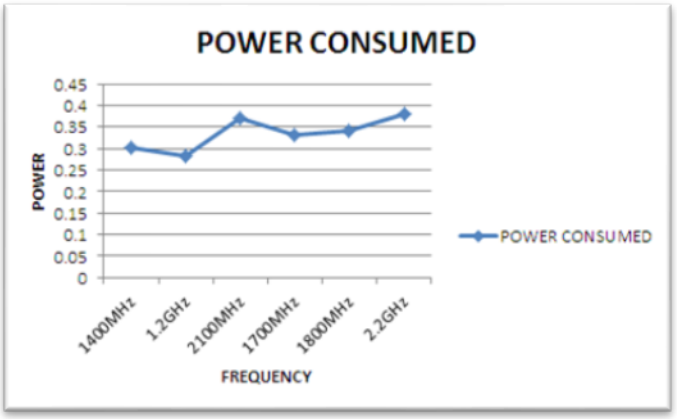

Figure 4. Power Analysis for HSTL_II IO STANDARD

C. Power Analysis for HSTL_I_18 IO STANDARD

Table 5. Power Analysis for HSTL_I_18 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.367
1.2GHz	0.334
2100MHz	0.481
1700MHz	0.416
1800MHz	0.433
2.2GHz	0.499

There is 33.06% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 5 and Table 5.

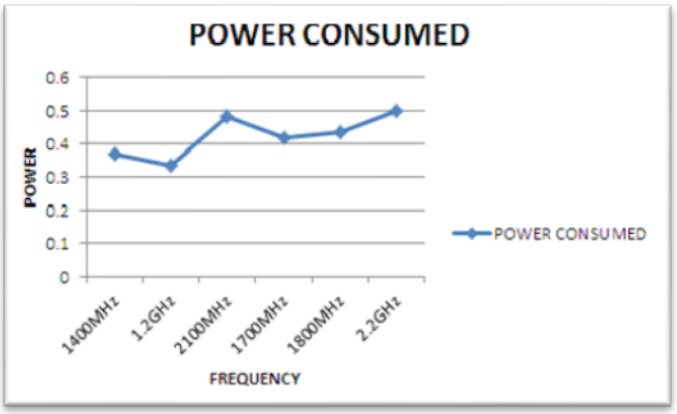

Figure 5. Power Dissipation for HSTL_I_18 IO STANDARD

D. Power Analysis forHSTL_II_18 IO STANDARD

Table 6. Power Analysis for HSTL_II_18 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.357
1.2GHz	0.336
2100MHz	0.429
1700MHz	0.388
1800MHz	0.399
2.2GHz	0.441

There is 23.80% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 6 and Table 6.

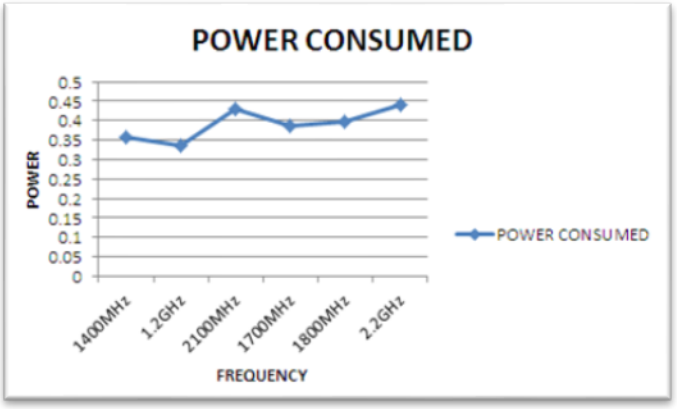

Figure 6. Power Analysis for HSTL_II_18 IO STANDARD

E. ***Power Analysis for HSTL_I_12 IO STANDARD***

Table 7. Power Analysis for HSTL_I_12 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.241
1.2GHz	0.222
2100MHz	0.305
1700MHz	0.268
1800MHz	0.276
2.2GHz	0.314

There is 29.29% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 7 and Table 7.

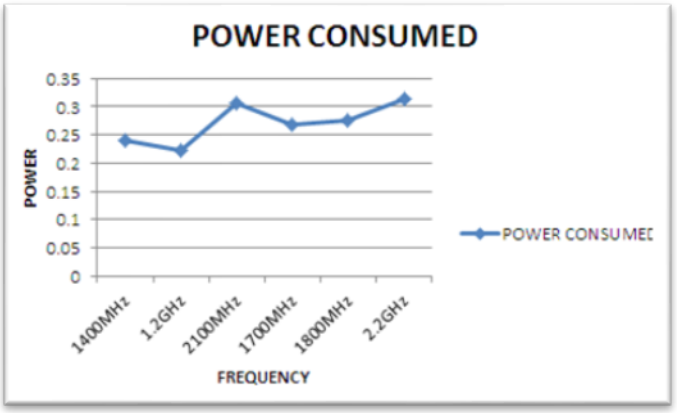

Figure 7. Power Analysis for HSTL_I_12 IO STANDARD

F. Power Analysis for different IO STANDARD with Different Frequencies

Table 8: Power Analysis for HSTL Family at Different Frequencies

IO STANDARD	1400 MHz	1.2 GHz	2100 MHz	1700 MHz	1800 MHz	2.2 GHz
HSTL_I	0.311	0.283	0.407	0.352	0.366	0.422
HSTL_II	0.303	0.283	0.370	0.332	0.342	0.381
HSTL_I_18	0.367	0.334	0.481	0.416	0.433	0.499
HSTL_II_18	0.357	0.336	0.429	0.388	0.399	0.441
HSTL_I_12	0.241	0.222	0.305	0.268	0.276	0.314

There is 34.33%, 33.92%, 36.59%, 35.57%, 36.25%, 37.07% saving in power dissipation with HSTL_I_12 when compared with HSTL_II at 1400 MHz,1.2 GHz, 2100MHz, 1700MHz, 1800 MHz and 2.2 GHz respectively as shown in Figure 8 and Table 8.

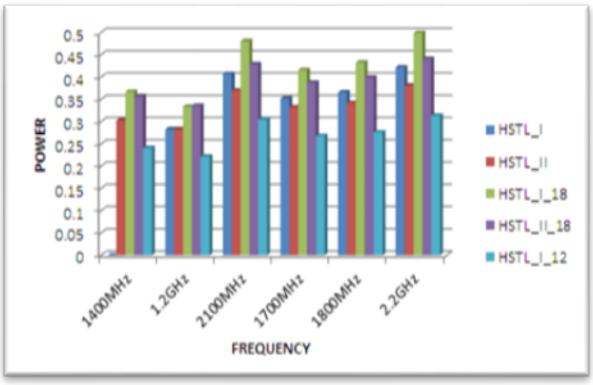

Figure 8. Power Analysis for HSTL Family at Different Frequencies

3. Conclusion

In this research work, we have designed an FIR Gaussian low pass filter in 28nm Kintex-7 FPGA. The design is low power energy efficient and the code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family. FIR Filter design consists of three inputs and one output. The three inputs are input data that is 8 bit or 1 byte, clock and reset. The output is 18 bits wide. The design is tested by varying frequencies at different SSTL IO STANDARDS at constant temperature that is 25 degree Celsius and also keeping air flow constant. We can conclude that there can be 23-33% saving of total power dissipation by using frequency scaling technique.

4. Future Scope

The future scope of "HSTL IO Standard Based Energy Efficient FIR Filter Design on 28nm FPGA"is that we can also implement this design on 22nm or 18 nm FPGA. We can also use different FPGA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive

Spartan 3E, automotive Spartan6, Spartan3, Spartan3E.Here, we are using frequency scaling in which we are changing the operating frequency of a device and analyzing its power. We can redesign this device with other energy efficient technique like capacitance scaling, thermal scaling, clock gating,various design goals, impedance matching with different logic family, and mapping. Analysis has been done with different frequencies like 1400 MHz, 1.2 GHz, 2100 MHz, 1700MHz, 1800MHz, 2.2GHz. We can use any other frequency range and test our design on that also. The temperature has been kept constant that is 25 degree Celsius so if needed it can also be varied. Air flow can also be varied when required.

References

[1] en.wikipedia.org/wiki/Finite_impulse_response
[2] D. Yagain and K. A. Vijaya, "FIR filter design based on retiming automation using VLSI design metrics", Technology, Informatics, Management, Engineering, and Environment (TIME-E), 2013 International Conference on. IEEE, **(2013)**.
[3] G. Jinding, H. Yubao and S. Long, "Design and FPGA implementation of linear FIR low-pass filter based on Kaiser window function", Intelligent Computation Technology and Automation (ICICTA), 2011 International Conference,. vol. 2, **(2011)**.
[4] D. Dencun, W. Wenqi and Z. Shujing, "A new method for design 2-D FIR highpass and bandstop digital filters", Industrial Electronics, 1992., Proceedings of the IEEE International Symposium, IEEE, **(1992)**.
[5] R. Kar, "Optimization of linear phase FIR band pass filter using particle swarm optimization with constriction factor and inertia weight approach", Industrial Electronics and Applications (ISIEA), 2011 IEEE Symposium, **(2011)**.
[6] B. Pandey, "Capacitance scaling based energy efficient FIR filter for digital signal processing." Optimization, Reliabilty, and Information Technology (ICROIT), 2014 International Conference on. IEEE, **(2014)**.
[7] C.-T. Hsieh and S. P. Kim, "A highly-modular pipelined VLSI architecture for 2-D FIR digital filters", Circuits and Systems, 1996., IEEE 39th Midwest symposium, vol. 1, **(1996)**.
[8] P-C. Wu, L-G. Chen, and T-D. Chiueh, "Scalable implementation scheme for multirate FIR filters and its application in efficient design of subband filter banks", IEEE transactions on circuits and systems for video technology, vol. 6, no. 4, **(1996)**, pp. 407-410.
[9] K. Fushinobu and T. Hatakeyama, "Thermal scaling consideration of Si MOSFETs with gate length typically larger than 100 nm", Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2011 27th Annual IEEE. IEEE, **(2011)**.
[10] Y. Zhang, "Automatic Register Transfer level CAD tool design for advanced clock gating and low power schemes", SoC Design Conference (ISOCC), 2012 International. IEEE, **(2012)**.
[11] Z. Liu and Z. Wang, "Analysis to Goal-Driven Design."
[12] T. Kumar, "Simulation of voltage based efficient fire sensor on FPGA using SSTL IO standards", Robotics and Emerging Allied Technologies in Engineering (iCREATE), 2014 International Conference on. IEEE, **(2014)**.
[13] B. Pandey and G. Singh, "Simulation of CMOS IO Standard Based Energy Efficient Gurmukhi Unicode Reader on FPGA", IEEE 6th International Conference on Computational Intelligence and Communication Networks (CICN), Bhopal, **(2014)**.
[14] M. L. George, G. S. Tomar, "Hardware Implementation of Adaptive-Differential Pulse Code Modulation Speech Compression Algorithm", International Journal of Smart Device and Appliance, vol.2, no.2, **(2014)** , pp.1-10.
[15] P. Zahradnik, B. Simak, and M. Vlcek, "Fast design of 2D extremely narrow bandstop FIR filters", Circuits and Systems, 2004. MWSCAS'04. The 2004 47th Midwest Symposium, vol. 2, **(2004)**.

