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Wideband Active-RC Channel Selection Filter for 5-GHz Wireless LAN

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Abstract

An active-RC channel selection filter for wireless LAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover from 6MHz to IEEE802.11a (20MHz) including the effect of process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feedforward frequency compensation scheme. The in-band input third-order intercept point (iIP3) is 18dBV at the highest gain mode. The input referred noise is $13nV/\sqrt{Hz}$ *at the lowest gain mode. Implemented in a* $0.25\mu m$ *CMOS technology, the filter operates with 2.5V supply voltage, consuming 9mA*

Keywords*: Channel selection filter, active-RC, CMOS, Wireless LAN*

1. Introduction

Recently, the interests for wireless local area network (WLAN) has been increasing due to its nature of user convenience and adaptability to newly emerging wireless standards. In WLAN, almost all the important radio characteristics are defined by the software stack in DSP. Nonetheless, RF front-end including low noise amplifier (LNA), mixer, and channel selection filter are required to relieve the burden of analog-to-digital converter (ADC) and DSP as shown in Fig. 1 which is the conceptual block diagram of WLAN with direct conversion receiver (DCR) architecture. Among various architectures of RF front-end, direct conversion architecture seems to be the optimum choice for WLAN because of its simplicity, the lack of intermediate frequency (IF) stages, and low power dissipation. RF front end with DCR architecture can be far simpler if ADC has sufficiently large dynamic range so the channel selection filter can be eliminated [1-4]. However, the power consumption would become extremely large because ADC is normally a power hungry device. The challenge of analog channel selection filter for WLAN is the fact the channel bandwidth can vary in a very wide frequency range depending on the wireless standard. The simplest approach is to have a channel selection filter whose cut-off frequency is fixed at the value for the wireless standard with widest channel bandwidth among the standards being supported. Then, the information is not lost in the channel selection filter even for the other wireless standards. However, the performance requirements of ADC such as dynamic range and effective resolution become stringent [5]. Therefore, the cut-off frequency of channel selection filter should be tunable depending on the channel bandwidth of each wireless standard. Several research results on dual-mode analog channel selection filter have been reported [6-7], but to the authors' knowledge there has been no true software definable channel selection filter tunable for multiple wireless standards.

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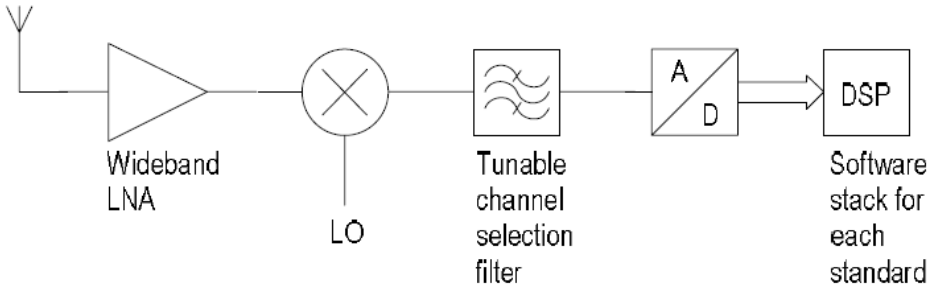

Figure 1. Direct-Conversion RF Front-end Architecture of WLAN

In this paper, an active-RC channel selection filter for WLAN application is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover IEEE802.11a (20MHz) and process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feedforward frequency compensation scheme. Implemented in a 0.25μm CMOS technology, the channel selection filter operates with 2.5V supply voltage, consuming 9mA. The measurement results are given in this paper.

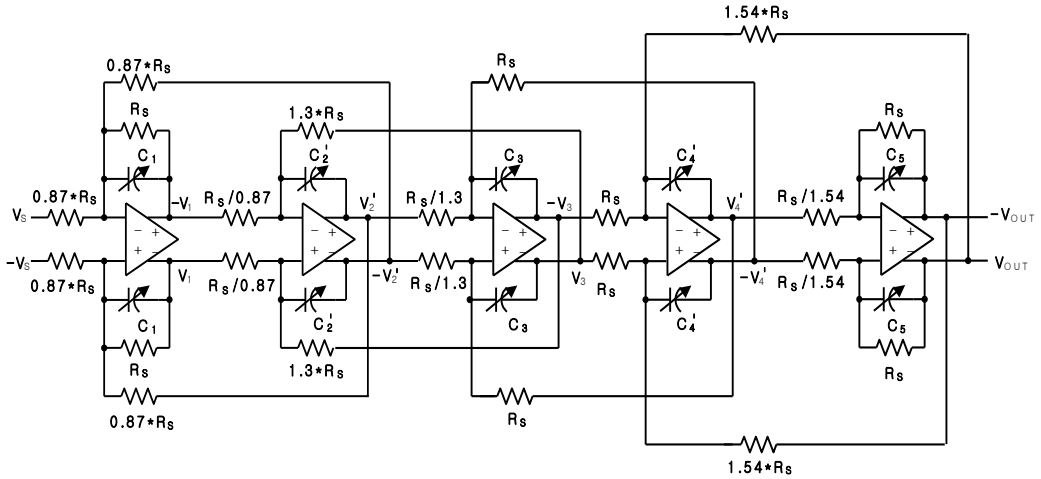

Figure 2. Fifth-order Chebyshev Active-RC Filter Whose Dynamic Range is Optimized by Voltage Scaling

2. Active-RC Channel Selection Filter with Fully-differential R-2R Ladder for WLAN

2.1. Fifth-order Chebyshev Active-RC Filter

Although the detailed frequency characteristics of channel selection filter may be different for each wireless standard in WLAN, a fifth-order Chebyshev filter as shown in Figure 2. has been chosen because it provides relatively large stopband attenuation with moderate group delay variation in passband. If equalized group delay is desired, all pass filter built with the same circuitry may be cascaded after the Chebyshev filter. For maximum dynamic range, the internal node voltages are scaled as shown in Figure 2. The dynamic range of the filter is maximized by scaling the resistor values to have the same

maximum signal swing for all internal nodes. The filter's element values after voltage scaling is shown in Table 1. The cut-off frequency is tunable in a very wide frequency range by employing differential R-2R ladder which is explained below.

Table 1. Voltage Scaling Element Values

Rs	10KΩ
C1	2.0711pF
C2	2.4763pF
C3	3.5668pF
C4	2.4763pF
C5	2.0711pF

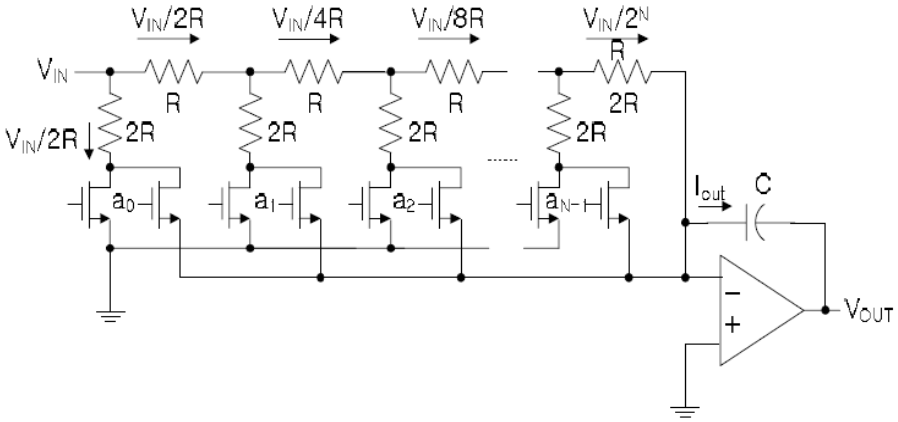

Figure 3. Single-ended Active-RC Integrator with R-2R Ladder

2.2. Differential R-2R Ladder

The cut-off frequency of active-RC filter can be tuned by varying the unity-gain frequency of active-RC integrators. Since the transfer function of active-RC integrator is given by-1/*sCR*, the cut-off frequency can be changed by either variable capacitor or resistor. If the maximum cut-off frequency *fmax* is *M*fmin* and variable capacitor (resistor) is used for frequency tuning, the maximum and minimum capacitances (resistances) are *M*Cmin* (*M*Rmin*) and *Cmin* (*Rmin*), respectively. Therefore, the required silicon area is proportional to *M* which can be a very large number for WLAN and about 3,000 for our work. In order to minimize the silicon area, differential R-2R ladder is used for frequency tuning. If R-2R ladder is used in active-RC integrator as shown in Figure 3, the output current is given as;

$$I_{out} = \frac{V_{in}}{R}\left(\sum_{i=0}^{N-1}\frac{a_i}{2^i} + \frac{1}{2^{N-1}}\right) \quad (1)$$

and thus its frequency response is ;

$$\frac{V_{in}}{V_{out}} = -\frac{1}{sCR}\left(\sum_{i=0}^{N-1}\frac{a_i}{2^i} + \frac{1}{2^{N-1}}\right) \quad (2)$$

From the above equation, we can see the effective resistance is ;

$$R_{eff} = R \Big/ \left(\sum_{i=0}^{N-1} \frac{a_i}{2^i} + \frac{1}{2^{N-1}} \right) \tag{3}$$

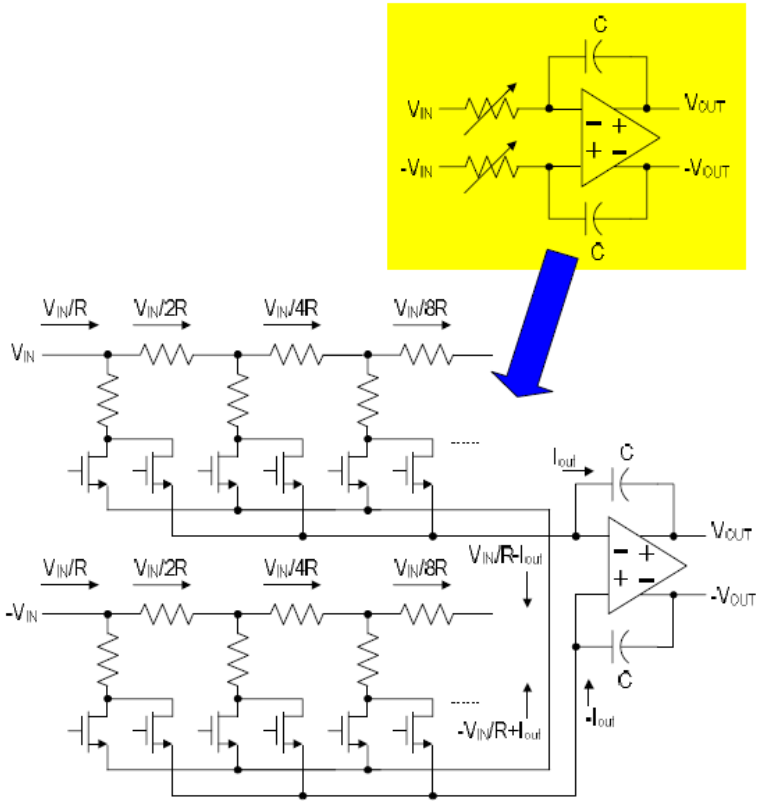

Figure 4. Active-RC Integrator Whose Unity-Gain Frequency is Tunable in a Wide Range by Employing a Differential R-2R Ladder

If *N*-bit R-2R ladder is used, the maximum and minimum resistances are 2*N*-1**R* and *R*, respectively. Therefore, the ratio of the maximum and minimum cut-off frequency is 2*N*-1. For *fmax=M*fmin*, the required number of bits of R-2R ladder is *N*=(log*M*/log2)+1, that is, the silicon area is proportional to log*M* instead of *M*. To apply the R-2R ladder to fully differential active-RC filter, differential integrator is implemented as shown in Figure 4. In single-end R-2R ladder, unselected currents are bypassed to ground, but if the same method is used for differential R-2R ladder, another supply voltage (VDD/2) is required. To avoid the use of additional supply voltage, the unselected differential currents are merged together and due to its fully differential nature, they are cancelled out at the merging node as shown in Figure 4. This can be understood that the merging node acts as virtual ground effectively.

2.3. Operational Amplifier

The DC gain, unity-gain frequency, and the phase shift at the unity-gain frequency are the most important performance parameters of integrator. All these performance parameters are mainly determined by op-amp used for active-RC integrator. Thus, the DC gain and bandwidth of op-amp should be as large as possible. Unfortunately, more power must be dissipated for larger DC gain and bandwidth with widely used conventional Miller frequency compensation. In order to alleviate this issue of Miller compensation, a left half plane (LHP) zero can be generated by a feedforward signal path to compensate the phase shift due to parasitic pole [8]. The feedforward signal path, however, results in additional power dissipation. The op-amp used in this work shown in Fig. 5 employs current re-using technique in feedforward signal path in order to avoid the additional power dissipation [9]. The op-amp of this work employs feedforward frequency compensation method whose transfer function is given as;

$$H(s) = -\frac{g_{m1}r_1 g_{m2}r_2 + g_{m3}r_2 + sC_1 r_1 g_{m3}r_2}{(1+sC_1r_1)(1+sC_2r_2)} = -(A_1A_2 + A_3)\times\frac{1+s/z_1}{(1+s/p_1)(1+s/p_2)} \quad (4)$$

where $A_1=g_{m1}r_1$, $A_2=g_{m2}r_2$, $A_3=g_{m3}r_2$, $p_1=1/C_1r_1$, $p_2=1/C_2\,r_2$, and z_1 is given as ;

$$z_1 = p_1\left(1+\frac{A_1A_2}{A_3}\right). \quad (5)$$

From the above equations (4) and (5), the phase shift of the poles can be compensated with a left-half plane zero whose position can be varied by controlling A_3. In Figure 5, the op-amp employing the feedforward frequency compensation scheme is shown. In order to save the current consumption, the differential pair (M6 and M7) generating g_{m3} is re-using the bias current of g_{m2} [9].The bias current of the second stage, transistors M11 and M12, is re-used in the feedforward signal path formed by the transistors M9 and M10. The HSPICE simulation results including all the parasitic capacitance indicate 77dB DC gain and 870MHz unity gain frequency with 1pF load capacitance. The phase margin is simulated to be 56° as shown in Figure 6.

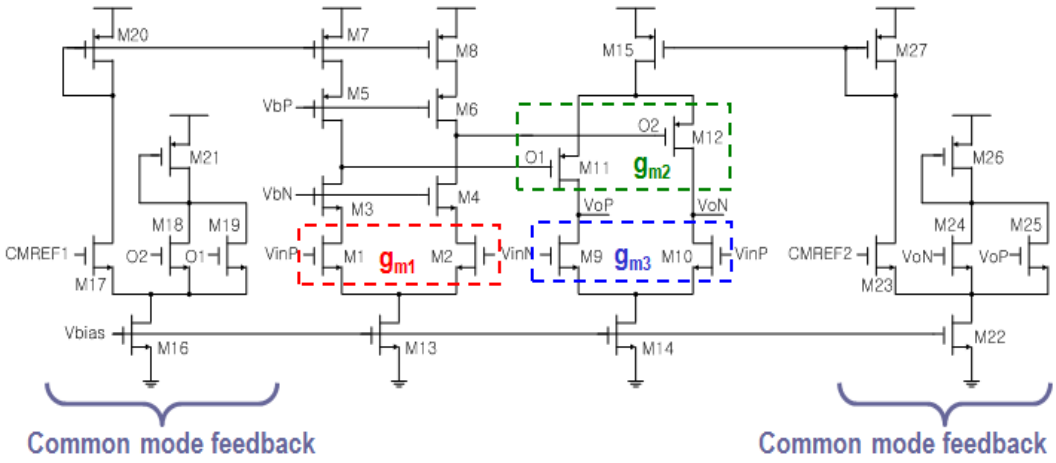

Figure 5. Fully Differential op-amp Whose Frequency Response is Compensated by the Current Re-using Feedforward Frequency Compensation Method

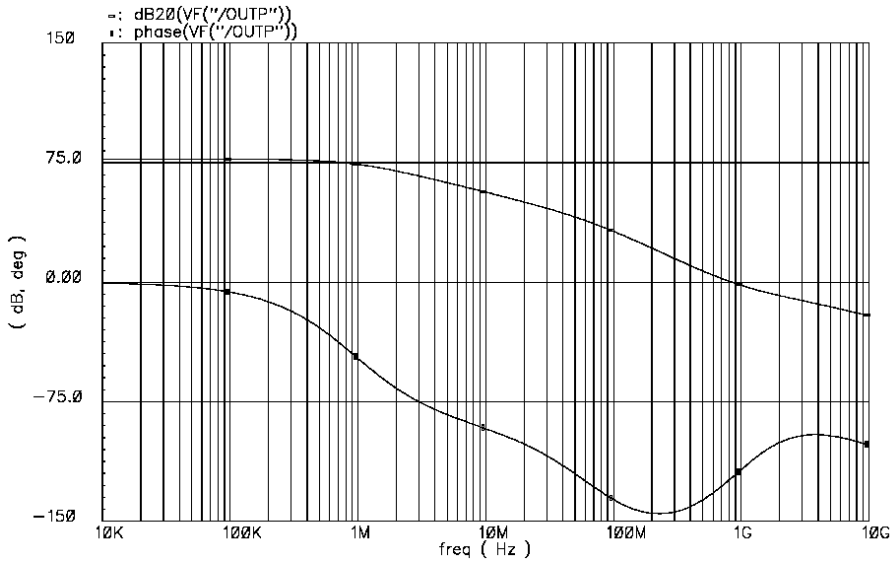

Figure 6. Frequency Response of the op-amp with All Parasitics Included

3. Measurement Results

The filter is designed with a 0.25μm CMOS technology and its layout is shown in Figure 7. In order to include the effects due to parasitic capacitance and resistance. Implemented in a 0.25μm CMOS technology has been performed. The filter operates with 2.5V supply voltage, consuming 9mA. The frequency response for some R-2R ladder control codes shown in Figure 8 measures the cut-off frequency is tunable from 6MHz to 20MHz. The passband ripple is smaller than 0.5dB while the stopband is attenuated by more than 41dB. The linearity of the filter is checked by the third order input intercept point (iIP3) for both in-band and out-of-band signal (see the Figure 9) and the second order input intercept point (iIP2) for out-of-band signal. The measured results of the linearity are summarized in Table II with other performance parameters.

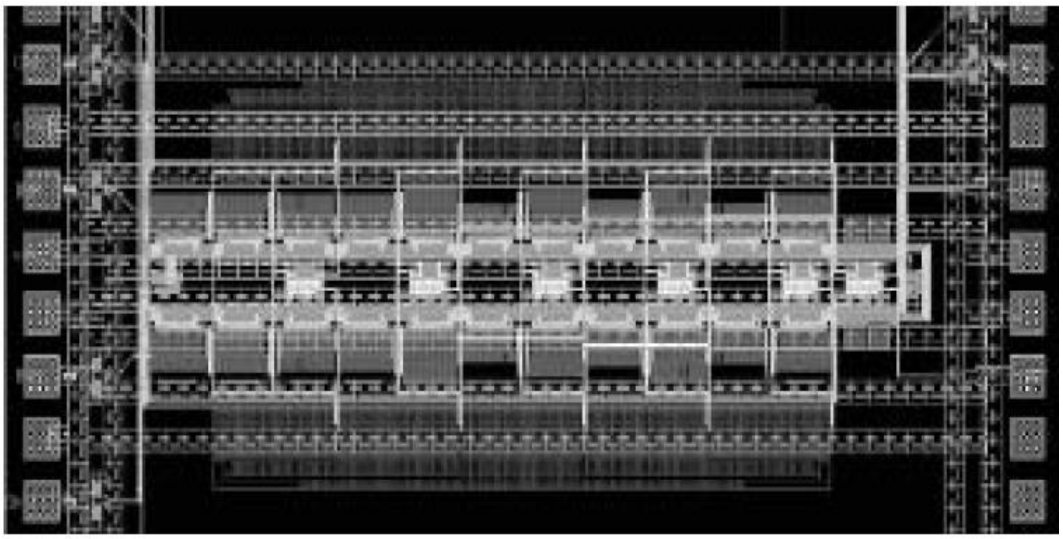

Figure 7. Layout of the Active-RC Channel Selection Filter

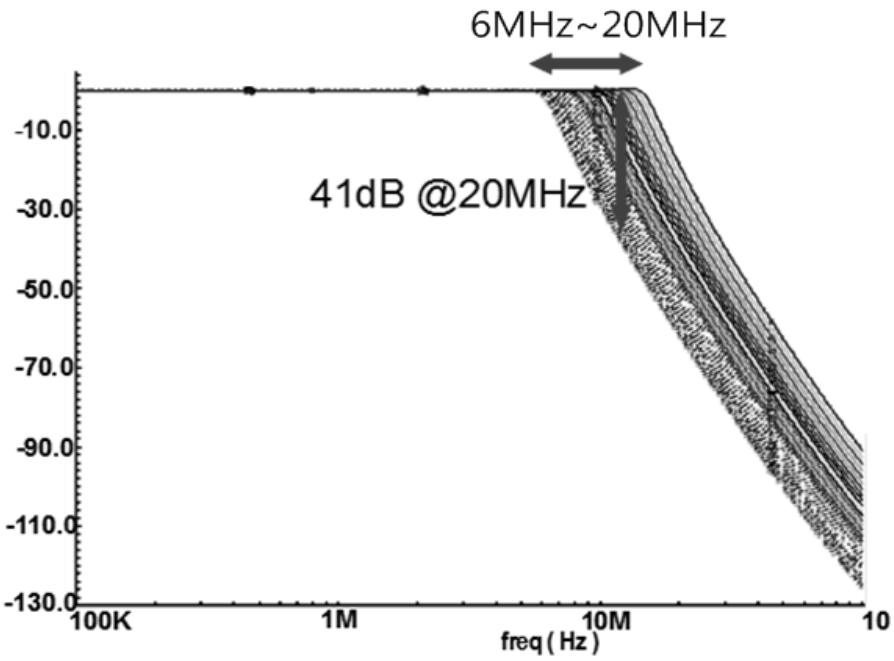

Figure 8. Frequency Response of the Filter for Some R-2R Control Codes

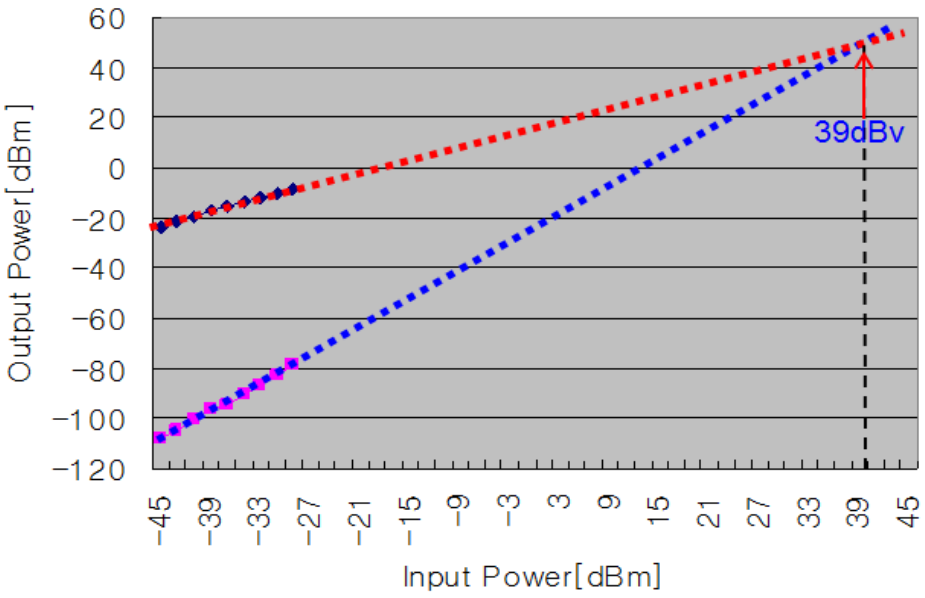

Figure 9. Measured Out-of Band iIP3 of CSF

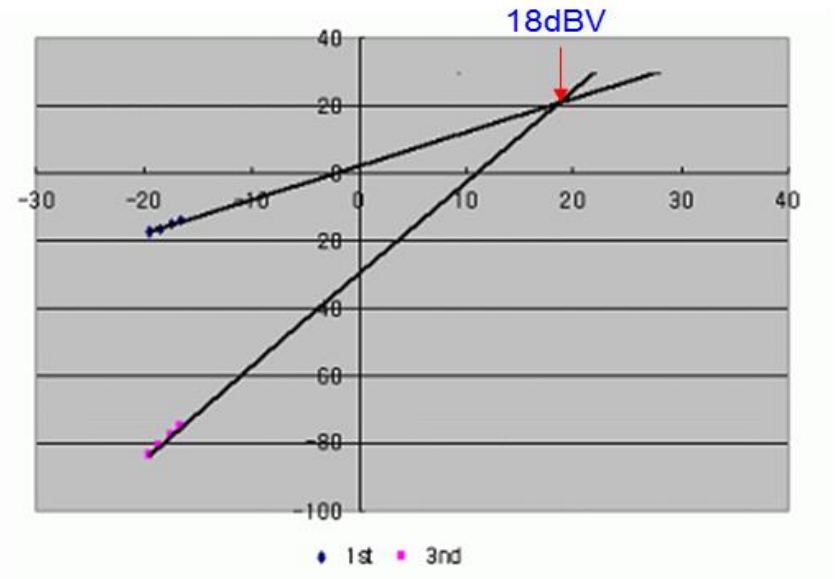

Figure 10. Measured in-Band iIP3 of CSF

Table 2. Measured Performance Summary of the Filter

Process	0.25μmCMOS
Current consumption	9mA @2.5V
Tunable range of cut-off frequency	6MHz~20MHz
Passband ripple	< 0.5dB
Stopband attenuation	>41dB
iIP3(in-band)	18dBV
iIP3(out-of-band)	39dBV
iIP2(out-of-band)	72dBV

4. Conclusion

This paper describes a CMOS active-RC channel selection filter for for 5GHz wireless LAN. An active-RC channel selection filter for WLAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover IEEE 802.11a (20MHz) including the effect of process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feedforward frequency compensation scheme. The in-band input third-order intercept point (iIP3) is 18dBV at the highest gain mode. The input referred noise is $13\text{nV}/\sqrt{\text{Hz}}$ at the lowest gain mode. Implemented in a 0.25μm CMOS technology, the filter operates with 2.5V supply voltage, consuming 9mA..

Acknowledgements

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