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LDPC Code Based on Cyclic Shift Register Structure

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Abstract

The non-rule circulates LDPC code is the core of the forward-acting error correction code of our country digital television broadcasts in ground DTMB transmission standard. In view of sub block characteristic of this LDPC code generates matrix. It has designed a kind of LDPC encoder based on the linear feedback shift register structure to achieve the LDPC real-time encoding under three different code rates. The whole design occupies 4699 ALUTs, it shorten 20% logical resources compared with same designable project. It fits low complexity DTMB standard transmitter to develop.

Keywords: *circulation of the shift register; encoder; cycle LDPC codes; real-time coding*

1. Introduction

Low density parity check code (LDPC) is a sparse parity check matrix of a linear block code based. LDPC code is a packet-error-correcting codes having a sparse parity check matrix of the Massachusetts Institute of Technology Robert Gallager in 1962 doctoral thesis presented in [1]. Suitable for almost all of the channel, thus becoming coded circles in recent years, the research focus. Its performance approaching Shannon limit, and the description and easy to implement theoretical analysis and research, coding is simple and can be implemented in parallel operation, suitable for hardware implementation. Otherwise the research production was ignored by people over a long period of term untio 1996. Mackay find strong performance of LDPC code again. From then, LDPC code becomes a main research hot point of information channel Golay code. LDPC code has big performance of error correction [2]. For example, S.Y.Chung designed 1/2 code rate, code of the rules of the 107 LDPC code under the binary system inputs the AWGN channel, when the probability of error from 106 at shannon limit only 0.00455 DB[3], this is the limitation of the performance of any code close to Shannon.

In August 2006, our country digital TV broadcasting the transport standard DTMB is promulgated formally. Through the efforts of many experts, DTMB standard in the December 6, 2011, and eventually became the fourth ITU terrestrial digital TV standard. We have completed two proposals ITU ITU-R BT.1306-6 and ITU-RBT.1368-9 book, and that the two proposals has been officially revised and released.The forward error correction of DTMB standards is concatenated by BCH code and LDPC, was applied three code rate of 0.4、0.6、0.8.. The LDPC codes are QC-LDPC not rule code. They have block cycle features of check matrix and generated matrix, each blockette is zero matrixes and cyclic matrix to low the complexity of compiled coding, while still maintaining good performance of LDPC error correction.

With good performance, the coding complexity of LDPC code higher than general linear block code, and to achieve better capability[4]. Many of check matrixes of LDPC code is by computer random structure and corresponding code and generally much long (to tens of thousands of thousands of bits). If we used Gaussian elimination methods to make check matrix and calculate the checksum bit, the corresponding operating amount

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and yards, and even medium-sized proportional to the square yards of coding used for hardware and implementation[5], so we must use its low complexity coding program.

The article aims at the must cycle features of LDPC code in DTMB standard based on the circulation of the shift register structure to achieve three different rates of the DTMB standard code. The whole design layout lines and synthesize the FPGA chip. The clock achieves at 182. 82 MHz has far exceeded DTMB real-time coding requirements, and the design has a strong universal property. It only need change the interior of the days to a polynomial record module, it can apply to any QC-LDPC coding.

2. LDPC Code Based on Cyclic Shift Register Structure

In the DTMB standard, The input data bit stream after scrambling into the FEC processing module. The forward error correction is achieved by BCH code connect with LDPC code.

DTMB standard provides for three types of FEC code rate, corresponding to the LDPC code rate there are three types of LDPC (7493, 3048) code; LDPC (7493, 4572) code; and LDPC (7493, 6096) code; in the LDPC code FEC code word as the output, delete the previous five parity bit, so in fact the output is only 7488 bits.

Three types of LDPC code detailed arguments.

Table 1. DTMB Standard LDPC Cose Arguments

model	LDPC code	k	c	b
0.4 code rate FEC	LDPC(7493, 3048)	24	35	127
0.6 code rate FEC	LDPC(7493, 4572)	36	23	127
0.8 code rate FEC	LDPC(7493, 6096)	48	11	127

3. Based on the Structure of the LDPC Cyclic Shift Register Encoder

Quasi-cyclic Low Density Parity Check (QC- LDPC) code is a LPPC code, its generator matrix and parity check matrix have quasi-cyclic characteristics. QC- LDPC coding can be used to complete the shift register, the address decoder available counters and easy part of the parallel implementation, DTMB standard channel coding using QC-LDPC codes., DTMB used in the QC-LDPC codes are the system codes, parity bits in the former, the information bits in the post, all of the three sub-block size of the bit rate are 127 × 127. If the code generator matrix of the time to take advantage of cyclical nature of sub-blocks, even if the generator matrix is not sparse, which also can be done under low complexity LDPC codes [6], the following details of the encoding process.

3.1. QC-LDPC Coding Algorithm

On the QC-LDPC code generation matrix (such as formula (1) as shown in the form), the sub-matrix Gi,j with the cyclic shift properties, just recorded its first line of data gi,j can be obtained by the sub-matrix Gi,j, it said gi,j for the polynomial matrices, so the whole generator matrix Gqc can be described fully by c × (tc) a generator polynomial gi,j.

Write a = (a1, a2, .., a (tc) b) to be encoded information bits, which can be divided in accordance with sub-block size (t-c) sub-vector (a1,a2,..,a(t-c)), which ai=(a(i-1)b+1, a(i-1)b+2,..,aib), $1 \leq i \leq (t-c)$. Under the theory of linear block codes, the corresponding encoding codes of information bits a are:

$$\boldsymbol{v} = \boldsymbol{a} * \boldsymbol{G}_{qc} = (\boldsymbol{p}_1, \boldsymbol{p}_2, \cdots \boldsymbol{p}_c, \boldsymbol{a}) \qquad (1)$$

On where, pj=(pj,1, pj,2,…pj,b) is the parity bit of the first sub-vector j, 1≤ j≤ c, the knowledge can be obtained by matrix multiplication:

$$\boldsymbol{p}_j = \boldsymbol{a}_1\boldsymbol{G}_{1,j} + \boldsymbol{a}_2\boldsymbol{G}_{2,j} + \ldots + \boldsymbol{a}_{t-c}\boldsymbol{G}_{t-c,j} \quad (2)$$

Let $\boldsymbol{g}_{i,j}^{(l)}$ becomes generator polynomial gi,j of Gi,j and cyclic right rotate l bit, and then:

$$\boldsymbol{a}_i\boldsymbol{G}_{i,j} = a_{(i-1)b+1}\boldsymbol{g}_{i,j}^{(0)} + a_{(i-1)b+2}\boldsymbol{g}_{i,j}^{(0)} + \ldots + a_{ib}\boldsymbol{g}_{i,j}^{(b-1)} \quad (3)$$

At this point, we can see that, with the input information bits (a1,a2,.., a(t-c)) to enter the serial encoder, the j parity bit sub-vector pj can be completed by equation (3), (4). When the ai into the encoder, first of all, according to the formula (4) completed aiGi,j operations, the type can be easily used implementation of linear feedback shift register structure, and then calculate Sj=a1G1,1+ aiGi,j+…+aiGi,j. And when a(t-c) all entered the encoder, then Sj=a1G1,1+ aiGi,j+…+at-cGt-c,j, exactly it's the j parity bit sub-vector pj, so if encoder contains c pj parallel computing modules, you can read all the information in bits parity bits after the completion of all calculations, the only store c×(t-c) generator polynomial gi,j information within the encoder.

3.2. Design Requirements

Coder design needs to be able to complete all three DTMB standard real-time encoding LDPC codes. Three information bit length of the LDPC codes were 3048, 4572 and 6096 bits are 7493-bit code length, but not in front of five parity bit output, only the output bit to the back of 7488.

Using the above QC-LDPC codes algorithm, the input is completed in all information bits at the same time to calculate all the parity bits, and then remove the front five of the parity bits and information bits to form a complete code word output of the serial form, which takes 7488 clock cycles, while the maximum length of the input information bits 6096 bits. Work to improve the stability of the system, using single-clock design, input / output are a serial mode, and each with a separate Data_Valid signal. First of all, we should determine the encoder clock frequency, in accordance with the provisions of DTMB standard, the system load was the highest net 32.486Mbps (FEC rate corresponding to 0.8 modes). We know at this time LDPC codes and the code word bits of information bit rate, respective for: 32.486*762/752 =32.918Mbps 和 32.486*7488/6016=40.435Mbps. To leave some margin, select the 45MHz operating clock for the encoder.

3.3. LDPC Encoder Design

The core of the encoder are shift register the adder- accumulator structure (Shift-Register-dder- Accumulator, SRAA), which can be completed formula (3), (4) calculation of parity bits as shown, the specific structure is as following:

It can be seen, the SRAA composed by the two sets of register array, the top of the register B array Reg_B, the below one is the register A formation Reg_A which the width of both sub-block size 127.The initial state, the register array A, B contents of all clear. To start coding, at first let the generating polynomial g0,0 of the sub-block G0,0 of generator matrix G load into register B, then the first information bit s0 appears at the input, s0 and Reg_B phase deal with the gate array appear the array of the input. In GF(2) domain of addition and visional arithmetic is equivalent, due to the initial content Reg_A is zero, we can see the updated Reg_A value is for:.

$$\mathrm{Reg\_A} = s_0 * \boldsymbol{g}_{0,0} \quad (4)$$

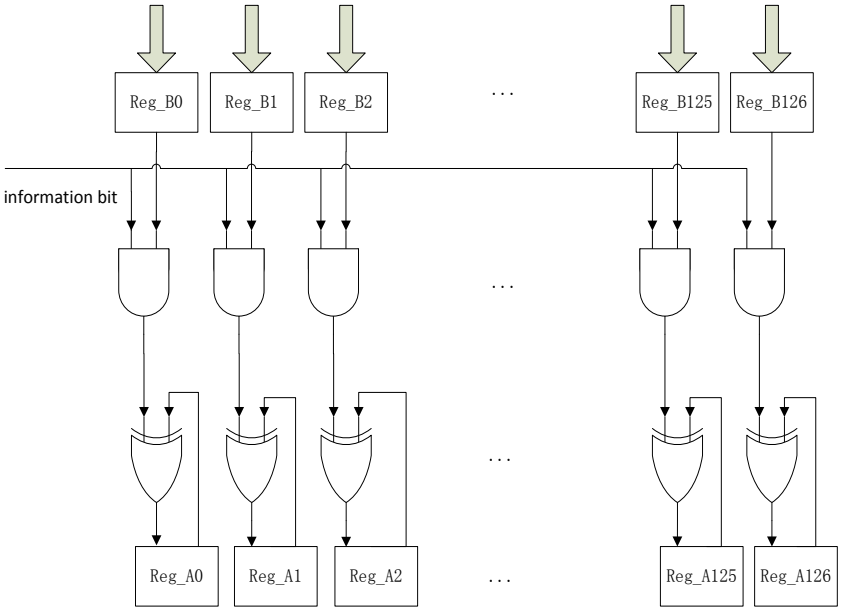

Figure 1. SRAA Structure Chart

The next clock cycle, the second information bit s_1 appears at the input, Reg_B content cycle right one into the same $g_{0,0}^{(1)}$ with the doors and gate array, the time Reg_A becomes:

$$Reg\_A = s_0 * g_{0,0} + s_1 * g_{0,0}^{(1)} \quad (5)$$

So, in the first 127 clock cycles, Reg_A as:

$$Reg\_A = s_0 * g_{0,0} + s_1 * g_{0,0}^{(1)} + \ldots + s_{126} * g_{0,0}^{(126)} = s_0 * G_{0,0} \quad (6)$$

On where, s0 is the first group of sub-array of the information bits divided by sub-block length 127 (the meaning of s1, s2 as above, write s=(s1, s2,…s t-c)).Since then, Reg_B start loading t the generating polynomial g1,0 of he sub-blockG1,0 and then repeat the operation, after 127 clock cycles, Reg_A as:

$$Reg\_A = s_0 * G_{0,0} + s_1 * G_{1,0} \quad (7)$$

Thus, when all the information bits are input has been completed, the value in the register array A:

$$Reg\_A = s_0 * G_{0,0} + s_1 * G_{1,0} + \ldots + s_{t-c} * G_{t-c,0} = p_0 \quad (8)$$

Thus, a SRAA structure can be complete a calculation sub-block parity bits (including parity bits 127)in the information bit length (t-c)*127 clock cycles, with c set SRAA structure work in parallel. After all information bits completed input to achieve all the parity bits at the same time (the results are stored in Reg_A array), removal of the previous five parity bits, form the other parity bits and remaining bits of the original information to the holistic 7488-bit serial mode output. So we completed the whole process of LDPC codes.

Figure 2 shows the top of DTMB standard LDPC block diagram of the encoder, the encoder structure based on SRAA, the main sub-modules are: Load_sbit, Sbit_FIFO, SRAA array, Gbase_data, Output_code, Main_control.To meet the requirements of real-time encoder with a 3-stage pipeline design: the first stage pipeline ping-pong buffer to

complete the input information bits (information bits from the LDPC encoder maximum transmission rate and the clock shows the work done up to a bit of information transmission takes 8333 clock cycle), the second-level calculation of parity bits to complete (up to 6096 clock cycles time-consuming), the third-level output of the encoding code word (takes 7488 clock cycles).

Hardware encoder with Altera's Stratix II EP2S15 chip series, the following details of each sub-module design.

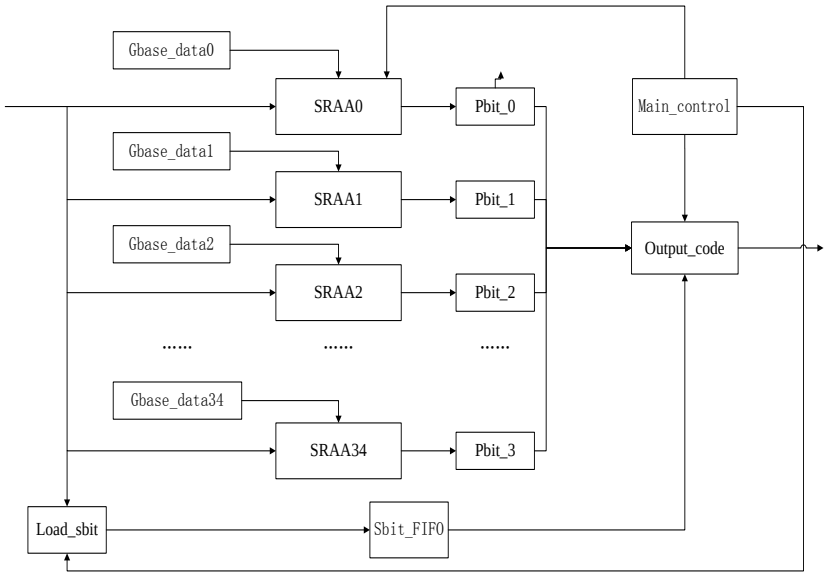

Figure 2. LDPC Encoder Structure Block Based on Cyclic Shift Register Structure

1.Load_sbit module

Load_sbit module completed information bits read-in mainly, the information bits will be read into the buffer within the ping-pong, but also record the corresponding rate information code rate, the ping-pong buffer may be a bit wide for the 1-bit depth of the RAM 16384 composition, its highest level as a ping-pong buffer address switch position.LDPC code word when a transfer is completed, set the corresponding Buf_available signal is high, representing the current ping-pong buffer is available, then SRAA module inside the module can receive Load_sbit ping-pong buffer output information bits, while the next frame of information bits of data has also continued ping-pong buffer to be written, this could make Load_sbit module is always in working condition, reducing system latency.

2.Sbit_FIFO module

Sbit_FIFO mainly used for the cache module sent to the SRAA information bits, when the parity bit calculation is completed, by the code word output module Output_code read information bits in the data FIFO, and with the parity bits into holistic composition of LDPC code word, the module Altera's IP core can be dedicated to achieve generation tool MegaWizard, FIFO data width is a maximum depth of 16384.

3.SRAA module array

SRAA array is the core of the encoder and also the most resource module. In which the internal structure of single SRAA module as described earlier. Three kinds of the DTMB standard LDPC code rate, the corresponding parity bit sub-block length of 35 (0.4 rate FEC mode), 23 (0.6 rate FEC mode), and 11 (0.8 rate FEC mode).Accordingly, the three bit rates needed SRAA are exactly the number required for the 35,23,11. In practice, these

SRAA timing work to accomplish the same array, so the design uses a main SRAA module SRAA0_prior, it's not only the completion of the module under the rate of three sub-block check bit computing, but also has shared SRAA module timing signal for the remaining modules from the SRAA. Different from the SRAA according to the work module can also be divided into three categories, one can support all three bit rates (SRAA0), a class can support 0.4,0.6 rate mode (SRAA1), there is a class only supports 0.4 Bit rate mode (SRAA2).

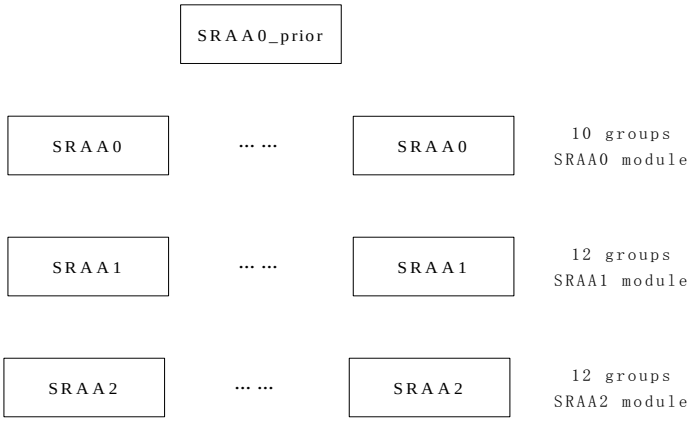

Figure 3. SRAA Array of Parallel Computing

When all SRAA modules are enabled, and SRAA0_prior, SRAA0, SRAA1 rate were set to 0.4 mode, the encoder can be completed LDPC (3048,7492) code; when SRAA0_prior, SRAA0, SRAA1 enabled, SRAA2 disabled and SRAA0_prior, SRAA0, SRAA1 rate set to 0.6 mode, the encoder can be completed LDPC (4572,7492) code; when SRAA0_prior, SRAA0 enabled, SRAA1, SRAA2 disabled and SRAA0_prior, SRAA0 rate set to 0.8 mode, the encoder can be completion of LDPC (6096,7492) encoding. SRAA specific arrangement as shown below:

In the 35 group of SRAA module, SRAA0_prior is at the heart of information bits input polynomial generator matrix sub-block read, parity calculation sub-block, SRAA state update and output functions by the module. Just the other modules from the SRAA SRAA0_prior output timing signals with parity bits can be calculated.

4.Gbase_data module

Gbase_data module was stored sub-block generator matrix of LDPC code generator polynomial, each generator polynomial bits wide is 127 bits. Three kinds of bit-rate required to store the data, 0.4FEC bit rate corresponding to 24 × 35 = 840 G matrix polynomial; 0.6FEC bit rate corresponding to 36 × 23 = 828 G generator polynomial matrix; 0.8 FEC bit rate corresponding to 48 × 11 = 528 G generator polynomial matrix;

Gbase_data modules correspond with SRAA module, so will require a total of 35 groups Gbase_data module, where the first 11 groups need to store all the G-3 bit-rate sub-block columns of generator polynomial matrix, the depth is 24 +36 +48 = 108; among 12 groups depth is 24 +36 = 60; the final depth of 12 groups are 24.By the ROM build, according to an external rate signal different, Gbase_data module can automatically output the corresponding data bit rate of the generator polynomial.

5.Output_code module

When the parity bit calculation is completed, output_code module is completed word output, at first parity bit output data (removal of the previous five parity bits), serial output parity bits to be finished, and then read the information bits in the Sbit_FIFO data, but also to the serial model output, the two with holistic 7488-bit FEC code word. To reduce the output data glitch phenomenon, increase in the output encoded data when the level of register.

6.Main_control module

Main_control module mainly control of each module is enabled, disabled; FIFO data is cleared and identified SRAA operation according to the different rate.

4. The Implementation and Verification of Decoder FPGA

Used RTL-level Verilog HDL code to write the whole design implementation for the platform of EP2S15. The Quartus II 7.2 successfully completed comprehensive and layout of the cabling, wiring up after the maximum operating frequency of 182.82MHz, has far exceeded the DTMB standard clock requirements. After routing the encoder specific resource occupancy shown in Table 2, compared with existing similar design, saving nearly 20% of the hardware resources [7].

Table 2. Decoder Footprint Statistics

Resources	Occupation quantity	Occupation percent
ALUT	4699	10%
Memory bit	357,888 bit	28%

5. Conclusions

DTMB standard uses QC-LDPC codes, corresponded generator matrix has quasi-cyclic shift properties, it can be done directly with generator matrix LDPC code encoder only stores 3 rate LDPC codes under the sub-block generator matrix generated polynomial to the whole array of encoder structure based on SRAA by linear feedback shift register to complete the LDPC codes, the design takes a total of 4699 ALUTs, storage resource consumption is 350Kbit.The encoder can work at 45MHz clock to complete real-time under the DTMB standard LDPC codes, and supports all three kinds of LDPC code rate.

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