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SSTL IO Standard Based Energy Efficient Digital Clock Design on 28nm FPGA

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Abstract

In this paper we have aimed to have an energy efficient digital clock design. Digital clock is a type of clock that displays time digitally. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family using different SSTL IOStandards. Comparison between different SSTL IOStandard has been done to achieve minimum IO power. Via SSTL technology, we achieve green computing with respect to low voltage impedance. In this work we are testing our digital clock design with different SSTL IOStandards such as SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. The design consists of five inputs and six outputs. At th end we concluded that there is 24-35% saving in total power dissipation with 1.2 GHz when compared with 2.2 GHz.

Keywords: *Digital Clock, FPGA, SSTL , IO Standard, Energy Efficient*

1. Introduction

Digital clock is a type of clock that displays time digitally. Earlier time was indicated by the position of rotating hands [1]. In digital clocks the driven mechanism is not digital [1]. The biggest digital clock is the Lichtzeitpegel ("Light Time Level"), Germany [1]. In this paper, we have attempted to design an energy efficient digital clock and the code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family. Nowadays the requirement is for energy efficient devices or the devices that consumes low power to diminish the extra power consumed by the devices. Many attempts have been performed using digital clock. A digital clock design which is based on Nios has also been introduced [2]. Digital designs are suitable for both high-speed clocking and low-voltage applications [3]. Digital methods avoids phase loops or delay line loop which are referred to as analog methods [3]. The objective of this design is to minimize system's dynamic power consumption [4]. Nowadays digital clocks are also present on the rear view mirrors of the vehicles [5]. A general architecture for digital clock for high-speed binary links had also been discussed [6].A paper presents a prototype of a 6- digit digital clock displaying time on a four- digit seven- segment LED module using FPGA (field programmable gate array) [7].Our design of digital clock has been implemented on Xilinx ISE Design Suite 14.2 using different SSTL IOstandards. Comparison between different SSTL IOStandard has been done to achieve minimum IO power. Via SSTL technology, we achieve green computing with

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respect to low voltage impedance [8]. Here we are taking different operating frequencies and testing our digital clock design with different SSTL IOStandards such as SSTL15, SSTL18_II, SSTL135, SSTL12, SSTL18_I.Operating frequencies are listed in Table 3. Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [9]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink.Our design consist of five inputs and six 7 bits output as shown in Figure 1. The outsegh1 and outsegh2 are for hours, outsegm1 and outsegm2 are for hours , outsegs1and outsegs2 are for seconds.

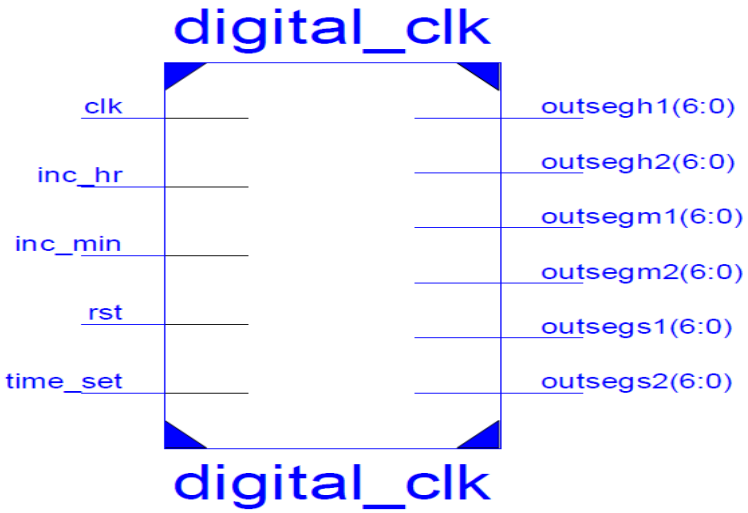

Figure 1. Symbol of Digital Clock

Table 2. Different Parameters in Kintex-7 FPGA

IO pins	676
LUT Elements	101400
Flip Flop	202800
DSPS	600
Available IOBS	400
Gb transceiver	8
Block RAM	325
GTXE2 Transceiver	8
PCI Buses	1.1
MMCMS	8
Min operating temperature	0 degree Celsius
Reference operating temperature	85 degree Celsius
Maximum operating Temperature	85 degree Celsius
Minimum operating voltage	0.97V
Reference operating Voltage	0.97V
Maximum operating Voltage	1.03V
Temperature Grade Letter	C

Our design "digital clock" is based on the Very High Speed Integrated Circuit Hardware Description Language (VHDL) hardware description language, synthesized by the Xilinx Synthesis Technology (XST) synthesizer [7].This design is based on 28nm FPGA and the code has been tested on Kintex-7 and the device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. Table 2 shows different parameters in kintex-7 FPGA.

Table 3. Set of Frequencies Taken In Consideration

Frequency	Mobile set
1400MHz	Nokia Lumia 710
1.2GHz	Samsung Galaxy Core
2100MHz	I phone6
1700MHz	HTC/T
1800MHz	Micromax X091
2.2GHz	Sony Xperia Z1

2. Power Analysis

A. Power Analysis for SSTL15 IO STANDARD

Table 4. Power Analysis for SSTL15 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.354
1.2GHz	0.323
2100MHz	0.461
1700MHz	0.400
1800MHz	0.416
2.2GHz	0.477

There is 32.28% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 2 and Table 4.

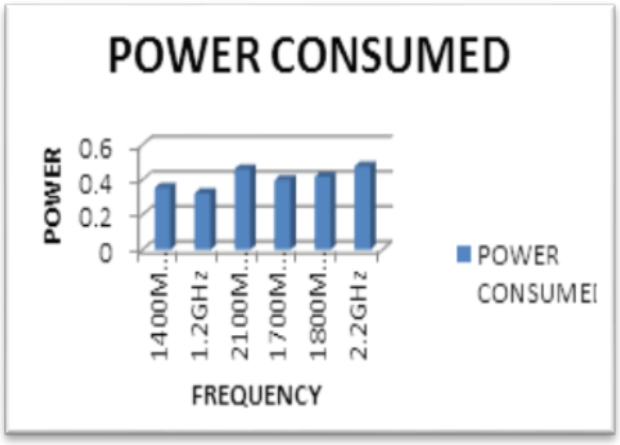

Figure 2. Power Analysis for SSTL15 IO STANDARD

B. Power Analysis for SSTL18_II IO STANDARD

Table 5. Power Analysis for *SSTL18_II IO* STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.631
1.2GHz	0.573
2100MHz	0.836
1700MHz	0.719
1800MHz	0.749
2.2GHz	0.865

There is 33.75% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 3 and Table 5.

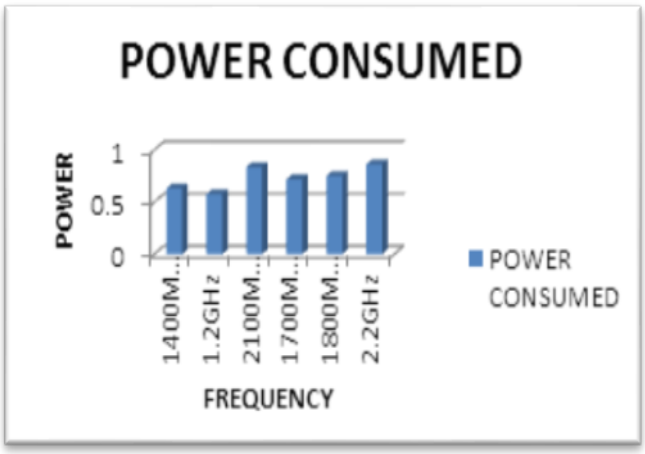

Figure 3. Power Analysis for SSTL18_II IO STANDARD

C. Power Analysis for SSTL135 IO STANDARD

Table 6. Power Analysis for *SSTL135* IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.338
1.2GHz	0.308
2100MHz	0.444
1700MHz	0.523
1800MHz	0.399
2.2GHz	0.460

There is 33.04% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 4 and Table 6.

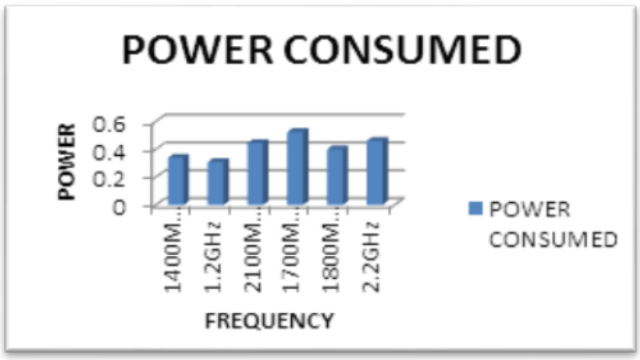

Figure 4. Power Dissipation for SSTL135 IO STANDARD

D. Power Analysis for SSTL12 IO STANDARD

Table 7. Power Analysis for SSTL12 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.218
1.2GHz	0.205
2100MHz	0.264
1700MHz	0.237
1800MHz	0.248
2.2GHz	0.270

There is 24.07% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 5 and Table 7.

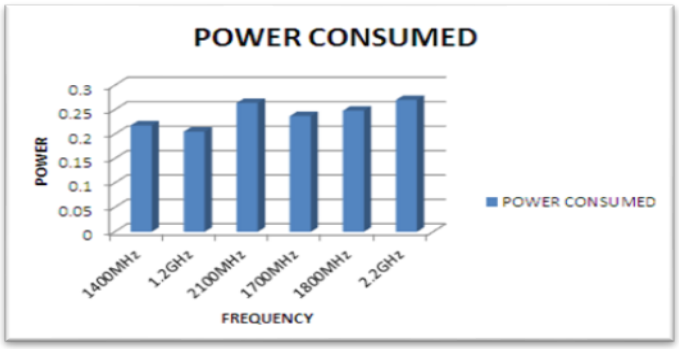

Figure 5. Power Analysis for SSTL12 IO STANDARD

E. Power Analysis for SSTL18_I IO STANDARD

Table 8: Power Analysis for SSTL12 IO STANDARD

FREQUENCY	POWER CONSUMED
1400MHz	0.722
1.2GHz	0.473
2100MHz	0.696
1700MHz	0.598
1800MHz	0.623
2.2GHz	0.722

There is 34.48% saving in total power dissipation with 1.2 GHz when compared with 2.2GHz as shown in Figure 6 and Table 8.

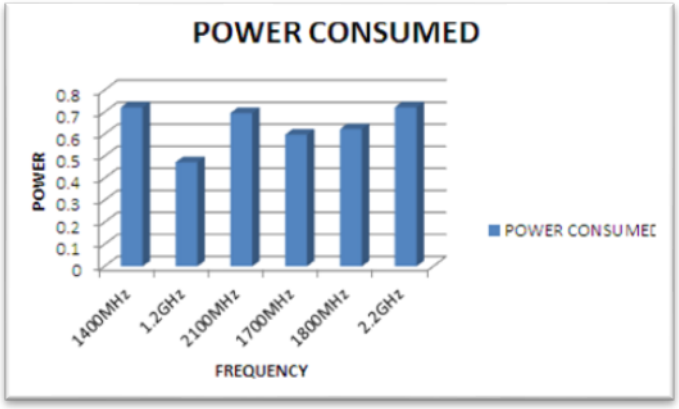

Figure 6. Power Analysis for SSTL12 IO STANDARD

F. Power Analysis for different IO STANDARD with Different Frequencies

Table 9. Power Analysis For SSTL Family At Different Frequencies

IO STANDARD	1400 MHz	1.2 GHz	2100 MHz	1700 MHz	1800 MHz	2.2 GHz
SSTL15	0.354	0.323	0.461	0.400	0.416	0.477
SSTL18_II	0.631	0.573	0.836	0.719	0.749	0.865
SSTL135	0.338	0.308	0.444	0.523	0.399	0.460
SSTL12	0.218	0.205	0.264	0.237	0.248	0.270
SSTL18_I	0.722	0.473	0.696	0.598	0.623	0.722

There is 69.80 % is saving in total power dissipation with SSTL12 when compared with SSTL18_II at 1400MHz.There is 64.22%saving in total power dissipation with SSTL12 when compared with SSTL18_II at 1.2 GHz.There is 68.42% saving in total power dissipation with SSTL12 when compared with SSTL18_II at 2100MHz.There is 67.03% saving in total power dissipation with SSTL12 when compared with SSTL18_II at 1700MHz.There is 66.88% saving in total power dissipation with SSTL12 when compared with SSTL18_II at 1800MHz.There is 68.78% saving in total power dissipation with SSTL12 when compared with SSTL18_II at 2.2 GHz as shown in Figure 7 and Table 9.

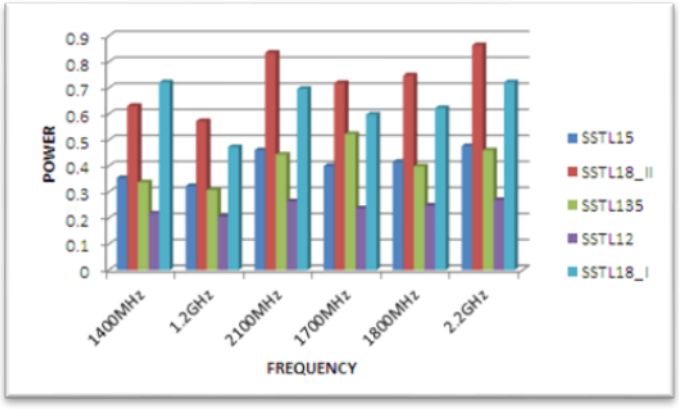

Figure 7. Power Analysis for Sstlfamily at Different Frequencies

3. Conclusion

The design is low power energy efficient and the code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family. The digital clock consists of 5 inputs and 6 outputs. Outputs are 7 bits output. The design is tested by varying frequencies at different SSTL IO Standards at constant temperature that is 25 degree Celsius and also keeping air flow constant. We can conclude that there can be 24-35% saving of total power dissipation by using frequency scaling technique.

4. Future Scope

The future scope of "SSTL IO Standard Based Energy Efficient Digital Clock Design on 28nm FPGA" is that we can also implement this design on 22nm or 18 nm FPGA. We can also use different FPGA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E. Here, we are using frequency scaling in which we are changing the operating frequency of a device and analyzing its power. We can redesign this Digital Clock Design with other energy efficient technique like capacitance scaling, thermal scaling, clock gating, various design goals, impedance matching with different logic family, and mapping. Analysis has been done with different frequencies like 1400 MHz, 1.2 GHz, 2100 MHz, 1700MHz, 1800MHz, 2.2GHz. We can use any other frequency range and test our design on that also. The temperature has been kept constant that is 25 degree Celsius so if needed it can also be varied. Air flow can also be varied when required.

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