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A Fractal Ultra-High-Speed Oscillator/Distributor Network with Structural Robustness to Voltage and Temperature Gradients

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Abstract

A study of a fractal structure of a clock generator and distributor is performed with possible use in today's ultra-high-speed, GHz range or higher, integrated circuit design and other future digital system applications. A fractal cell is composed of a simple ring oscillator with three inverting amplifiers, configuring a triangle shape, with an inverting amplifier placed at each side. Each side is then shared with an adjacent cell, which makes this fractal structure that is, theoretically, spreadable infinitely in 2D domain. This fractal structure is proved to have insensitivities to supply voltage and temperature variations: less than 1% of clocks skew of a clock period, with given 3% of supply voltage or 5% of temperature fluctuations. This is because any local disturbances or gradients will instantly and evenly be distributed to the whole networks yielding a global averaged state change. SPICE simulations are done with 0.5μm, 3V, N-Well CMOS process technology in order to prove the validity of the idea. A simple fractal CMOS layout, with 108 inverters, is also performed and included for future chip measurement.

Keywords: *Fractal Structure, GHz Oscillator, Clock Skew, Jitter, Clock Generation and Distributtion, Process/Voltage/Temperature (PVT) Gradient*

1. Introduction

Clock generation and distribution technique, in a few GHz-level or higher, for today's SOC and future ULSI chips is emerging as one of engineering's important bottlenecks, especially in terms of the overall performance of the whole digital system [1-3]. It is because the timing windows for recent digital systems have been scaling down to tens of a pico-second level during which data should be fetched and also processed, imposing a heavy timing constraint over a system data flow synchronization [2, 4-8].

The most popular and currently widely-used solution for an ultra-high-speed synchronization is Phase Locked-Loop (PLL) [9-12]. Along with symmetric clock line layout schemes, the PLL is known to provide synchronized system clocks with minimum level of clock skew, or jitters. However, with the physical nature of the clock line material characteristics, the jitters are still a limiting factor of systems overall performance, causing synchronization malfunctions even with today's state of the art PLLs [2, 8, 13-15].

Several researches for controlling the clock jitters, or skew, have been focused to minimize the skew, and several different techniques are still undergoing review for actual on-system use. These techniques seem to have complex structures with a heavy routing area or clock signal distribution length limit [2, 8, 13, 16-19].

In this paper, we are proposing a novel way of GHz clock generation and distribution technique [20]. This technique, called Fractal Cellular Oscillator Network, adopts a fractal structure of a very simple oscillator, which can spread infinitely in 2D in the current

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silicon-based IC systems. Due to this inherent fractal structure, it minimizes the jitters caused by local gradients, yielding global averaging and thus minimized jitter signals for each and every node instantly. This means that even with voltage and/or temperature gradient, this technique can still generate clock signals within a very small jitter range.

Temporal or steady-state temperature and/or power supply gradients are given for the proposed technique's robustness proof.

2. Structure of Fractal Cellular Oscillator Networks

Figure 1 shows the structure of the fractal Cellular Oscillator Network (CON). As seen, the CON has a fractal modular structure, theoretically spreadable infinitely. Each branch is composed of an inverting amplifier, performing an inverting function.

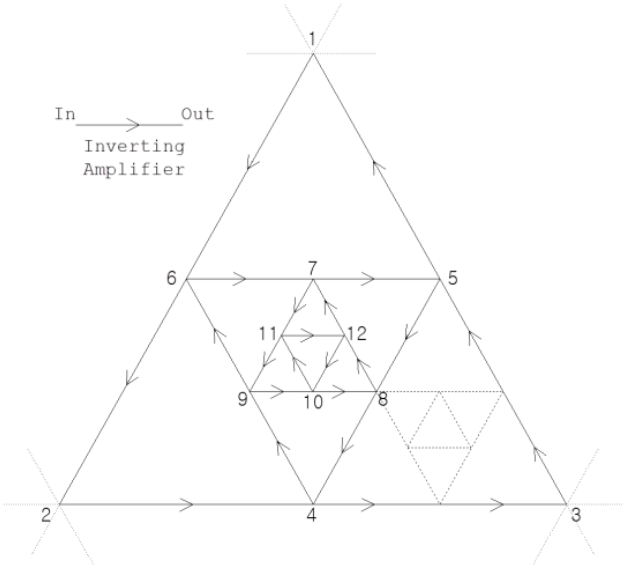


Figure 1. Structure of Fractal Cellular Oscillator Network

Here in this work, each branch is implemented with a CMOS inverter, as the simplest form, and each loop consists of an odd number of inverting nodes, which act as a type of a ring oscillator. Notice here that not just an inverter but any type of inverting amplifiers can be placed at each branch. Sharing each branch with adjacent three loop branches, this basic ring oscillator becomes a fractal cell of the fractal cellular oscillator network (CON).

In this scheme in Figure 1, if we use the exact same circuitry for each branch, this CON generates three different oscillating signals from three different nodes, with $2/3\pi$ phase shift among them [6, 8, 15, 20]. These oscillating signals will have exact 50% of duty cycle, which is another important criterion in today's telecommunication digital systems [8, 14, 15].

Once an external power supply is given for the CON, each loop will naturally and inherently oscillate with the exact same frequency. And even with a frequency change or a phase shift in one or several nodes in the network with voltage or temperature gradient, this local disturbance will spread out to the entire network, yielding an instant global state change with minimum skews among clock signals [6, 20].

3. CMOS Oscillator Network with an Inverter for Each Branch

Figure 2 shows a simple example of a fractal CMOS cellular oscillator network that is made up of only 108 inverters.

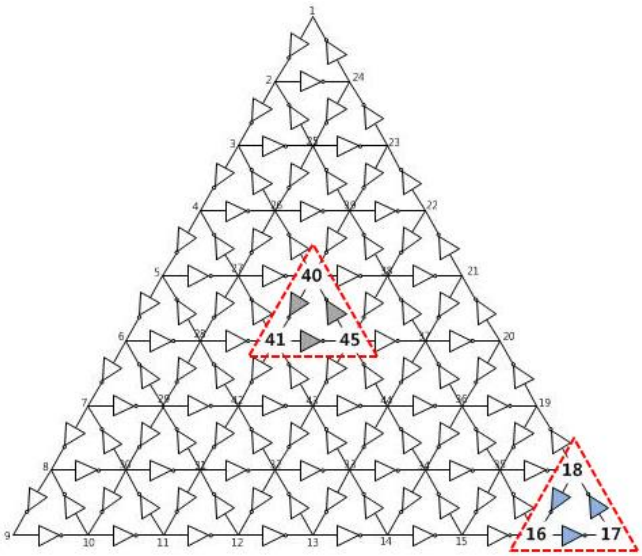


Figure 2. Fractal CMOS Cellular Oscillator Network With 108 Inverters

A way of implementing the CON is hereby suggested and displayed in Figure 3 using today's multilayer integrated circuit process and package technique. Analog and digital planes are separated for minimum interference between two different planes, and in the middle the proposed CON can be installed as shown.

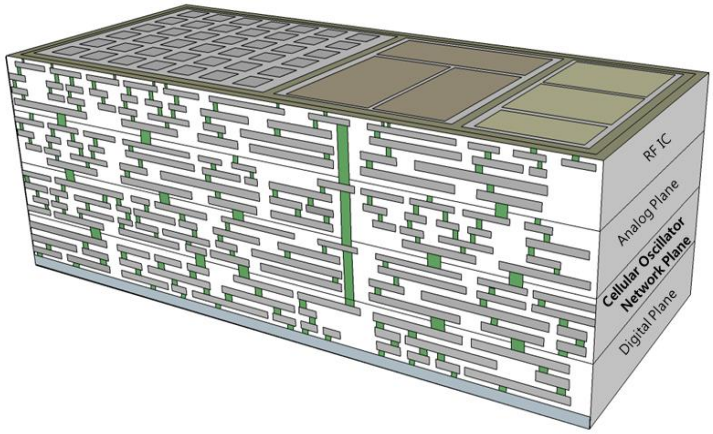


Figure 3. The CON Silicon Implementation in Multilayer CMOS/ Multi-Chip Module Package Technique

Notice in this scheme shown in Figure 1, there will be an instant global clock signal distribution with unbalanced load conditions, and in this paper, even with local power supply and/or temperature disturbances. The CON will have an inherent robustness against these different kinds of temporal or static gradients, with possibly minimum skews.

4. Clock Skew Simulation Results of Fractal Cellular Oscillator Network

Simulation results of the Figure 2 in time domain are shown in Figure 4.

The temperature and power supply are the same for the whole circuit with 300K and 3volts, respectively. As seen here, only three different oscillating signals are detected from the network, with a 120-degree phase difference among them.

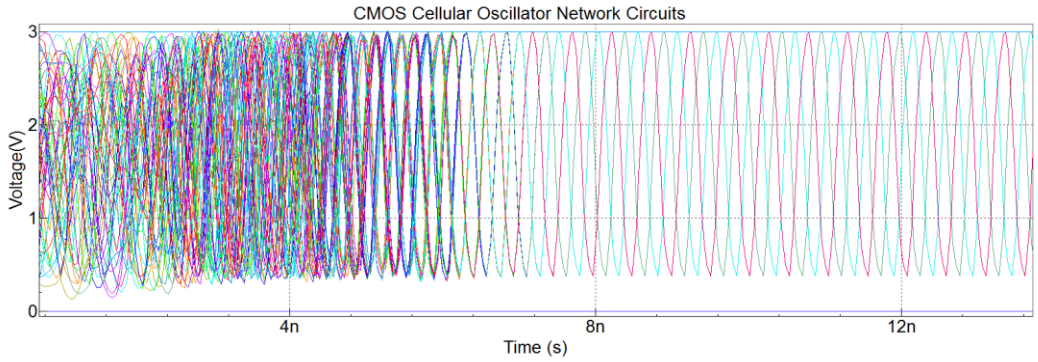


Figure 4. Simulation Results for the Figure 2

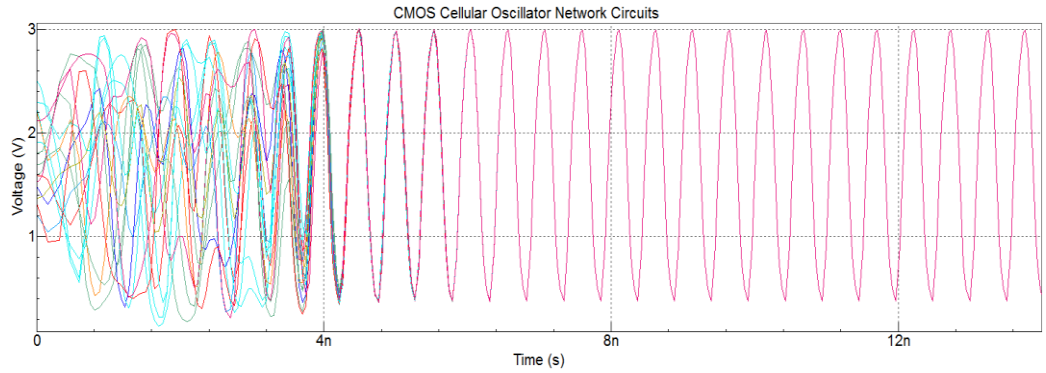


Figure 5. Fifteen In-Phase Nodes Simulation Results

In Figure 5, only 15 in-phase nodes signals in Figure 2 are displayed separately. With this fractal structure, and with feedback loops in the networks, fifteen nodes generate exact same signals.

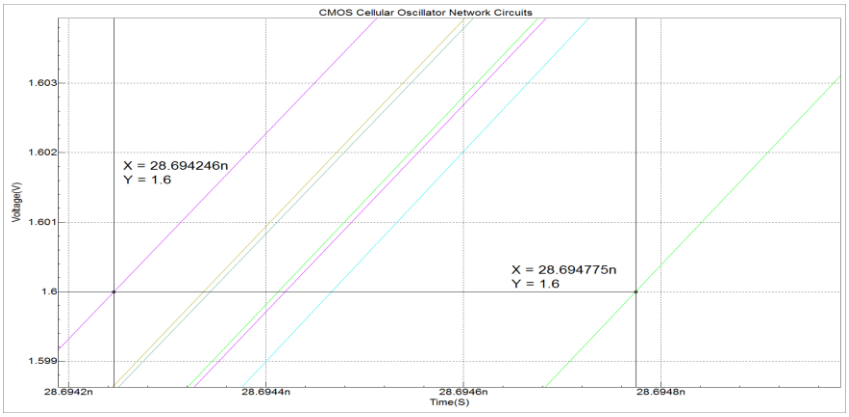


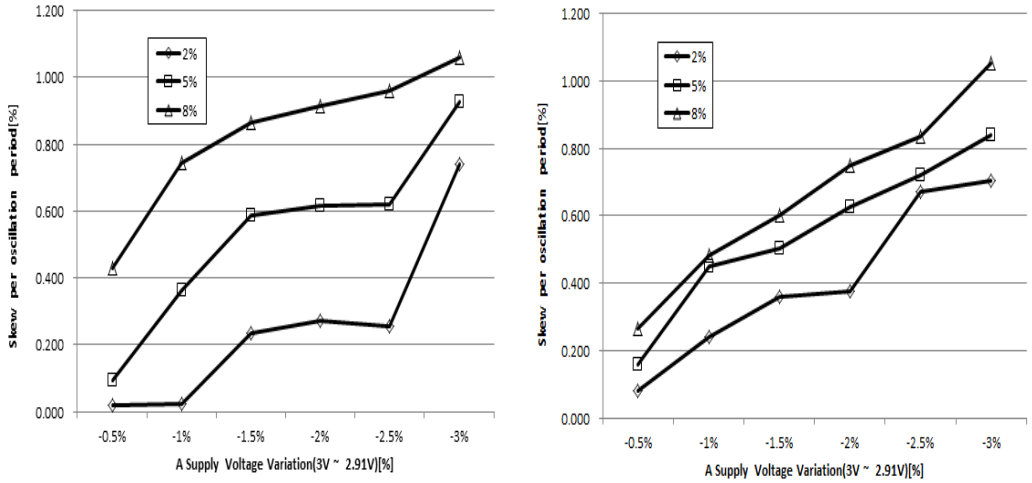
Figure 6. In-phase Nodes Clock Signals Skew Measurement

5. Simulation Results with Power Supply Voltage/Temperature Gradients

Simulations were done with CMOS n-well technology, along with 3V, 0.5um minimum feather size (both N- and P- MOS) conditions. Supply voltage is assumed changing 3% range, while the temperature is fluctuating within 5% of a given ambient temperature, a room temperature 300K.

5.1. Clock Skew Simulation with Supply Voltage Gradient

Figure 7 shows clock skew simulation measurements when power supply is changing locally up to 2, 5, and 8%, respectively. The (a) is when the local change is given only in the center loop (node 40, 41, 45 in Figure 2) and the (b) is for the corner loop (node 16, 17, 18 in Figure 2).



(A) Center Loop and (B) Corner Loop

Figure 7. Clock Skews with Local Power Supply Voltage Change

As read from the Table 1, maximum of ~1% of clock period is measured among in-phase nodes with 8% of supply voltage is given. The insensitivities for a local supply voltage fluctuation is clearly witnessed.

Table 1. Skew Variation Results for a Local Supply Voltage Change (Center and Corner)

The Center of Networks at Supply Voltage Variation								
Volt Variation			-0.5%	-1%	-1.5%	-2%	-2.5%	-3%
Skew Rate[%]	Cell Area	2%	0.021	0.023	0.235	0.273	0.257	0.742
		5%	0.095	0.364	0.587	0.618	0.620	0.929
		8%	0.430	0.745	0.866	0.916	0.960	1.061
Supply Voltage Range : 3 ~ 2.91V								
The Corner of Networks at Supply Voltage Variation								
Volt Variation			-0.5%	-1%	-1.5%	-2%	-2.5%	-3%
Skew Rate[%]	Cell Area	2%	0.081	0.240	0.361	0.375	0.672	0.703
		5%	0.159	0.451	0.502	0.628	0.722	0.841
		8%	0.265	0.483	0.602	0.748	0.836	1.054

5.2. Clock Skew Simulation with Temperature Gradient

Local temperature change is given, from 0% up to 100% for the whole nodes, and the skew was measured for each case. Figure 8 shows the simulation results.

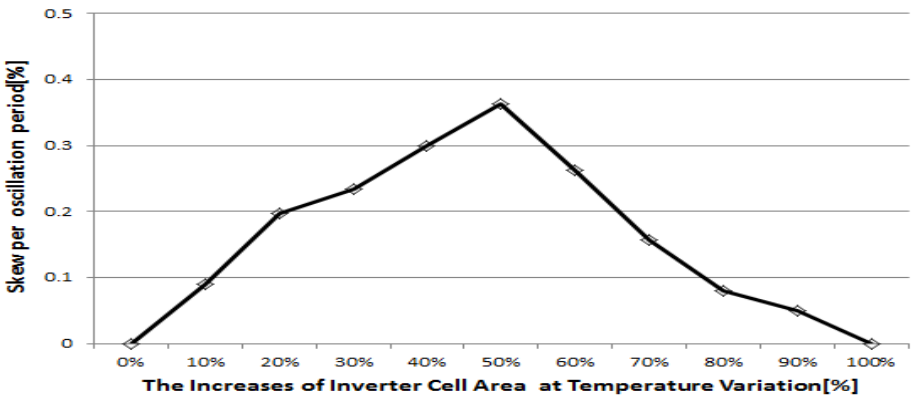


Figure 8. Clock Skew Variation with a Different Local Node Numbers (%)

As seen, the more nodes (cells) have temperature changes, the more skew is measured, at 50% the largest of 0.35%.

Table 2. Skew Variations for Maximum 5% of Temperature Change

Temp Variation	-5%	-3%	-1%	0%	1%	3%	5%
Skew Rate[%]	0.347	0.095	0.062	0	0.065	0.185	0.340
Operation Temperature Range : -40 ~ 85℃							

6. CMOS Layout

Figure 9 is a CMOS layout of 108 inverters CON shown in Figure 2.

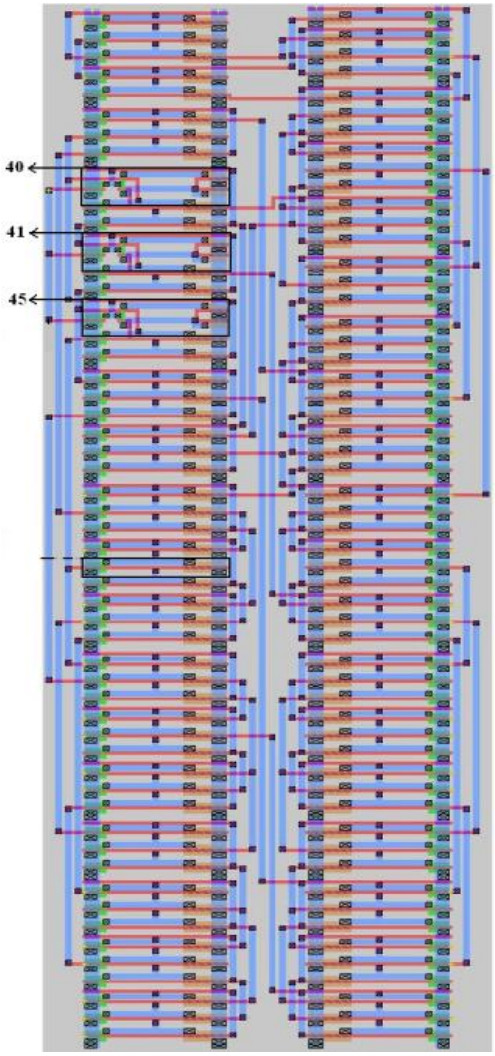


Figure 9. CMOS Layout of Figure 2

7. Conclusions

A primitive idea of fractal ultra-high-speed oscillator and distributor network is newly presented. Using an idea from well-known fractal model, this new and very simple approach of clock generation and distribution technique is tested and proved to work well in GHz range with minimum skews. With supply voltage and temperature gradients, simulations were performed to measure clock skews in different cases. With its inherent fractal structure, the cellular oscillator network is proven to have less than 1% and 0.4% clock skews of a clock period with given 3% of power supply and 5% of temperature fluctuations, respectively. This implies that the fractal cellular oscillator network can be adopted in GHz clock generation and distribution in a single chip, and chip-to-chip and system-to-system (SOC) applications as well. With its simple structure, and easy-to-implementation, the proposed technique is expected to be adopted in future digital systems. Layout is done and a chip is under fabrication for a future test.

Acknowledgements

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