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Research on Phase Locking and Tracing C-W Pulses

Weixian Song, Yuhua Chai* and Kezhu Tan

College of Electrical and information, Northeast Agricultural University, Harbin, China
songweixian@163.com

Abstract

In this paper the function of PPL and the principle of measuring frequency were introduced, as meanwhile, the references for the design of PPL based on software was provided. Based on this, we proposed the function of PPL based on software using MATLAB. Because PPL could be affected by different parameters, we analyzed the system in different condition. According to the results, the method of phase locking and tracing C-W pulses using PPL was proposed. We reached our goal that C-W pulses can be phase locked and traced.

Keywords: *phase locking and tracing; software PPL;CW-Pulses*

1. Introduction

The technique of phase locking is one of the important methods for signal tracing filter. The method is applied in communication, aerospace, and measuring widely [1].

Narrow-band filter can improve the signal-to-noise ratio and acquire detected signal of different time and different frequencies in signal processing [2]. However, it is difficult to realize tracing filter for C-W pulses using narrow-band filter, since the center frequency changes constantly in C-W pulses. At present, many researchers pay attention to the technique of tracing filter in signal. Some results have been achieved in this aspect, but it is not enough for C-W pulses. The trouble is that C-W pulses can be traced when it appears while C-W pulses can't be traced when it disappears. The principle of software PLL was introduced and the method of phase locking and tracing C-W pulses using PPL was proposed in this paper. Finally, the function of PPL based on software was proposed, and the tracing procedure was simulated using MATLAB.

2. The Design of Software PPL Model and Parameters

2.1. The Design of Software PPL's Model

Z domain model of digital phase discriminator is shown as (1).

$$\theta_e(z) = \theta_i(z) - \theta_2(z) \tag{1}$$

This paper adopts the signal of orthogonal decomposition to realize digital phase, the principle block diagram of this method is shown as Figure 1 [3, 4].

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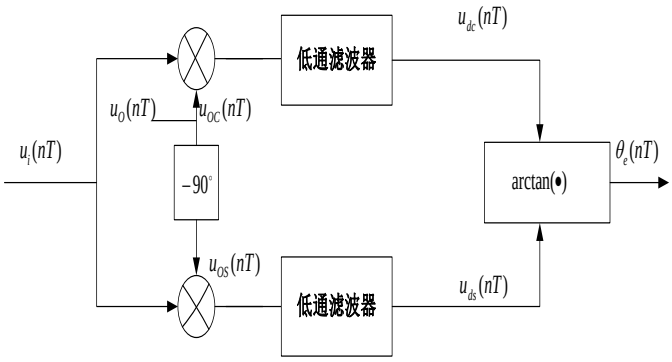


Figure 1. The Principle Diagram of the Digital Phase Discriminator

If:

$$u_{ds}(nT) = AU_i U_o \sin[\theta_i(nT) - \theta_2(nT)] \tag{2}$$

$$u_{dc}(nT) = AU_i U_o \cos[\theta_i(nT) - \theta_2(nT)] \tag{3}$$

else:

$$\begin{aligned} u_{ds}(nT) &= LPF[u_i(nT) \cdot u_{oc}(nT)] \\ &= AU_i U_o \sin[\theta_i(nT) - \theta_2(nT)] \end{aligned} \tag{4}$$

$$\begin{aligned} u_{dc}(nT) &= LPF[u_i(nT) \cdot u_{os}(nT)] \\ &= AU_i U_o \cos[\theta_i(nT) - \theta_2(nT)] \end{aligned} \tag{5}$$

In the equation, LPF is low pass filter; A is constant gain brought by low pass filter. So the output of the phase discriminator:

$$\theta_e(nT) = \arctan[u_{ds}(n)/u_{dc}(n)]$$

$$= \theta_i(nT) - \theta_2(nT) \tag{6}$$

Z domain model of digital phase discriminator is shown as following equation.

$$H_{LF}(Z) = U_c(Z)/\theta_e(Z) = \frac{2\xi}{\omega_n} + \frac{T}{2} + \frac{T}{Z-1} \tag{7}$$

Through inverse Z transform time-domain expression of digital loop filter is:

$$u_c(nT) = u_c[(n-1)T] + (\frac{2\xi}{\omega_n} + \frac{T}{2}) \cdot \theta_e(nT) - (\frac{2\xi}{\omega_n} - \frac{T}{2}) \cdot \theta_e[(n-1)T] \tag{8}$$

The Z domain model for NCO (numerically controlled oscillator):

$$H_{NCO}(Z) = \theta_2(Z)/U_c(Z) = \omega_n^2 \cdot \frac{T}{2} \cdot \frac{Z+1}{Z-1} \tag{9}$$

NCO of time-domain expressions is obtained by inverse Z transform:

$$\theta_2(nT) = \theta_2[(n-1)T] + \omega_n^2 \cdot \frac{T}{2} \cdot u_c(nT) + \omega_n^2 \cdot \frac{T}{2} \cdot u_c[(n-1)T] \tag{10}$$

Type (10) is a recursive expression of variables, The formula can be recycled:

$$\theta_2(nT) = \theta_2(0) + \omega_n^2 \cdot \frac{T}{2} \cdot \sum_{k=1}^{n} u_c(kT) + \omega_n^2 \cdot \frac{T}{2} \cdot \sum_{k=0}^{n-1} u_c(kT) \tag{11}$$

$u_c(nT)$ Variable values small and the change will not too fast, it is $\sum_{k=1}^{n} u_c(kT) = \sum_{k=0}^{n-1} u_c(kT)$ set up. Considering NCO output signal of the total phase:

$$\theta(nT) = \omega_n nT + \theta_2(nT) \tag{12}$$

The comprehensive formula (9), (10)and(11), get the NCO output signal of the expression:

$$u_o(nT) = U_o \cos[\omega_o nT + \theta_o + \omega_n^2 \cdot T \cdot \sum_{k=1}^{n} u_c(nT)] \tag{13}$$

2.2. Parameter Design

According to the principle of PLL, the choice of natural resonance frequency(ω_n) and damping factor (ξ) for PLL to PPL's performance is contradictory and unitive. Capture zone will be increased and acquisition time decreased as ω_n and ξ growing, and the noise of VCO can be filtered , the steady - state correlation can be decreased , synchronization band can be increased ,the synchronization scan ration can be increased. As ω_n and ξ decreasing, the input noise can be filtered, tracing precision can be raised and the average time of pulse can be delayed. Therefore, the reasonable design of parameters can optimize the performance of PLL.

2.2.1. Damping Factor:

According to the loop suppression performance of the input noise, equivalent noise bandwidth will be the minimum when we chose $\xi = 0.5$. [5] We should choose a value in the $0.6 < \xi < 1$ because of considering the loop transient response should not be too long, In fact we should chose general $\xi = 0.707$[6].

2.2.2. Natural Resonance Frequency:

Assumes that the maximum deviation of the input signal $\Delta\omega_{\max}$ (or the maximum Doppler frequency offset), in order to improve the capture of loop performance and to ensure that can makes the greatest frequency deviation come into fast capture bandwidth that $\Delta\omega_{\max} \le 2\xi\omega_n$ [7], so we can see $\omega_n \ge \Delta\omega_{\max} / 1.414 = 0.707\Delta\omega_{\max}$ [8].

A closed-loop amplitude frequency response on the Structure of the active power filter of second order is $|H(j\Omega)| = \sqrt{\frac{1+4\xi^2x^2}{(1-x^2)^2+4\xi^2x^2}}$.

Among them, $x = \omega/\omega_n$ the ideal second order PLL is equivalent to a low pass filter. When $\xi = 0.707$, if $|H(j\Omega)|^2 = 0.5$, we can obtained the cut-off frequency of the phase-locking loop $\omega_c = 2.06\omega_n$. The Ideal loop filter should be only allow through by tracked carrier component and Filtering out all other filtering signal, so that make $\omega_c = 2.06\omega_n \le \omega_{i\min}$, scilicet $\omega_n \le 0.485\omega_{i\min}$ [9, 10].We can make the value of ω_n is 0.485-0.707 according to the above analysis. When the input signal to noise ratio is large,

we should be taken close ω_n to the limit to get a faster capture speed ;and when the input signal to noise ratio is small, we should consider the tracking accuracy and will ω_n get close to the lower limit firstly [11]. We can use the flexibility of the software implementation and set different parameters in different working stages of phase-locked loop in order to achieve optimal performance [12-15].

3. The Simulation Analysis

3.1. The Effect Of Natural Resonant Frequency on The Phase-Locked Loop Performance

The maximum of Doppler frequency offset is $\Delta f_{\max}=0.5KHz$ when the signal center frequency is 35.5 Hz. The 35 KHz reference signal is used for tracking. At this point the frequency offset is 0.5KHz. $\zeta=0.707$, $K=4$, $f_{\max}=500Hz$, so that when $\omega_n=4200$ $\omega_n=5000$ $\omega_n=7000$,the simulation results are shown from Figure 2 to Figure 4.

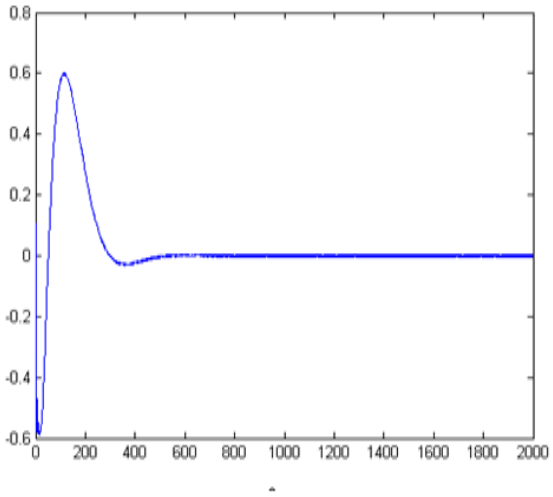


Figure 2. Phase Locked Tracking Simulation Diagram, $\omega_n=4200$

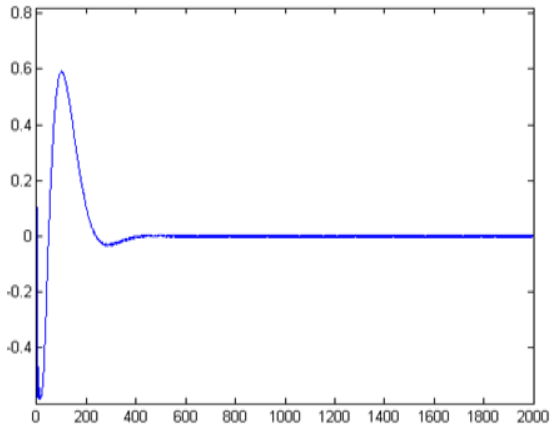


Figure 3. Phase Locked Tracking Simulation Diagram, $\omega_n=5000$

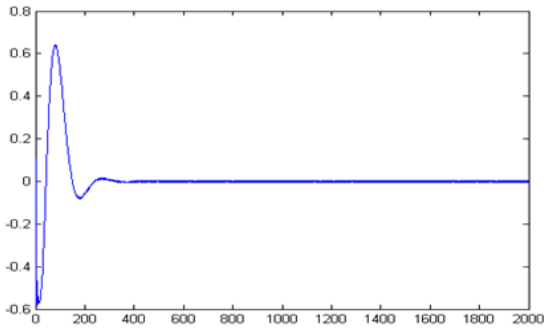


Figure 4. Phase Locked Tracking Simulation Diagram, $\omega_n = 700$

Simulation diagrams above have shown that in the reasonable θ_n range the greater θ_n mans the faster capture speed and the smaller θ_n means the higher tracking precision.

3.2. The Effect of SNR on the Phase-Locked Loop Performance

The 35KHz reference signal is used for the phase-locked tracking of the 35.3KHz input signal, at this point the frequency deviation is 0.3KHz. The sampling rate is 300KHz, and the damping coefficient is 0.707.

When the SNR is 40dB, the output phase displacement of phase discriminator is shown in Figure 5 and the simulation of signal tracking process is shown in Figure 6.

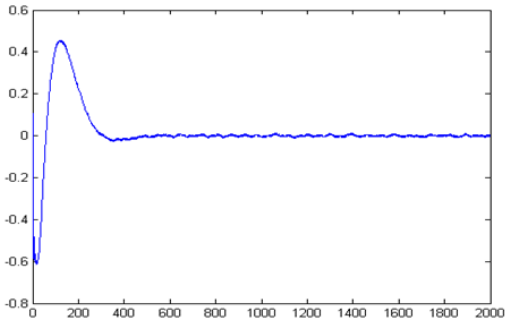


Figure 5. The Output Phase Displacement of Phase Discriminator, SNR=40db

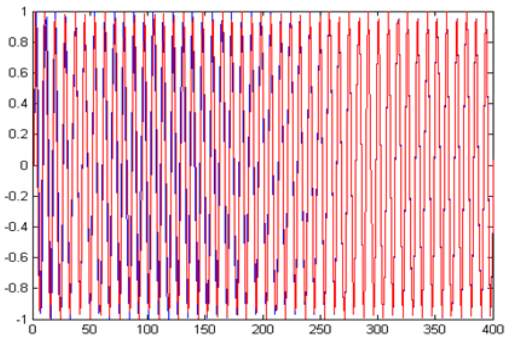


Figure 6. The Process of Signal Tracking, SNR=40db

The measured input signal frequency is 35300.5188Hz, and the error is 0.5188Hz.

When the SNR is 10dB, the output phase displacement of phase discriminator is shown in Figure 7 and the simulation of signal tracking process is shown in Figure 8.

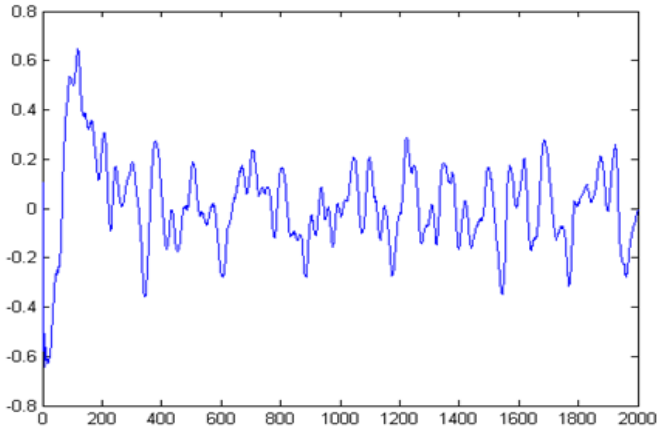


Figure 7. The Output Phase Displacement of Phase Discriminator, SNR=10db

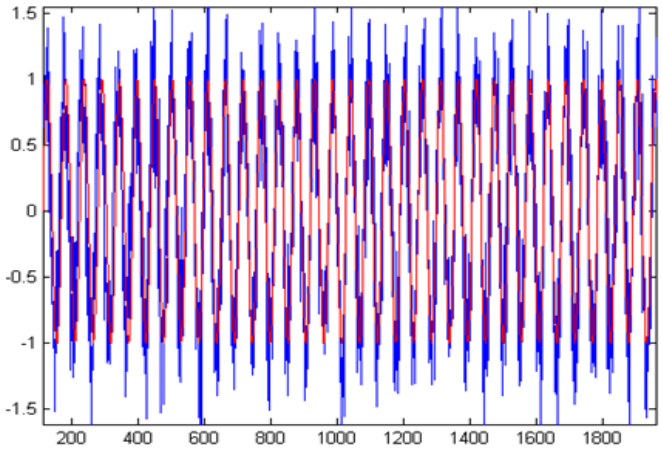


Figure 8. The Process of Signal Tracking, SNR=10db

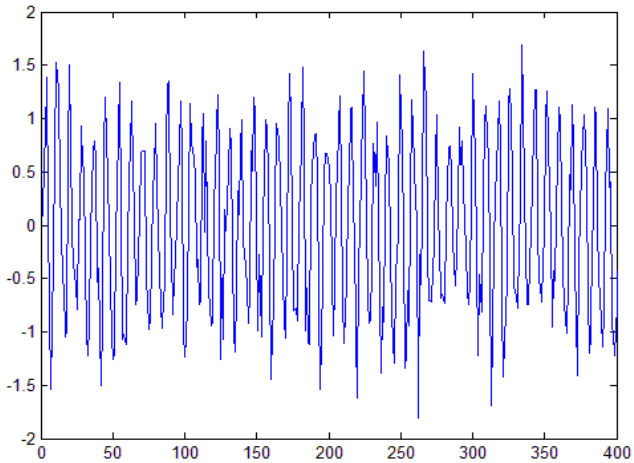


Figure 9. Input Signal

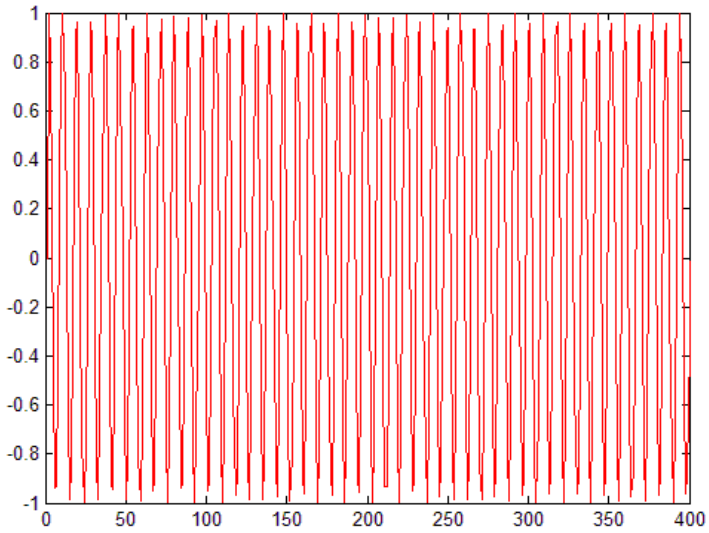


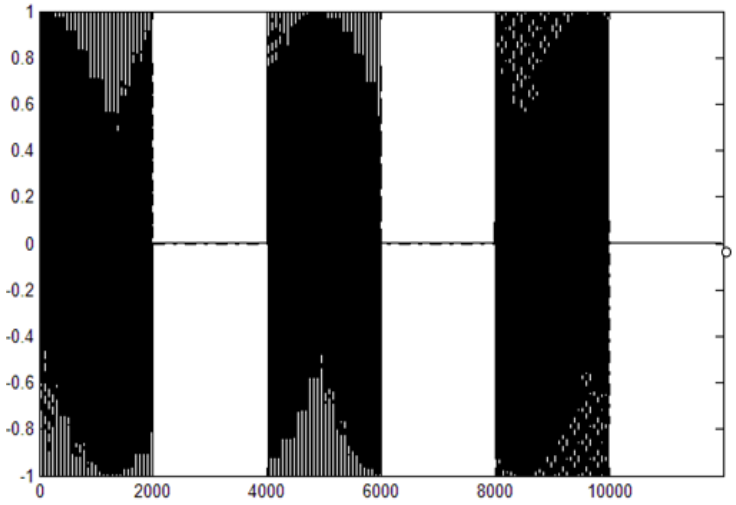
Figure 10. After Tracking the Output of the Signal

The measured input signal frequency is 35304.5789Hz, and the error is 4.5789.

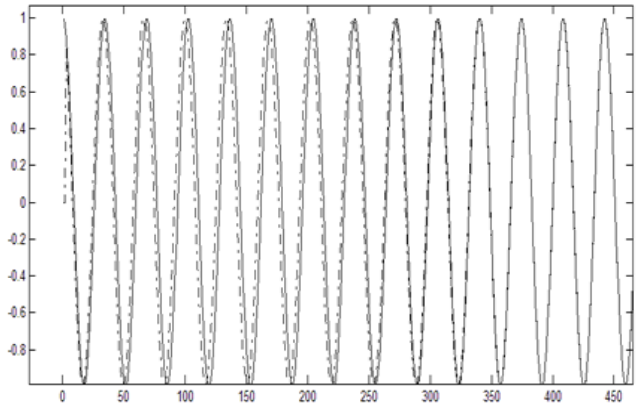
Through the simulation analysis, we can see that higher SNR means higher measurement accuracy, the lower SNR means lower measurement accuracy. Under low SNR(10dB) conditions, when $\Delta f = 0.3kHz$,the PLL can still accomplish capture in a relatively short period of time. Phase error fluctuates up and down in the zero point because of the high noise. The SNR is greatly improved through PLL, this illustrates that the phase-locked loop has a high ability to filter out the noise.

3.3. Phase-Locked Tracking for CW Pulse Signal

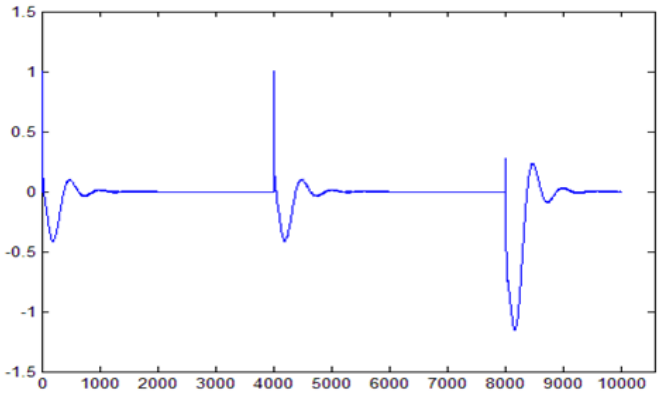
The simulation is shown in Figure 11. In the figure the input signal is shown in dotted line, and the output signal after phase-locked loop tracking is shown in solid line.



(A) The Overall Figure of Tracking Process



(B) Local Amplification of Tracking Process



(C) The Output Phase Displacement of Phase Discriminator

Figure 11. Phase-Locked Tracking for CW Pulse Signal

The errors of three pulse frequency measured through simulation respectively is 0.5443Hz 0.5425Hz, 0.5459Hz.

The simulation results show that CW pulse signal can be well tracked by phase-locked loop, and the measurement precision of the input CW pulse frequency is high.

4. Conclusion

Based on the theory of Phase-locked loop, the PLL simulation algorithm is researched through Matlab in this paper. The simulation results show that CW pulse signal can be well tracked by phase-locked loop model, and the measurement precision of the input CW pulse frequency is high.

Acknowledgements

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Author

Weixian Song, is a Ph.D. student in the Agricultural Electrification and Automation School at College of Electrical and information ,Northeast Agricultural University. His fields of research are Weak Signal Detection, Agricultural Products Detection and Signal Processing.