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EMC Research and Design for a Fiber Access Communication System

Xiaochun Liu[1] and Dongping Hu[2]

[1]*Information Engineering College, Chang'an University*
Xi'an,710064,China
xchliu@chd.edu.cn
[2]*Research and Development Department, ZTE Corporation*
Xi'an 710065, China
hudongping118@163.com

Abstract

A fiber access communication system is developed to cater for the need of network communications industry. In this paper, the basic framework of the system is described; with regards to the characteristics of the system, firstly the electromagnetic interference approaches of the whole system are discussed. Emphasis is laid on the engineering analysis and discussion of the interference sources of electromagnetic emission, with solutions thereof suggested; meanwhile, analysis and discussion are conducted on the electromagnetic immunity of the system in view of electromagnetic coupling paths, with corresponding solutions put forward as well. Lastly, the EMC testing results of the system is presented. Practice has proven that this approach is specially favorable for EMC design and comprehension throughout the system development process, which is also effective for the communication industry in EMC design and verification.

Keywords: *optical fiber communication, EMC, conduction coupling, harmonic interference, signal integrity*

1. Introduction

In telecommunications, electromagnetic compatibility (EMC) has drawn enormous attentions. There are two basic EMC requirements for electronic communication system equipment, including: mandatory demand by government agencies; requirements put forward by manufacturers for ensuring the reliability and quality of products and winning well-standing reputations so as to secure success in market competitions[1]. To cater for the need of network communication industry, an optical fiber access communication system has been developed. In this paper, the basic framework of the said system is described; EMC problems such as electromagnetic radiation emission, radiation sensitivity, conduction emission and sensitivity of the system are analyzed. The paper mainly conducts discussions on EMI-related problems from the "source", and ends up with corresponding solutions. Practice has proven that this approach is specially favorable for EMC design and comprehension throughout the system development process, which is also effective for the communication industry in EMC design and verification.

2. Analysis on the Electromagnetic Interference of the System

A. Introduction to the Basic System Architecture

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System hardware platform is mainly composed of CPU mini-systems, operation nest plates, FPGA signal processing module, CPLD logic module and power supply system and so on. See Figure 1 for the typical system architecture as follows. CPU mini-system runs VxWork real-time embedded operating system; while Flash is used to store CPU mini-system program and basic configuration information. SDRAM and DDR2 memory chips are mainly involved in storage of intermediate data during program running process. FPGA is responsible for completion of comprehensive processing of various access operations. Access modules are mainly intended to complete processing of GPON and EPON communications protocol processing. Optical modules are utilized for photoelectric signal conversion and operation distribution. CPLD is in charge of the detection and management of version information of plate system, presence of clock signals, power supply voltage, temperature, and reset signals, etc.

B. Analysis on System Electromagnetic Interference Channels

The generation of electromagnetic interference has to be equipped with three basic elements: interference source, interference transmission path and sensitive device [2-5]. The interference paths of optical fiber access network equipment mainly include: conduction interference incoming or outgoing through the signal cable, power cord, and ground wire, etc of service interference; impedance coupling interference generated from the workplace as well as emission interference generated from various "accidental" antenna. In practical electromagnetic environment, interference channels of the electronic system are extremely complex. For ease of analysis, we give a brief on the distribution pattern of the three major electromagnetic interference elements as shown in Figure 2:

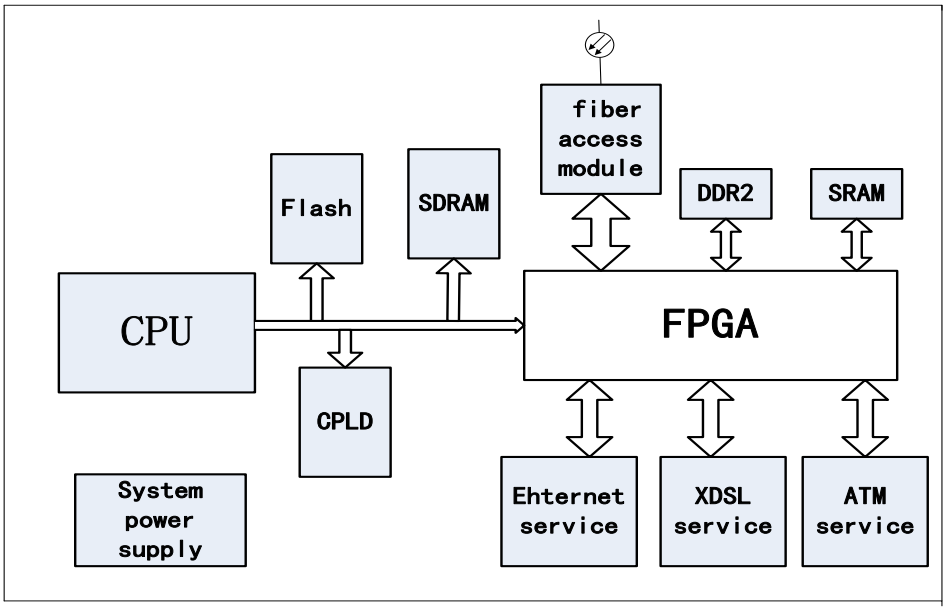

Figure 1. System Architecture Diagram

C. Analysis and Research on Radiated Emission (RE)

The so-called EMI problems refer to that upon normal operation of equipment or system under a certain environment, there should not be excessive electromagnetic energy generated. It's not hard to find from the electromagnetic interference path as indicated in Fig. 2 that

clock signals and high-speed interface signals are distributed everywhere on the system board. System clock signal and its harmonics, as well as high-speed digital signal and its SI problems, are the major contributors to electromagnetic emission interference.

Signal integrity (SI) is another original source of EMI problem. As the communication network system clock and communication rate are constantly increasing, the rise/ fall time of digital signal on physical links is becoming shorter and shorter. To conduct engineering estimate by taking 10%-90% of the rise/ fall time of a digital signal, its equivalent bandwidth of F_{3dB} is $F_{3dB} = \frac{0.35}{t_{10\%-90\%}}$. In this system, there exist enormous signals with rise/fall time shorter than 1ns and high-frequency harmonic signals with F_{3dB} bandwidth larger than 350MHz in important access circuits, such as Ethernet GMII interface, high-speed SERDES interface, Local-Bus line and DDR2 memory interface, etc. In case that the lengths of physical transmission line of these signals are greater than $1/6$ of the effective length of

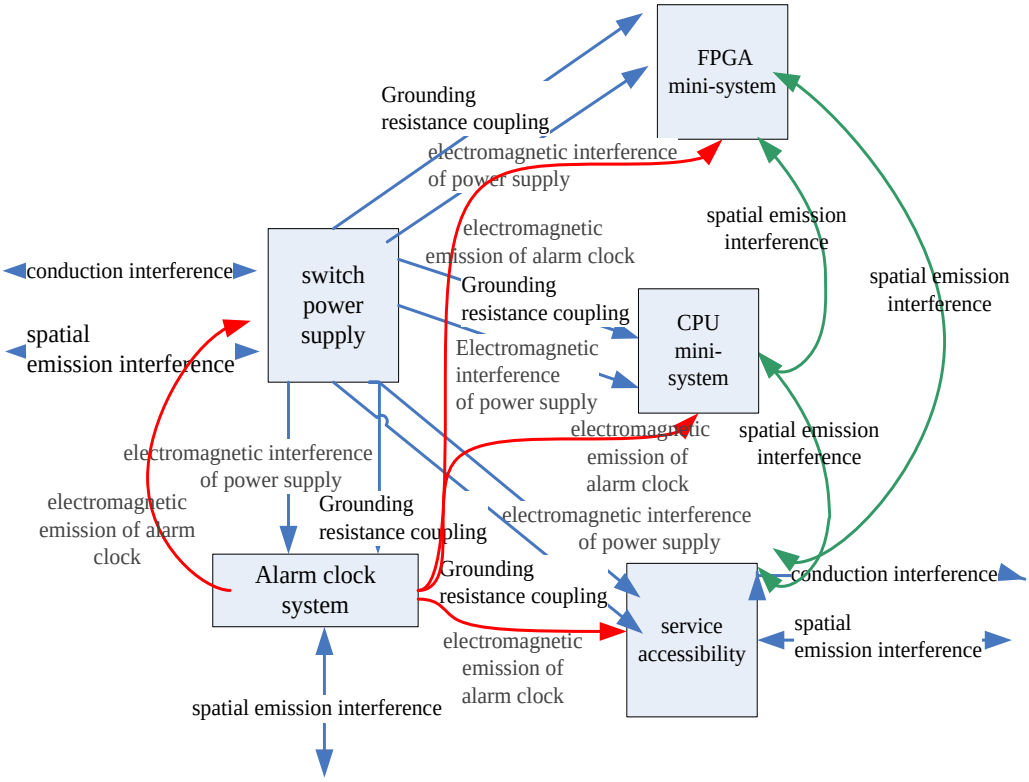

Figure 2. Distribution Map for System Electromagnetic Interference Paths

signals, the physical line mainly demonstrates the characteristics of a distribution parameter transmission line[6]. The characteristic impedance is $Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$, wherein, R, G, L, and C are the distribution parameters of the transmission line. When confronted with

discontinuous impedance, signal integrity problems occur, such as ringing, overshoot, undershoot, ground bounce, and other system problems [7]. Such incomplete signal will strengthen certain area of the original waveform signal spectrum[8], forming strong magnetic interference source at a certain frequency point, thus producing radiation interference to other circuit systems[9-10].Inductance and capacitance of PCB lands and wires in a digital system can cause a phenomenon referred to as ringing. It is the most prominent contribution to electromagnetic compatibility. As the signal level transitions from one logic level to another, there is a tendency for the signal level to oscillate about the desired level. Losses tend to damp this ringing. This type of waveform can be described mathematically as a function of the form $f(t) = Ke^{-\partial t}\sin(\omega_r t + \theta)$, among which, clock signals can be unfolded in form of Fourier series:

$$f(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos(2\pi \mathrm{n}\frac{t}{T}) + \sum_{n=1}^{\infty} B_n \sin(2\pi \mathrm{n}\frac{t}{T})$$

Wherein, A_0 in the expansion form represents the average value of signals, A_n is cosine coefficient, and B_n is sine coefficient. In the design of this system, as the clock signal is periodic, which is approximately considered with a duty ratio of 50% in engineer; the signal amplitude is A, and the duration is $\tau = \frac{1}{2}T$, $A_0 = \frac{1}{2}A$, $A_n = 0$; while fundamental frequency is $\omega_0 = \frac{2\pi}{T}$, $B_n = \frac{2A}{n\pi}$ (n is an odd number), $B_n = 0$ (wherein, n is an odd number), which represents the “square wave signal".

$$f(t) = \frac{1}{2}A + \frac{2A}{\pi}\sin(\omega_0 t) + \frac{2A}{3\pi}\sin(3\omega_0 t) + \bullet\bullet\bullet$$

In consideration that the minimum external clock signal source in the circuit is 25MHz, which can reach about 400MHz after N times frequency inside the chip, A is mostly of 3.3V (electric level), so apparently alarm clock signals contain a large amount of high-frequency harmonics, which are extremely liable to generate emission interference through "accidental" antenna. Therefore, alarm clock signal is the crucial source of system EMI problems, thus inhibition of radiation interference generated by clock signals from the source is an effective approach for addressing EMI problems.

Secondly, signal integrity (SI) is another original source of EMI problem. As the communication network system clock and communication rate are constantly increasing, the rise/ fall time of digital signal on physical links is becoming shorter and shorter. To conduct engineering estimate by taking 10%-90% of the rise/ fall time of a digital signal, its equivalent bandwidth of F_{3dB} is $F_{3dB} = \frac{0.35}{t_{10\%-90\%}}$. In this system, there exist enormous signals with rise/fall time shorter than 1ns and high-frequency harmonic signals with F_{3dB} bandwidth larger than 350MHz in important access circuits, such as Ethernet GMII interface, high-speed SERDES interface, Local-Bus line and DDR2 memory interface, etc. In case that the lengths of physical transmission line of these signals are greater than $1/6$ of the effective length of signals, the physical line mainly demonstrates the characteristics of a distribution parameter transmission line [6]. The characteristic impedance is $Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$, wherein,

R, G, L, and C are the distribution parameters of the transmission line. When confronted with discontinuous impedance, signal integrity problems occur, such as ringing, overshoot, undershoot, ground bounce, and other system problems [7]. Such incomplete signal will strengthen certain area of the original waveform signal spectrum [8], forming strong magnetic interference source at a certain frequency point, thus producing radiation interference to other circuit systems [9-10].

D. Analysis and Design on Conducted Emission (CE) of the System

CE is another EMI interference source for the system, *i.e.* conducted emission interference. Interference signals are mainly distributed in low-frequency section below 30MHz. In this system, -48V-12V switch power source is adopted. High-frequency switch power supply is one of the main sources of system CE interference, with the CE conduction model of the switch power source shown as Figure 3:

Wherein, C, C3 and C4 are parasitic capacitance. Upon the power-on and power-off of the switch tube Q1, comparatively great voltage spike noise would occur to switch power supply, which forms conduction disturbance after transmission to the input/ output terminals of the power source through the parasitic coupling path as shown in Figure 3. Conduction disturbance can be effectively inhibited by adoption of transformer shielding, reduction of parasitic capacitance, and truncation of noise coupling path.

E. EMS Analysis and Design of the System

The so-called EMS problems refer to that upon normal operation under a certain environment, the equipment or system can undertake corresponding electromagnetic energy interference within a specified range, mainly involving transient interference (mainly includes ESD, EFT/B, and SUREE), radiation immunity RS and conducted immunity, etc. In certification and reliability test, these items are mainly used for simulating some short high-energy pulse interference existing in actual electromagnetic environment such as

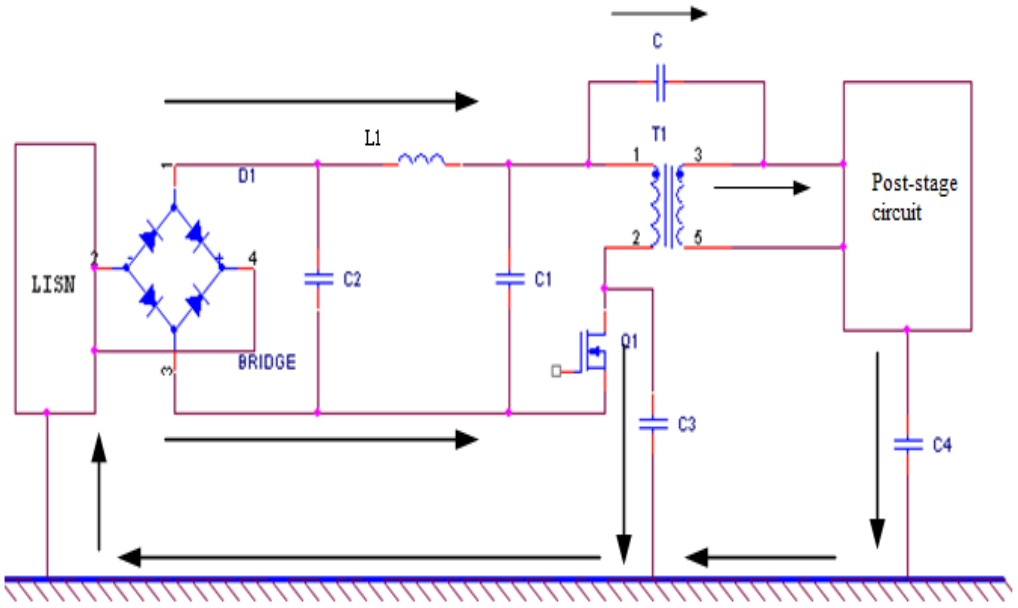

Figure 3. Analysis Model for Switch Power Source Disturbance

lightning and static electricity discharge, etc for electronic communication equipment. Take RJ45 connector ESD discharge test for example to discuss the EMS analysis and design method of the system. When ESD discharge gun discharges against the metal housing on RJ45, the impact on the system includes:

-the initial electric field would be coupled to the network with large surface area, and KV/m-grade high electric field would be generated near the electric arc:

-Part of the charges and current discharged would be infused into the IO terminal of the chip, leading to chip damages or work abnormity;

-The arc would generate strong magnetic field in the range of 1-500 MHZ, which would be also inductive coupling to the adjacent loops, thus resulting in disturbance and high-voltage pulse on the conductor.

In addition, as the various transient interferences would generate large transient current, thus another kind of typical disturbance is given rise to due to existence of impedance as shown in the Figure 4:

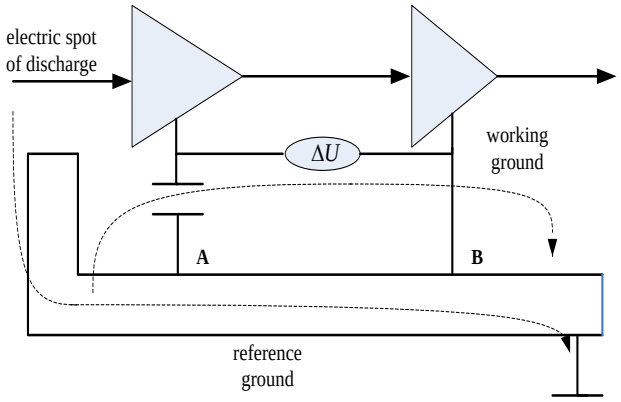

Figure 4. Analysis Model for Switch Power Disturbance

Upon the passing of common-mode interference electric current through the ground line AB, due to the presence of parasitic inductance and because that the impedance is not zero, common-mode current would produce $\Delta U = L \times \mathrm{d}\frac{\mathrm{dI}}{\mathrm{dt}}$ on the ground line in middle of AB, the existence of which would result in logical maloperation of subsequent circuit.

3. Solution Design to Electromagnetic Compatibility of the System

There are numerous EMC design methods in engineering practice. Different design solutions are effective in varied degrees as to system EMC problems. Besides, EMC testing and certification involve many aspects, thus designing of solution needs to take all factors into consideration for overall layout. Comprehension of the main contradictions of EMC problems and the major aspects of contradicts constitutes the engineering guiding ideology to address electromagnetic compatibility related problems. The major solutions are as follows:

1. It can be known from analysis in Section 2.2 that for EMC problems of fiber access system in this paper, we firstly take the following aspects into consideration as to the overall layout and planning, as shown in Figure 5: with high-speed digital circuit, keeping away from external-interface circuit; separating the system by reference to form PGND and GND, which

are connected to the housing by single point through structural screws, so as to realize "three-to-one" common-mode protection bridging in-between, with the protective circuit strictly in reference to the ground floor of PGND; With PGB, a laminated design scheme of "Top ─ GND ─ S1 ─ S2 ─ Power ─ GND ─ S3 ─ S4 ─ Power ─ Bottom" is adopted. The high-speed signal reference floor keeps integrity and continuity, which conforms strictly to "20H" principle.

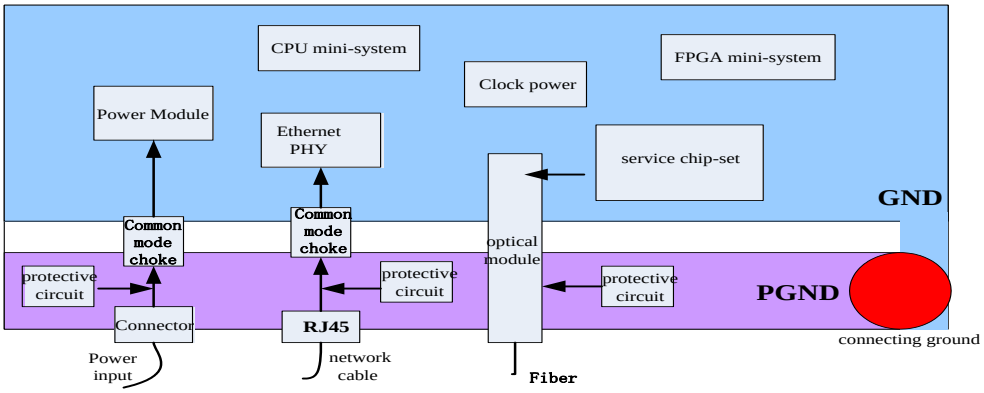

Figure.5 Schematic Diagram for System Layout Planning

2. From analysis in Section 2.3, we know that the key to address EMI problem lies in inhibition of emission source. In terms of layout, the clock and high-speed signals should be kept away from external interface circuit. Besides, on the precondition of meeting the system timing and reliability requirement, clock frequency and rise/ fall time of digital signals should be minimized. The method of "origin match" is adopted for high-speed digital signal. Clock distribution links can be designed into the form of "daisy chain". Emissions from high-frequency harmonic should be inhibited to avoid the occurrence of SI problems. In addition, PCB routing should follow "3W" principle so as to reduce mutual emission disturbance. In consideration of interference coupling path, EMC protection treatment should be conducted on metal housing; and 360 degrees of lap-joint treatment needs to be performed on bottom cable of external shielding cord, etc.

3. Protection of external service accessibility is a key object for system EMC design, which is also an effective approach for addressing CE and RE problems in interfaces. Take the design of internet access in this system as example, which is as shown in the figure 6:

4. System Emc Test

EMC design is an engineering discipline heavily dependent on tests. The effect of EMC design can only be verified through EMC testing and certification as well as EMC reliability test. Hereto, the EMC test results on the communication system device designed in this paper are shown in Table 1.

Table 1. System EMC Testing Results

Test Item	***Testing Method***	**Testing Result/ Testing Grade**
RE test	CISPR 22 Radiate IE	CFPR47P15; Class A
CE test	CISPR 22 Conduct IE	Meeting EN55022 standard; Class A
ESD test	EN61000－4－2	Contact discharge 6KV； air discharge 8KV
RS test	EN61000-4-3RI	80MHz-1000MHz 10V/m

CS test	EN61000-4-6CI	0.15MHz-80MHz,10Vrms
SURGE test	EN61000-4-5VS	1KV L-L; 2KV L-Earth
EFT/BTest	EN61000-4-FTB	1KV Clamp (LAN）, 2KV Direct（L，N，L+N）

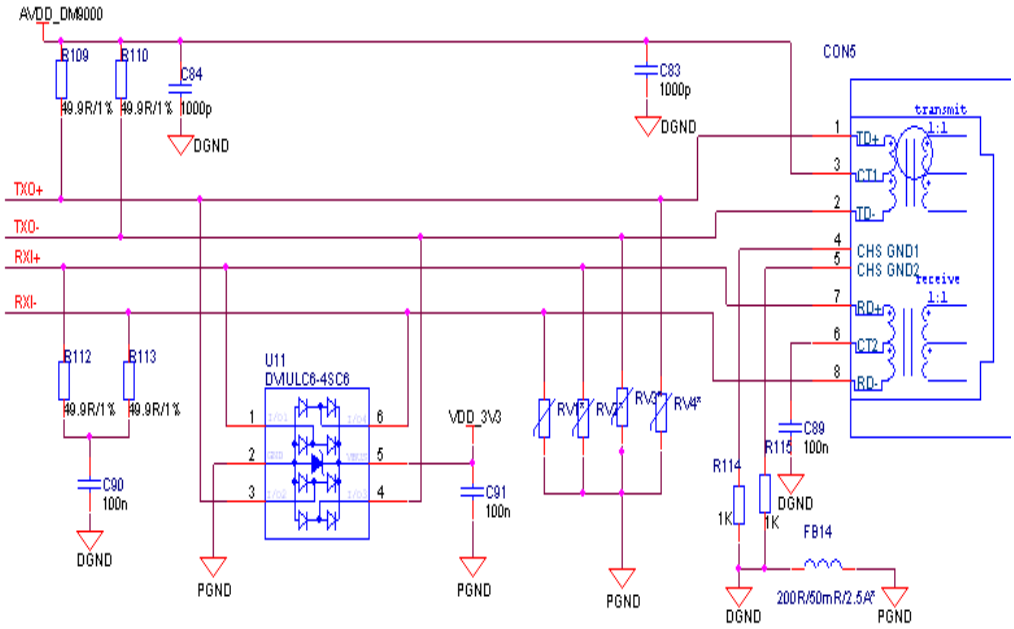

Figure 6. MII Interface Circuit

5. Conclusions

In network communication industry, the EMC design and test of system and product need to be assured throughout the processes of system integration and product development. Practice proves that the earlier EMC design is initiated, the lower the expense for addressing EMC problems would be. The EMC analysis and solution of fiber access network products described in this paper can effectively satisfy the EMC solutions throughout the processes of system design and product development. Based on test verification and practice proof, the system meets up to EMC industrial standards, and can save enormous manpower and material resources.

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Authors

Xiaochun Liu, she conferred with bachelor degree in management information system by Tianjin University of Commerce and master degree in management science and engineering by Xi'an Jiaotong University, Xiaochun Liu is currently a lecturer and doctoral candidate of Chang'an University. Her main research areas are analysis of transport information data and economic evaluation of intelligent transport system.

Dongping Hu, he conferred with bachelor degree in microelectronics by Hunan Normal University, Hu Dongping is currently a senior communication engineer of ZTE Corporation and a master candidate of Xi'an Jiaotong University. His main research area is communication electronics.