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A Design of Aircraft Grid Harmonic Detection Device using DSP and ARM

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Abstract

In order to detect the aircraft grid harmonic better, we design a kind of dual CPU harmonic detection device based on Digital Signal Processor (DSP) and ARM. Harmonic detection algorithm using the combination algorithm of FFT and wavelet transform. The measured signal through binary wavelet transform is separated into high frequency part and low frequency part, high frequency part by wavelet analysis can get the transient component, and low frequency part by FFT can get each steady-state harmonic parameters. By this method we can not only get the every steady-state harmonic component, but also determine the transient and sudden change signals. Design of ARM software adopts the embedded Real-Time Operating System (RTOS) of μC/OS-Ⅱ. This device makes full use of the powerful control ability of ARM and the powerful operation ability of DSP, and can achieve a precise measurement of the harmonic in aircraft grid.

Keywords: *FFT; Wavelet Transform; Harmonic Detection; DSP; ARM; μC/OS-II*

1. Introduction

Aircraft electrical system is an important part of the aircraft system. With the development of More Electric Aircraft, aircraft electrical equipment is becoming more and more, capacity is increasing and the nonlinear load is also more and more [1]. This makes a large amount of harmonic current in aircraft systems, causes a definite threat to the safety of the aircraft power grid operation, even endangering flight safety. Therefore, it is necessary to take action on the aircraft grid harmonic reduction. Harmonic detection is the precondition of harmonic suppression [2]. In the process of development of advanced aircraft, needing accurate detection of aircraft grid harmonic type, in order to make the reasonable design of the power grid and choose the appropriate power filter unit. In this paper, we design a kind of dual CPU aircraft power grid harmonic detection device based on DSP and ARM, by adopting the combination algorithm of FFT and wavelet transform. Using the device, we can realize the steady-state harmonic and transient harmonic detection of aircraft grid.

2. Choice of Algorithm

In theory, when the aircraft grid running smoothly, there are no transient components of the signal, by using Fourier transform can easily get the value of each harmonic. But when the system once appears abnormal state, the signal will inevitably contain transient or high frequency resonant interference [3], such as the starting process of the motor and electrical equipment failure process, on this occasion, using Fourier transformation is powerless. The wavelet transform is a powerful tool for analyzing non-stationary signal, it has incomparable advantages in the analysis of transient process compared with Fourier transform [4]. So we consider adopting the combination harmonic detection algorithm of Fourier transform and wavelet transform, using Fourier transform to steady-state harmonic detection, while using the wavelet transform to transient harmonic detection [5]. So when the system in a transient state we can also detect the aircraft grid harmonic.

The signal processing flow chart is shown in Figure 1.

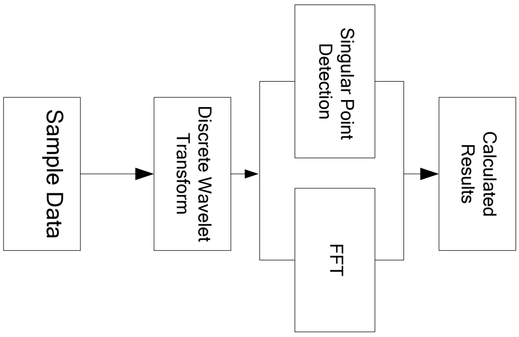

Figure 1. Signal Processing Flow Chart

After the dyadic discrete wavelet transforms, the original signal is decomposed into the high frequency part and low frequency part. Generally, singular signal components such as unsteady content and discontinuity point is in the details after wavelet transform, for this part using the analysis of modulus maxima [6]; for the low frequency part, because it is steady-state, so adopting Fourier analysis to get each steady-state harmonic component.

3. Design of Hardware

The combination harmonic detection algorithm of Fourier transforms and wavelet transform has a heavy computational load, so we must adopt a high-speed microprocessor system. Most of the DSP chip has hardware multiplier and accumulator, can finish multiplication and accumulation in a single instruction cycle, the speed of floating point operations per second can reach tens of millions of times and even hundreds of millions of times, and has a bigger superiority in the data processing [7].

ARM chip is a type of excellent embedded devices chip. Processor based on the ARM architecture on the market accounted for 90% of all 32-bit embedded RISC processors [8]. So this design adopts a dual CPU solution of DSP+ARM, DSP unit mainly completes the voltage and current signal acquisition and the wavelet transform and FFT arithmetic operations, and make full use of its advantages of data computation. As the main controller, ARM mainly to accomplish the control of the whole system, keyboard processing and communication function, *etc*. [9]. Through dual-port RAM, the DSP and ARM communication with each other and realize the fast data exchange.

This solution can make full use of the advantage of digital signal processing of DSP chip and the advantage of control of the ARM chip, and can easily achieve the algorithm of FFT and wavelet transform. We can also improve the operation speed and the processing efficiency of the system, and improve the cost performance of the hardware system. In this design the ARM chip using LPC2294 microcontroller and the DSP chip using TMS320VC33 chip. This system includes the following main parts: Ac conversion module, data acquisition module, signal processing module, display module and communication module, *etc*. The general structure of the whole hardware is shown in Figure 2.

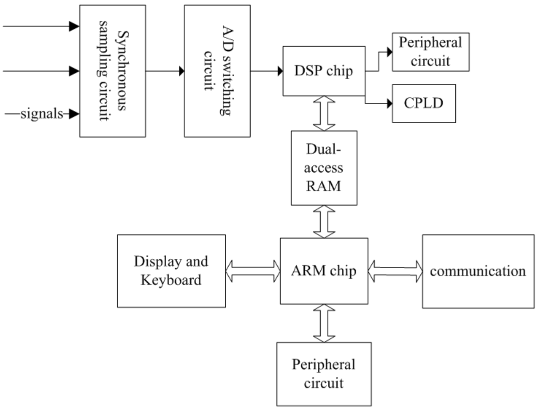

Figure 2. General Structure of the Whole Hardware

3.1. Ac Conversion Module

In the workplace, the input voltage and current amplitude are much higher than the design data acquisition system is able to deal with directly. Therefore, to complete the voltage and current sampling, we must transform the voltage and current to the signal which suitable for the A/D sampling. In order to achieve EMC performance, there must be an isolation between the input circuit with the internal circuit. So we need to process the input voltage and current signal through a voltage transformer and current transformer. The working principle is shown in Figure 3.

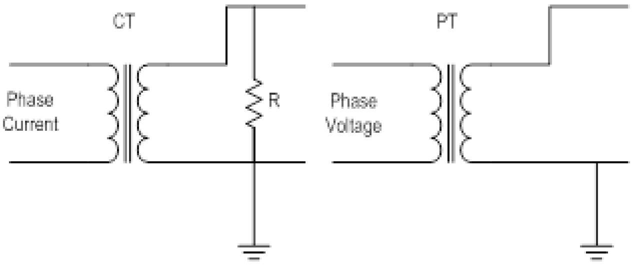

Figure 3. Principle Diagram of CT and PT

3.2. Anti-Aliasing Filter Circuit

According to the Shannon sampling theorem, in order to avoid the frequency aliasing, must meet $f_c \le 1/2 f_s$, so need filter the frequency which higher than 1/2 f_s [10], in addition, the test signal after Ac conversion device will inevitably mixed with some high frequency noise. Therefore, an anti-aliasing filter circuit must be equipped before the AD conversion circuit, avoid causing the problem of spectrum aliasing distortion.

The higher order number (N) of Butterworth filter, the faster rate of descent of amplitude, and the transition band will become narrower [11], so the cutoff frequency selectivity will be better. In order to improve the signal selectivity, we must choose the appropriate value of N, the choice of N is determined by the following formula:

$$N = -\frac{\lg k_{sp}}{\lg \lambda_{sp}} \tag{1}$$

$$k_{sp} = \sqrt{\frac{10^{\alpha_p/10} - 1}{10^{\alpha_s/10} - 1}} \tag{2}$$

$$\lambda_{SP} = \frac{\Omega_S}{\Omega_P} = \frac{2\pi f_s}{2\pi f_p} \tag{3}$$

α_p is the passband maximum attenuation coefficient, α_s minimum stopband attenuation coefficient, f_p is cut-off frequency passband, is stopband cutoff frequency. From the formula we can find that the higher order number of filters, the pass band attenuation is smaller, the stopband attenuation is bigger, and the cut-off frequency between passband and stopband is narrower. In order to increase the reliability and precision of the system, lower power consumption and reducing the volume, using MAX275 chip produced by the MAXIM Company to design the filter. The peripheral resistance using E24 series resistance, there is no potentiometer. The design of the filter is shown in Figure 4.

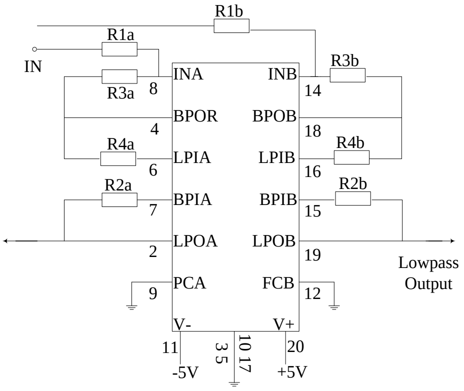

Figure 4. Design of Low Pass Filter

3.3. Synchronous Sampling and PLL Circuit

This design adopts FFT algorithm, after the FFT transformation, the leakage effect and fence effect caused by the grid frequency drift, can lead to inaccurate frequency, amplitude and phase [5]. So the data sampling must adopt a strict synchronous sampling method.

We use phase-locked loop circuit to achieve the goal of synchronous sampling. The circuit includes an integrated phase-locked loop (PLL) chip of CD4046, square wave generating circuit and 12 bit binary serial frequency division circuit chip of CD4040. The input signal through the square wave generating circuit can produce a square wave, and then send to the input terminal of PLL and the frequency multiplier circuit. The input voltage signal through 14 pin connection into the CD4046 phase comparator, after phase locked by CD4046, the frequency from CD4040 13 pin to CD4046 3pin is consistent with the original input signal frequency. Then, CD4046 generates a frequency of 128 times the input signal pulse as input of the CLK port of CD4040. Q1 to Q4 port of CD4040 are corresponding to 1, 2, 4, 8 divider output. This design need to produce 128 times frequency, so choose Q1 as an output port, provides signal for MAX125 port. CD4046 can make a corresponding change with the change of input frequency and ultimately locking. The PLL and frequency doubling circuit do not need the intervention of the software, and because all the circuit functions are completed by the hardware, so with the very high detection rate. The structure of the circuit is shown in Figure 5.

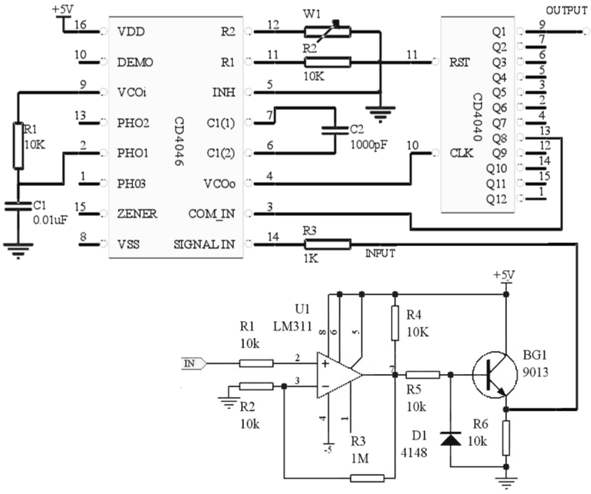

Figure 5. PLL and Frequency Doubling Circuit

3.4. A/D Converter Circuit

This design adopts the MAX125 chip as an A/D conversion device, due to the collected signals of the system is six-way of three-phase voltage and the three-phase currents, considering the synchronous change of voltage and current, we need two pieces of MAX125 to complete [12]. By default, the sample and hold amplifiers output of MAX125 transformation from 1 to 4 channels in turn, when all four channels transformation complete it will generate an interrupt signal. We can reprogram the two-way parallel port of MAX125, make its transformation only 1 to 3 channels, one chip collects the three-phase voltage signals and another one collects the three-phase current signals. Then two pieces of MAX125 can complete the data collection work of three-phase voltage and three-phase current.

Working process is as follows: Using TCLK1 of TMS320VC33 on-chip timer 1 as an A/D conversion start signal, the rising edge of the clock signal starts MAX125 to transform from channel 1 to channel 3 until all three channels completely. After the signal conversion, MAX 125 can produce an external interrupt signal $\overline{INT}$, namely the interrupt signal $\overline{INT}$ is low. The first piece of MAX125 INT and TMS320VC33 INT1 is linked together and the second piece of MAX125 INT is connected to the TMS320VC33 INT2. The interrupt signal is generated by the AND operation of the signal converted of two pieces of MAX125, then cause DSP interruption, and drive the interrupt service program, read the A/D conversion data.

Due to the MAX125 is +5V power supply device, and TMS320VC33 is a +3.3V power supply device, so their interface must be level match, this design uses a LVCH16245A chip. Output of D0 to D13 of MAX125 after A/D conversion can through a 16-bit transceiver channel LVCH16245A by parallel cable send to the DSP under the control of CPLD, and then can data processing after a cycle period or more. The schematic of the A/D converter circuit is shown in Figure 6.

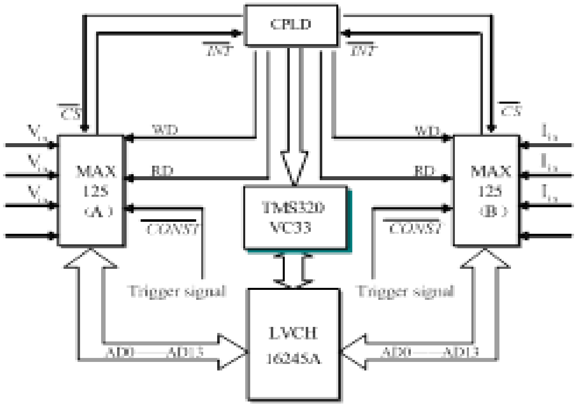

Figure 6. Schematic of A/D Converter Circuit

3.5. Design of DSP Peripheral Circuit

When using TMS320VC33 to form an application system, the first thing to consider is using the least amount of components to meet the requirements of the application system, this is known as a minimum system [13].

As harmonic detection, the design of minimum system should include an anti aliasing filter, PLL, sampling keeping circuit, etc. And also include oscillator, reset, serial port communication, power management circuits, as well as the extension of memory. Such design of a minimum system makes full use of the function of DSP chip, and cost saving.

3.5.1. Memory Expansion Circuit: TMS320VC33 has 16M×32bit addressable storage space, consisting of four separate optional address space, respectively is 000000h~3FFFFFH, 400000~7FFFFFH, 800000h~BFFFFFh and C00000h~FFFFFFh. Because its on-chip memory RAM is only 34K×32bit, in order to meet the needs of the system, this system extends the two pieces of data memory of IS61LV25616AL and a piece of program memory of AT29LV1024. Address of Data storage and program memory is respectively: 040000h~7FFFFH and 000000h~00FFFFH, chip selection of storage and control signal is generated by CPLD.

3.5.2. Design of TMS320VC33 Clock Circuit: Design of TMS320VC33 clock circuit has two methods: one is using the DSP internal oscillator circuit; another one is using an encapsulated crystal oscillators, make it input the EXTCLK pin, XOUT impending and XlN grounded. We adopt the second method [13].

3.5.3 Reset Circuit: Reset of TMS320VC33 including electric reset, manual reset and watchdog reset. In order to make the system reset correctly, the reset signal pulse width must be maintained at least more than 10 instruction cycles, because the TMS320VC33 instruction cycle is 13ns, so the reset time is at least 130 ns. In addition, the system has stable at work also need at least 20 ms, so the reset circuit should produce low level reset pulse from 100 to 200 ms. The reset circuit is shown in Figure 7, which have a combination of manual and automatic reset function.

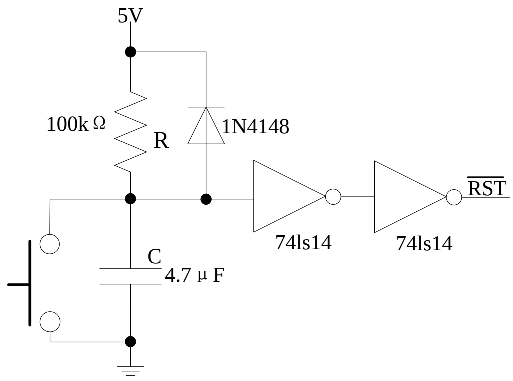

Figure 7. Reset Circuit

3.5.4 Power Source Management Circuit: Power source in this system is mainly the following types: the DSP needs 3.3V digital voltage; the ARM needs 5V, 3.3V, and 1.8V digital voltage; the peripheral analog chips need a 5V analog voltage. In order to reduce the power supply noise and interference, this system using an independent power supply of digital circuit and analog circuit. The input voltage of the system is 5V, 3.3V and 1.8V, voltages are obtained by designing SPX1117 chip.

3.6. DSP and ARM Data Communication Circuit

The data communication between DSP and ARM through the dual port RAMS to implement. The Chip we use is 16*16K dual port RAM of IDT7026. The dual port RAM with two sets of independent data, address and control bus, can allow two ports access to any address of the memory at the same time, when they access the same storage unit at the same time, on chip bus arbitration logic can solve this problem. Through the dual port RAM, the DSP and ARM can be convenient for a variety of data exchange. This design is easy to implement, and has good real-time performance. The principle of DSP and ARM data communication diagram is shown in Figure 8.

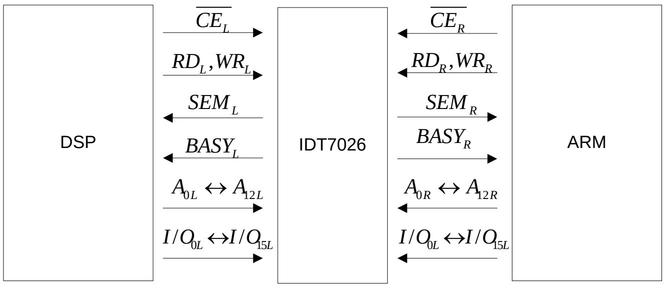
DSP
$\overline{CE_L}$
RD_L, WR_L
SEM_L
$BASY_L$
$A_{0L} \leftrightarrow A_{12L}$
$I/O_{0L} \leftrightarrow I/O_{15L}$
IDT7026
$\overline{CE_R}$
RD_R, WR_R
SEM_R
$BASY_R$
$A_{0R} \leftrightarrow A_{12R}$
$I/O_{0L} \leftrightarrow I/O_{15L}$
ARM

Figure 8. Principle Diagram of ARM and DSP Data Communication

3.7. Keyboard and Display Circuit

This design uses the keyboard as the input unit of the device. The keyboard has two kinds of independent type buttons and determinant buttons. In this design, we only need the six keys of →,←,↑,↓ ,confirm, exit, so we adopt the way of independent type buttons. The output is directly connected to the I/O port of the ARM. Reset button of the system set up separately, in order to prevent accidentally cause a reset operation. The design of the keyboard is shown in figure 9.

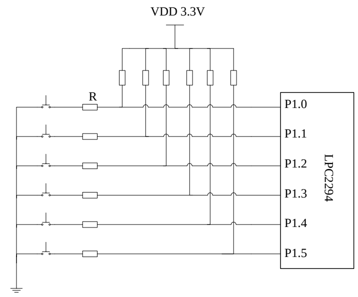

Figure 9. Design of Keyboard

In this design, the Liquid Crystal Display (LCD) control module is selected SED1335 LCD display control chip by the Japanese SEIKO EPSON Company. There is control, drive and interface three parts of the SED1335. Among them, the control part is the core components, consists of an oscillator circuit, functional logic circuit, video memory management circuit, character repertoire management circuit and timing generator. Design of SED1335 display driver needs to display data RAM. We use two piece of ISSI 62LV256 as a video memory, a total of 64K. The design of video memory of SED1335 is shown in Figure 10.

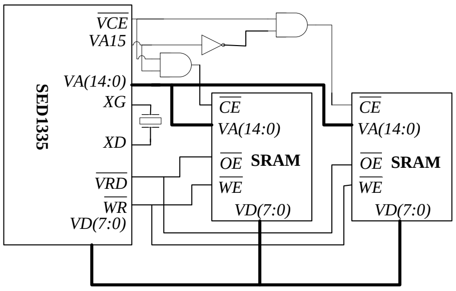

Figure 10. Design of Video Memory of SED1335

LCD module uses LM2028 module, which has its own word stock, with a resolution of 320*240. The drive signal pins of SED1335 are connected to the corresponding pins of the LCD display module, SED1335 can produce the LCD display directly. The interface of SED1335 has strong function of I/O buffers, when the CPU accesses SED1335 doesn’t need to judge whether or not busy. In addition, SED1335 in the interface set up two kinds of operation sequential circuit adaptation of 8080 series and M6800 series CPU. Through the pin level Settings, can choose any one of the two. Because the LCD is low-speed devices, ARM processor in the read/write cycle must be inserted into the appropriate waiting period.

3.8. Design of Communication with Host Computer Circuit

The communication with the host computer adopts the RS-232 standard. In contrast to the logical way of LPC2294. RS-232-C standard adopts negative logic, logic "1" corresponds to -5v~-15V level, while the logic "0" corresponding to +5v~+15V level, therefore, through signal level conversion to achieve communication between each other [14]. This design uses MAX232 chip as a level conversion circuit. The communication with host computer circuit is shown in Figure 11.

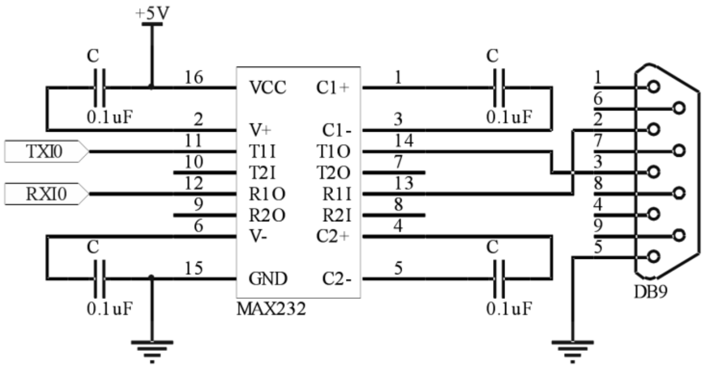

Figure 11. Interface of RS-232

3.9. Design of LPC2294 Peripheral Circuit

LPC2294 peripheral circuit including external memory, reset circuit, debugging interface, etc.

External memory including flash memory and SDRAM. Flash memory belongs to nonvolatile memory, mainly used as store the program code, constants and some user data need to save after power off, etc. The Flash memory in this design adopts two HY29LV160 chip parallel building a 32-bit memory system. SDRAM has no features of nonvolatile, but it is high access speed, and can be read/write. In the system, it is primarily used as the running space of program and data and stack area. The SDRAM in this design uses two HY57V641620 chips parallel building a 32-bit SDRAM memory system, a total of 16 MB SDRAM space and can meet the requirements of this system.

In order to improve the reliability of the system, the reset circuit using special microcontroller power source monitoring chip of SP708S. The interface debugging circuit adopts ARM JTAG standard 20 pin simulation debugging interface.

4. Overall Design of Software

The design of system software is divided into two parts: DSP program module and ARM based on an embedded operating system. The DSP program module is mainly responsible for time sampling, data processing, etc. The ARM is mainly responsible for communication with a host computer and control functions, etc. The use of embedded operating system can make the design of embedded device more convenient and flexible, it can also cost savings, improve the reliability and stability of the system. So for the ARM part, we adopt the real-time embedded operating system of μC/OS-Ⅱ, by μC/OS-Ⅱ to control the file management, storage, communication, keyboard and display of the whole system and also control the communication with DSP. This method not only can improve the security and reliability of the system, but also can reduce the development time, cost savings. For the DSP part, because it is mainly used as signal processing, so we adopt the independent programming of DSP for data acquisition and processing work. The overall structure of the system software design is shown in Figure 12.

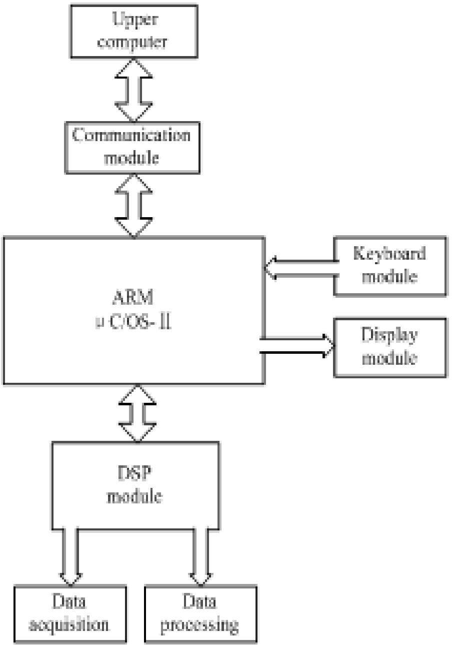

Figure 12. Overall Structure Design of the System Software

5. Porting μC/OS-Ⅱto LPC2294

5.1. μC/OS-Ⅱ Kernel

Real-time embedded operating system adopts the kernel to manage each task, allocate the CPU time, and is responsible for the communication between each task. The basic task of the kernel is task switching. The applications can be divided into several tasks and managed by the real-time kernel [15]. Using a real-time kernel can greatly simplify the design of an application system.

From the structure of μC/OS-Ⅱ kernel, it can be divided into five parts: core sections (OS_CORE.C), task processing (OS_TASK.C), time part (OS_TIME.C), synchronization and communication between tasks, porting relevant part. Porting relevant part refers to the porting part of the μC / OS-Ⅱ for a specific CPU. Because μC/OS-Ⅱ is a generic operating system, so for the LPC2294 chip, we need to do the corresponding porting to meet the requirements.

5.2. Required Conditions of Porting μC/OS-Ⅱ

Porting means to make a real-time kernel can run on a micro controller. In order to facilitate porting, most μC/OS-Ⅱ codes are written in C language, but μC/OS-Ⅱ can only through the assembly language when reading and writing processor registers, so some processor dependent codes need to be rewritten in C and assembly language. When porting μC/OS-Ⅱ to different processor platform, we need to solve the redefinition of the data type, the design of stack structure and the state save and recovery when task switching.

In addition, if we want μC/OS-Ⅱ run smoothly, the processor must also meet the following requirements: 1. C compiler of the processor can generate reentry code. 2. Can open and close interrupt with C language. 3. The processor support interrupt, and can produce a timer interruption (usually between 10 to 100 Hz). 4. The processor can support a certain amount data (which may be a few thousand bytes) hardware stack. 5. The processor has the stack pointer and the instructions to read and store other CPU register or memory to the stack. LPC2294 processor based on a kernel of ARMT7DMI-S is fully meeting the above conditions, so we can porting µC/OS-Ⅱ to LPC2294.

5.3. Concrete steps of Porting

The structure of µC/OS-Ⅱ and its relationship with the hardware is shown in Figure 13.

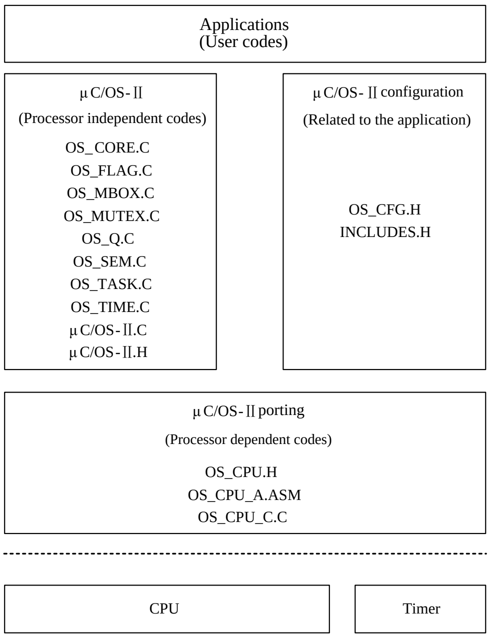

Figure 13. µC/OS-Ⅱ Hardware/Software System Structure

Processor dependent codes are key part of porting. Porting µC/OS-Ⅱ need to modify the OS_CPU.H, OS_CPU_A.ASM and OS_CPU_C.C. When writing programs based on µC/OS-Ⅱ, need to rewrite two files of OS_CFG.H and INCLUDES.H. OS_CFG.H file predefined a lot of switching value which configuring the kernel service function and some µC/OS-Ⅱ related constants. We can configure the file depending on the characteristics of the specific application. Concrete steps of porting are as follows:

1. INCLUDES.H

INCLUDES.H is a header file that contains each header file of *.C file of user programs. It can be used to enhance code portability. At the same time, users can edit INCLUDES.H to increase their own header file, but the user's header file must be added at the end of the list of header files.

```
/********µC/OS-Ⅱ dependent codes********/
#include   "os_cpu.h"
#include   "os_cfg.h"
#include     "ucos_ii.h"
```

2. OS_CPU.H file changes

OS_CPU. H file includes compiler dependent data type, processor dependent data type, definition of stack types, definition of interrupt handling and statement of stack growth mode. Unlike data types of C language, µC/OS-Ⅱ redefines the data types. In the design, we adopt ADS 1.2 compiler, the data types supported respectively are char (8bit), short (16bit) and int (32bit). The concrete codes are as follows:

```
typedef unsigned char BOOLEAN;      // Boolean variable
typedef unsigned char  INT8U;      // Unsigned 8-bit integer variables
typedef signed   char  INT8S;      // Signed 8-bit integer variables
typedef unsigned short INT16U;      // Unsigned16bit integer variables
typedef signed   short INT16S;      // Signed 16bit integer variables
typedef unsigned int   INT32U;      // Unsigned32bit integer variables
typedef signed   int   INT32S;      // Signed 32bit integer variables
typedef  float       FP32;      // Float-point number with single precision (32bit)
typedef  double      FP64;      // Float-point number with double precision (64bit)
typedef  INT32U  OS_STK;          // Stack is 32bit
//********Macro definition********//
#define OS_STK_GROWTH    1      // The stack from top to bottom
_swi(0x02) void OS_ENTER_CRITICAL(void);      //Disable IRQ
_swi(0x03) void OS_EXIT_CRITICAL(void);      // Enable IRQ
_swi(0x00) void OS_TASK_SW(void);      // Task switching
```

µC/OS-Ⅱ is same as all of the real-time kernel, needing to disable interrupt before accessing to the critical section of code, and allow the interrupt again after access completed. This makes µC/OS-Ⅱ can protect critical section of code from the destruction of multiple tasks or interrupt service routine. µC/OS-Ⅱ defines the OS_ENTER_CRITICAL() and OS_EXIT_CRITICAL() two macros to prohibit and allow the interrupt.

3. OS_CPU.C file changes

OS_CPU.C file changes are the core of porting, also has the biggest workload. The porting of µC/OS-Ⅱ requires the user to write ten simple C language functions: 1. OSTaskStkInit(); 2. OSTaskCreateHook(); 3. OSTaskDelHook(); 4. OSTaskSwHook(); 5. OSTaskIdleHook(); 6. OSTaskStatHook(); 7. OSTimeTickHook(); 8. OSInitHookBegin(); 9. OSInitHookEnd(); 10. OSTCBInitHook(). In these functions, the only necessary function is OSTaskStkInit(), other nine functions must be declared can contain code. When need for additional extensions, can add your own code in the nine functions. OSTaskCreate() or OSTaskCreateExt() by calling OSTaskStkInt() to initialize the stack structure.

4. OS_CPU_A.ASM file changes

Due to those codes operate the processor registers, so should be written in assembly language, it includes four subfunction: OSStartHighRdy(), OSCtxSw(), OSIntCtxSw() and OSTickISR().

OSStartHighRdy() is used to run the ready task with the highest priority, is called when starting the function of OSStart() in the multitask system. This function is executed only once when multitask start, used to launch a ready state, also is the highest priority task execution.

OSCtxSw() and OSIntCtxSw() are task switching functions. OSCtxSw() is called in the task and OSIntCtxSw() is called in the interrupt service routine. OSCtxSw() function is called by task level task switching function of OS_TASK_SW() to realize the switch from low priority to high priority.

When OSIntCtxSw() finds a higher priority task waiting clock signal arrival in clock interrupt ISR (interrupt service routine), it will call the ready high-priority task execution but do not return the interrupted task.

OSTickISR() is the interrupt service function of ticks of system time, and belongs to the periodic interruptions， it provides the ticks for the kernel. Its cycle determines the size of the minimum time interval that the kernel provides to applications.

6. Extended RTOS Architecture of μC/OS-Ⅱ

The successful porting of μC/OS-Ⅱ to the ARM chip is only part work of the software design of embedded system, μC/OS-Ⅱ is only the kernel responsible for the task scheduling [15]. In order to complete the whole system must also be extended based on μC/OS-Ⅱ, which including: to establish a file system, build drivers and specification corresponding API functions for peripheral equipment, create graphical user interfaces, establish other application interface *etc*.

According to the different task, the operating system can be divided into the following modules:

1. Hardware of the peripheral equipment. This part includes LCD, communication module, keyboard, storage, calendar and clock of the system. Hardware of the peripheral equipment is the underlying hardware to ensure the system to achieve the custom task.

2. Driver module. The drivers connect the underlying hardware equipments and upper Application Program Interface (API) functions. It can separate the API functions of the operating system from underlying hardwares. When any hardware is changed, deleted, or added, only need to delete or add the hardware drivers and will not affect the function of API functions and user programs.

3. API functions of the operating system. The operating system provides standard API functions, and can accelerate the development of user applications and provides convenience for the upgrade.

4. Multi-task management of RTOS. The main task of the μC/OS-Ⅱ kernel is scheduling and synchronization between the multitask.

5. System message queue. The message queue is derived messaging mechanism of μC/OS-Ⅱ system, which is used to implement various tasks in the system, every task of user applications and the communication between user tasks with system tasks.

6. System tasks. System tasks of μC/OS-Ⅱ include refresh of LCD and keyboard scanning task, they will run along with the system boot.

7. Users application. The user applications are based on the Main_Task, mainly through the system API functions to operate.

In this design, the peripheral equipments mainly are the serial port, LCD and keyboard. Through peripheral drivers can make the system access peripheral equipments interfaces, and separate the operating system from peripheral equipments. The serial port, LCD, keyboard driver is as follows.

1. Serial port drives

Serial port conform to RS-232 standard, the highest speed can be achieved 1152000bps, the serial port interface functions are as follows:

Uart_Init

Definition: void Uart_Init(int Uartnum,int mulk,int baud), the function is to initialize the serial port and set the baud rate for serial communication.

Uart_Printf

Definition: void Uart_Printf(*char fmt,…), the function is output strings to serial port 0.

Uart_Getch

Definition: char Uart_Getch(int Uartnum), the function is to accept the specified serial data and return when receive data.

Uart_SendByte

Definition: void Uart_SendByte(int Uartnum,int data), the function is to send data to specified serial port.

2. LCD drives

LCD_Init

Definition: void LCD_Init(void), the function is to initialize LCD, called when the system starts.

LCD_printf

Definition: void LCD_Printf(*char fmt,…), the function is output strings in the text mode of the LCD.

LCD _Changemode

Definition: void LCD_Changemode(U8 mode), the function is to change the LCD display mode.

LCD_Refresh

Definition: void LCD_Refresh(), the function is to refresh the LCD display.

3. Keyboard drivers

GetKey

Definition: U32 GetKey(), the function is low 16 bits are keyboard number and high 16 bits are the corresponding function keys scan codes, 1 valid. This function is a deadlock function, unless there is a key press after called, or they will not be returned.

SetFunctionKey

Definition: void SetFunctionKey(U16 Fnkey), the function is to set the scan codes, 1 valid.

GetNoTaskKey()

Definition: U32 GetNoTaskKey(), the function is low 16 bits are keyboard number and high 16 bits are the corresponding function keys scan codes, 1 valid. This function is a deadlock function, unless there is a key press after called, or they will not be returned.

7. Design of DSP Software

The DSP program is mainly responsible for data acquisition and data calculation and processing. The flow chart of the DSP routine is shown in Figure 14.

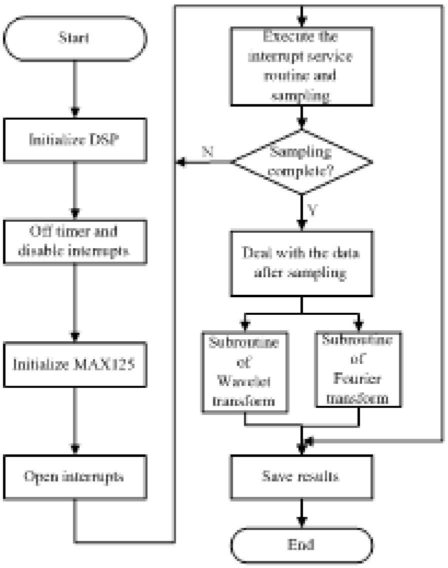
Start
Initialize DSP
Off timer and disable interrupts
Initialize MAX125
Open interrupts
Execute the interrupt service routine and sampling
Sampling complete?
N
Y
Deal with the data after sampling
Subroutine of Wavelet transform
Subroutine of Fourier transform
Save results
End

Figure 14. Flow Chart of the DSP Routine

7.1. Data Collection Subroutine

When MAX125 get a switching pulse, will synchronous sample 3 channel signals, hold and convert 3 channel signals in sequence. After the conversion, it will output a low pulse signal. The system uses this signal as an external interrupt signal and uses interrupt mode to read data in turn. Because read-write speed of MAX125 does not match VC33, so should insert at least three waiting cycle to receive the correct data, so should insert at least three waiting cycle to receive the correct data. In addition, the signal after MAX125 conversion is 14bit signed integer, the integer of VC33 is 4 bytes, and what we need is a floating point format in the operation. So the program must convert 14bit signed integer to 32bit signed integer and then convert to a 32bit floating point format. The flow chart of the data collection is shown in Figure 15.

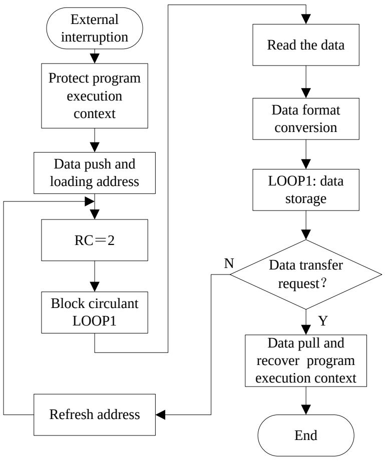

Figure 15. Flow Chart of the Data Collection

7.2. Data Processing Subroutine

The data processing subroutine includes two parts. One is the wavelet processing subroutine and the other one is FFT subroutine. The data processing flow chart is shown in Figure 16.

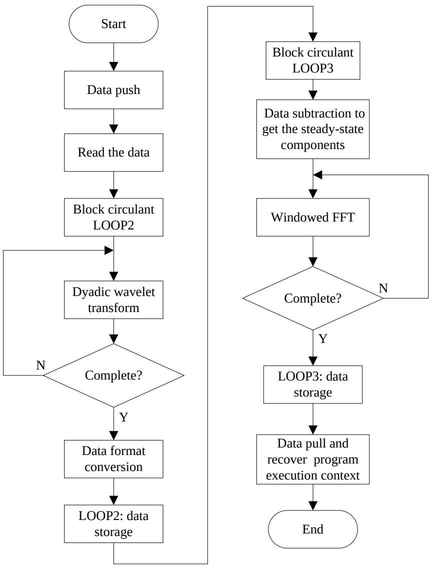

Figure 16. Flow Chart of the Data Processing

In the process of wavelet analysis, we need for signal singularity detection and diagnosing processing. The signal singularities will appear modulus maxima after wavelet transforms [16]. So using the wavelet transform modulus maxima denoising algorithm to detect the power system signal singularity and denoising. The denoising algorithm using the wavelet modulus maxima analysis is shown in Figure 17.

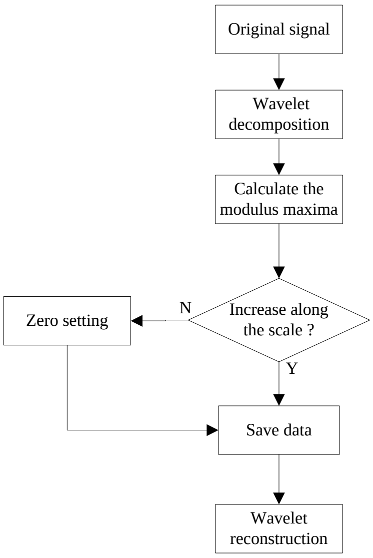

Figure 17. Flow Chart of Denoising Algorithm using Wavelet Modulus Maxima analysis

FFT subroutine is shown in Figure 18.

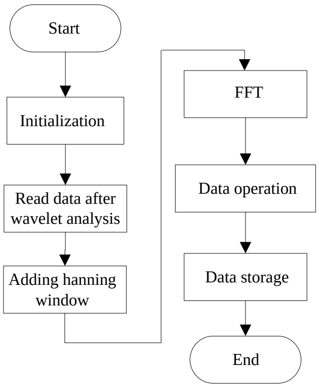

Figure 18. Flow Chart of FFT

8. Conclusion

Compared with the harmonic detection device on the market, this device has great advantages in both the algorithm and the design of hardware and software. This device adopts combined aircraft grid harmonic detection algorithm of FFT and wavelet transform, and can realize the both detection of steady-state harmonic components and transient harmonic components. The using of dual CPU architecture of the ARM and DSP and using the embedded RTOS of μC/OS-Ⅱ, can reduce the development difficulty, improve the stability of the system, and ensure the real-time and accuracy of the harmonic measurement. This device can provide accurate harmonic data support to the aircraft grid harmonic suppression.

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