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Design of Exclusive-OR Logic Gate on Quantum-Dot Cellular Automata

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Abstract

Most of Exclusive-OR(XOR) logic gates on quantum-dot cellular automata(QCA) is based on configuration of 2-input, and they are hardly to be scalable and exists unbearable noise because they are only focused on decrease of latency and space. In this paper, we propose how to make a scalable logic using a wire crossing technique, and give examples of two expanded XOR gate using typical logic gates on QCA. The designed logics are simulated and show accurate output results.

Keywords: *Quantum-dot cellular automata, Exclusive-OR logic gate, Wire crossing, Enable logic, QCA clocking*

1. Introduction

With the growth of very large scale integrated circuit (VLSI) technologies, various types of arithmetic and logic unit (ALU) or memory which can be the massive operation or a large capacity memory were proposed. Also, the reduction of feature sizes and the increase of processing power have been successfully achieved by this technology [2-10]. However, the development of VLSI technology was reached its peak owing to the fundamental physical limits of CMOS technology. We require new technologies which can overcome this limitation.

A quantum-dot cellular automata (QCA) is one of candidate technologies for the next generation. It is the computing with cellular automata consists of arrays of quantum-dot cells, and basic concepts of it were introduced by Tougaw and Lent [10, 11]. The inherent feature is that logic states are not stored in voltage levels as in digital circuits, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configurations The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits. In order to transmit data, QCA uses a clocking technique. It is operated by a tunneling barrier and quasi-adiabatic switching. Depending on the raising or lowering of tunneling barrier, the clocking technique consists of four stages: locking locked, relaxing and relaxed [11-14].

In QCA, there are various types of combinational and sequential circuits such as XOR logic gate, adder, multiplexer, decoder, counter, flip flop, ALU and memory [15-23]. Especially, XOR logic gate has been proposed in various configurations. They are divided into two types depending on using the wire crossing. Conventional types used wire crossing techniques such as coplanar-based, multilayer-based and difference of cell state. But latency of these gates is increased. On the other hand, latest types does not use wire crossing and were based on different types of Boolean algebra equations. Although they latency is less than it of conventional types, structure is not regular and scalable. Moreover, a total latency is increased

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depending on latency of each logic, when the number of inputs is multiple. Because they proposed just a 2-input XOR logic gate without consideration of scalability or expansion [24-27].

In this paper, we design and simulate a 3-input XOR gate using previous 2-input XOR logics on QCA. Like digital logic circuits, 3-input XOR logic gate is to operate an exclusive logical sum of 3-input. As the simulation results, we analyze the efficiency and performance between the proposed and previous techniques by QCADesigner [25, 29].

This paper is organized as follows. Section 2 introduces QCA basic concept and 2-input XOR logic gates. Designed 3-input XOR gates are discussed in section 3. Section 4 simulates mentioned logic gates, and analyzes the efficiency and performance between the proposed and previous techniques. Finally, section 5 gives our conclusions.

2. Related Works

In this section, we introduce basic concepts of QCA and previous XOR logic gates.

2.1. QCA Basic Concept

A typical QCA cell consists of four quantum dots located at each corner of a square as shown in Figure 1(a). It is expressed by an arbitrary state such as null or ground. When a cell was null state, electrons are moving freely between quantum dots. But, electrons are fixed as an arbitrary position, when a cell was ground state. They tend to attain maximal separation by occupying dots in opposite corners.

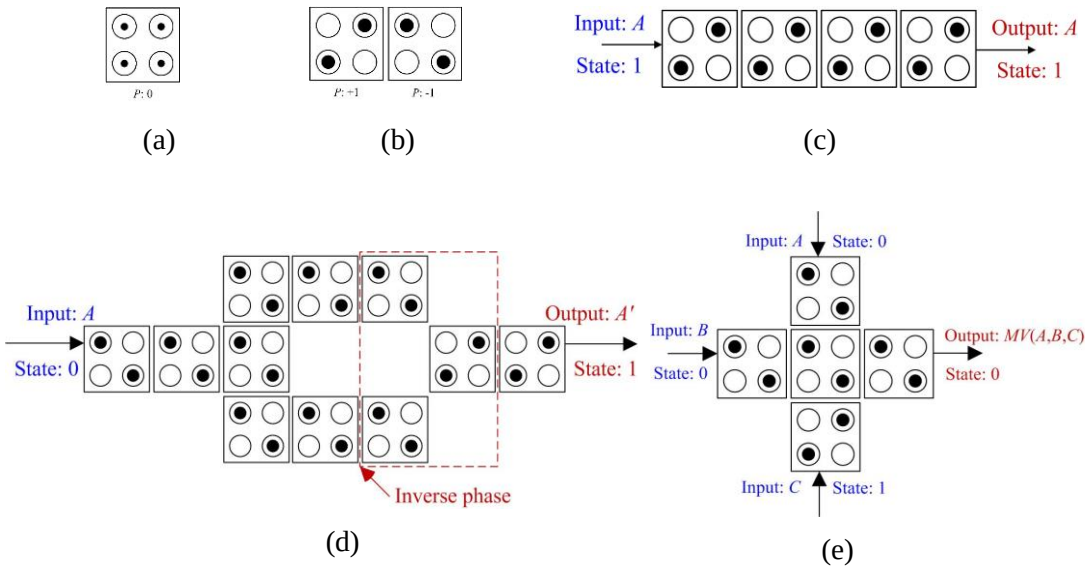


Figure 1. Basic QCA Structures: (a) a Cell at Null State, (b) Standard Cells at Ground State, (c) Binary Wire, (d) Formal Invertor and (e) Majority Voting Logic with 3input/1output

Two diagonal electron configurations correspond to two energetically equivalent ground states of a cell as shown in Figure 1(b). Demonstrated bistability allows representation of two binary logic values. The state of a cell is characterized with polarization P. The ground state configurations have polarization values of $P = +1$ and $P = -1$, which correspond to binary logic values '1' and '0', respectively [10-15].

When cells are placed in a linear array as shown in Figure 2(c), they tend to keep a polarization of input cell. Such arrangement acts as a binary wire, transmitting the logic value from input to output cell. Depending on array shape of cells, there exist two basic

logic gates such as inverter (INV) and majority voting (MV) gate as shown in Figure 2(d) and (e), respectively. INV inverts a logic value of input signal by Coulomb repulsion in an inverse phase. MV gate calculates 3-input majority logic function as $MV(A,B,C) = A \cdot B + B \cdot C + C \cdot A$, where '$\cdot$' and '$+$' indicate AND and OR Boolean logic function. Logic function AND is realized by majority gate with one of its inputs fixed to a permanent logic value 0. Similarly, if one of inputs is a constant 1, the majority gate implements a logic function OR. Thus, an arbitrary QCA circuit can be realized using wire, INVs and MV gates [10-23].

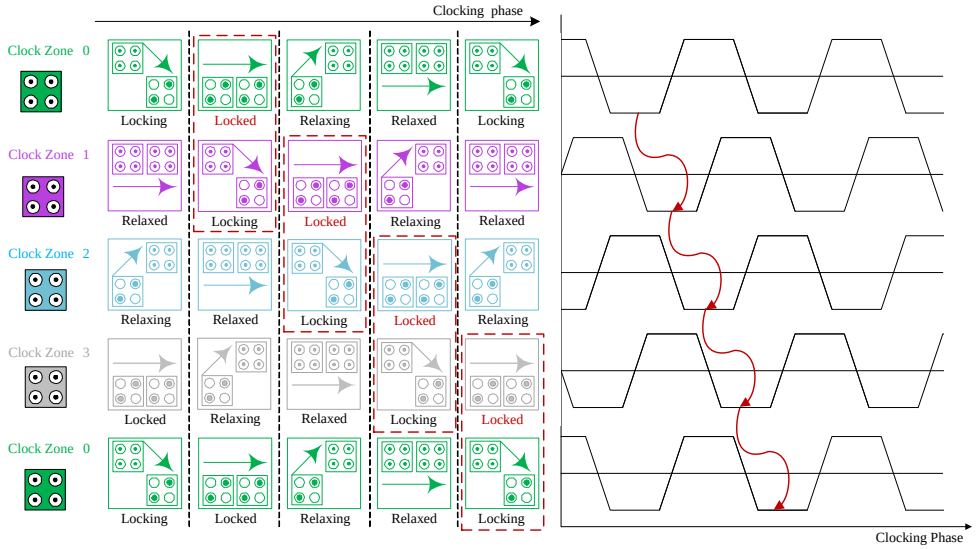


Figure 2. A Concept of QCA Clocking: (a) Four Distinct QCA Clock Stages and (b) Data Transmission between Two Clock Zones

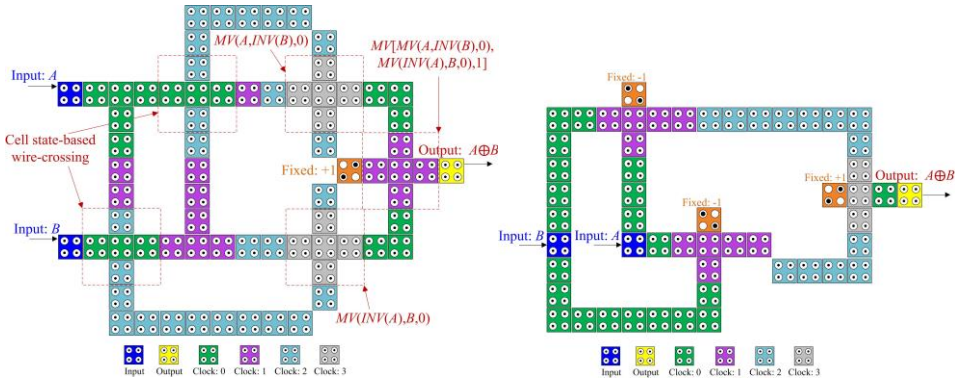
In order to transmit data, QCA uses a clocking technique based on the raising or lowering of tunneling barriers and quasi-adiabatic switching in a cell. The tunneling barriers are typically modulated through four separate stages as shown in Fig. 2: the locking stage that the tunneling barriers are raising, the locked stage that tunneling barriers are fully raised, and the relaxing stage that tunneling barriers are lowering, and the relaxed stage that tunneling barriers are completely lowered, allowing free electron movement within a cell. In two neighboring cells, data transmissions through two clock zones are performed as shown in Figure 2. Each cell has a different clock zone. Sequence of clock zone 0 is locking-locked-relaxing-relaxed. But, it of clock zone 2 is relaxed-locking-locked-relaxing. In this case, a difference of cell phase between clock zone 1 and 2 is 90°. When stages of clock zone 0 and clock zone 1 are locked and locking at the same time, there exists the data transmission from clock zone 0 to clock zone 1 [11-23]. Each clock zone is called a '*clock*', and one cycle consists of four clocks in this paper.

2.2. Previous XOR Logic Gates

There are two types of XOR logic gates on QCA according to applying wire crossing techniques. Many typical logic gates has used a wire crossing technique based on a Boolean algebra function as shown in Eq. (1) [24,25,28].

$$A \oplus B = A \cdot B' + A' \cdot B, \tag{1}$$

where '$\oplus$', '$\cdot$' and '$+$' indicate XOR, AND and OR Boolean functions, respectively.



(a) (b)

Figure 3. 2-Input XOR Logic Gates: (a) XOR Logic Gate Using Wire Crossing and (b) Latest XOR Logic Gate without Wire Crossing

Tougaw and Lent (TL) proposed XOR logic gate [24]. They used a coplanar-based wire crossing. This wire crossing technique has used standard and 45° rotated cells. But, there are some defeats such as occurrence of noise, consideration of the number of 45° rotated cells and decrease of Coulomb repulsion between 45° rotated cells. In order to overcome these defeats, Walus and Julian (WJ) proposed a XOR logic gate using multilayer-based wire crossing [25]. It was based on shape of an overpass, and can be more miniaturized because it is not need to rotate cells. Although this technique has some advantages, there are a noise problem between intersection cells in an overpass area and also several things to consider for design and simulation such as the number of layers, crossover and vertical cells. Shin et al. proposed a *XOR* logic gates using cell state-based wire crossing technique as shown in Fig. 3(a) [28]. It was based on QCA clocking and difference of cell state such as ground and excited. It does not exist noise and any problems such as the number of layers, crossover cells and rotated cells, but latency was increased by one clock.

On the contrary, some other researchers did not use wire crossing techniques [26, 27]. Beigh, *et al.*, proposed various types of *XOR* logic gate based on different Boolean algebra functions without wire crossing technique as shown in Figure 3(b) [27]. In order to reduce space and latency of logic gates, positions of input and output are placed inside of structure. Although space and latency of these logics were reduced, there exist additional tasks such like wire crossing or wire connection in order to connect other logics. Moreover, these logic gates are not provide a regularity, flexibility or scalability. In order to design a 3-input XOR logic gate, they used a concept of repeated twice in previous works. But, it demands increasing of latency and cell space.

3. Proposed 3-Input XOR Gate

In this section, we illustrate a design of 3-input XOR logic gate. We design two types of 3-input XOR logic gates using previous 2-input XOR logic gates. We select two different types of previous 2-input logic gates such as Shin, *et al.*, logic gate as shown in Figure 3(a) [28], Beigh, *et al.*, logic gate as shown in Figure 3(b) [27]. In wire crossing technique, we use a difference of cell state [28]. First XOR logic gate is designed using Shin et al.'s logic gate as shown in Figure 4. In order to design a logic gate in Figure 4, it demands two Shin, *et al.*, logic gates. It is expressed by Eq. (2).

$$A \oplus B \oplus C = MV(MV(A \oplus B, INV(C), 0), MV(INV(A \oplus B), C, 0), 1), \quad (2)$$

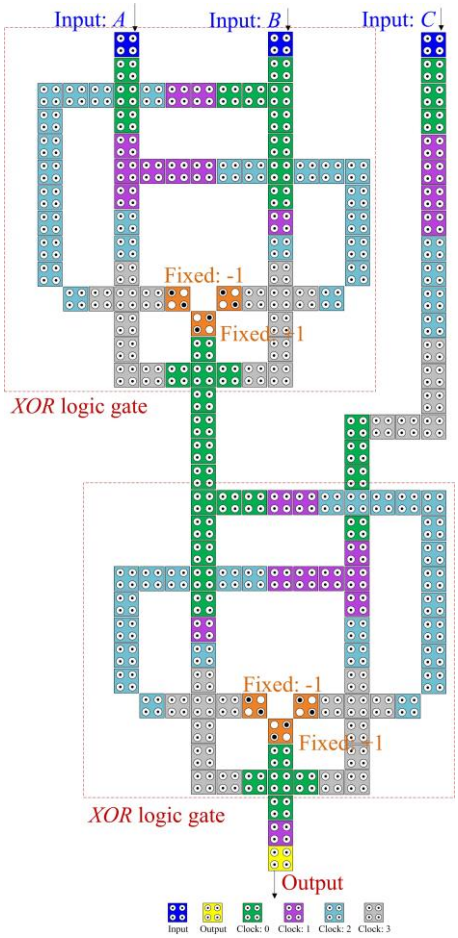


Figure 4. Configuration of 3-Input XOR Logic Gates Using Shin, *et al.*, Logic Gate

where '$A \oplus B$' is $MV(MV(A, INV(B), 0), MV(INV(A), B, 0), 1)$ in Shin et al.'s logic gate.

Second 3-input XOR logic gate is designed as shown in Figure 5. In order to design a logic gate in Figure 5, it demands two Beigh, *et al.*, logic gates as shown in Figure 3(b) and another wire crossing which is required because one input is located inside the gate. It is expressed by Eq. (3).

$$A \oplus B \oplus C = MV\big(INV\big(MV(A \oplus B, C, 0)\big), MV(A \oplus B, C, 1), 1\big), \quad (3)$$

where '$A \oplus B$' is $MV\big(INV\big(MV(A, B, 0)\big), MV(A, B, 1), 1\big)$ in Beigh et al's logic gate.

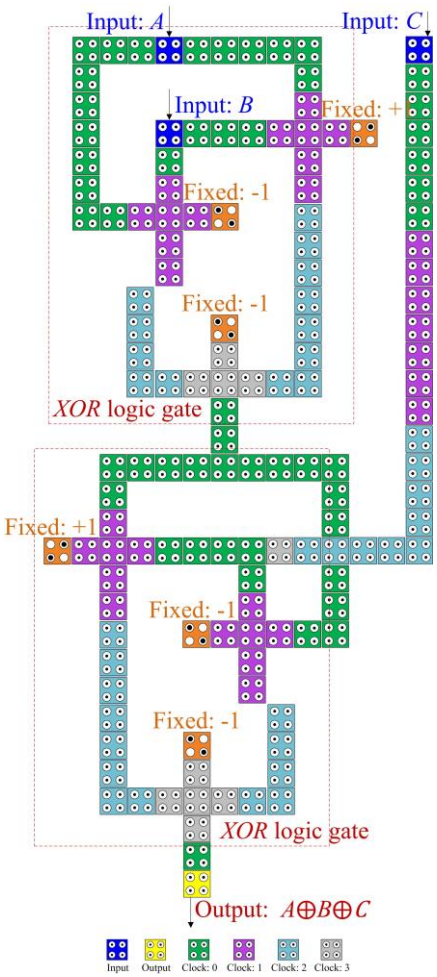


Figure 5. Configuration of 3-Input XOR Logic Gate Using Beigh, *et al.*, Logic Gate

4. Simulation and Analysis

In this section, we have simulated and analyzed two different types of 3-input XOR logic gate using bistable model and QCA Designer [25, 29].

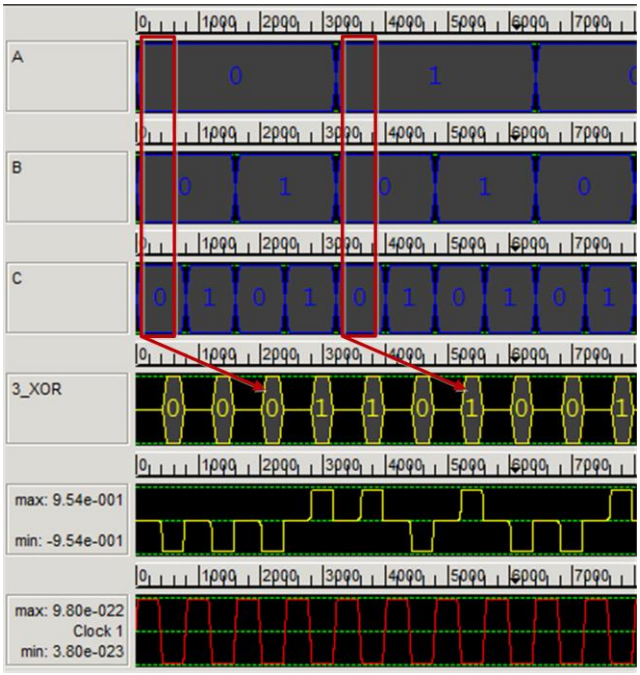


Figure 6. Simulation Results of Figure 4

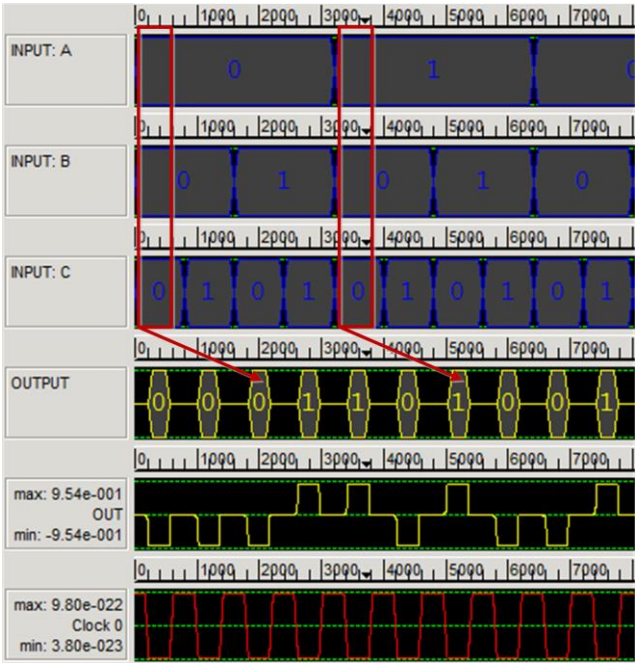


Figure 7. Simulation Results of Figure 5

In simulation result of first logic gate as shown in Figure 6(a), output is always the same result regardless of order of inputs because it was based on $A \cdot B' + A' \cdot B$ Boolean function. But, output of second logic gate as shown in Figure 6(b) is different depending on the order of inputs because of feature of Eq. (3). So, we have adapted such as $(A \oplus B) \oplus C$. As the results, these are shown that designed two gates did not affect surrounding wires, and we obtained accurate output values with high kink energy.

Table 2. Comparison of Two Different Types of 3-Input XOR Logic Gates

3-input XOR logic gates	Used cell (cell)	Cell space (μm^2)	Latency (clock)
First logic gate(Figure 4)	164	0.23	10
Second logic gate(Figure 5)	136	0.18	9

In order to estimate an efficiency of typical QCA circuits, we use three terms such as a cell space, the number of used cells and latency. Table 2 shows the detail comparison results of 3-input XOR gate. As you see in Table 2, all Figure 4 demands more cells, cell space and clocks but it has better scalability compared to Figure 5 which has one input at the inside of circuit. However, two types of 3-input XOR gate are very regular architecture and stable.

5. Conclusions

In this paper, we designed and simulated two different types of 3-input XOR gate using 2-input logics. First logic gate was more scalable, but second logic gate was more efficient. Simulation was performed by bistable model and QCADesigner. In first logic gate, output has always the same result regardless of the order of inputs while output was different depending on the order of inputs in second logic gate because of inherent feature of equation. However we obtained accurate output values with high kink energy for both circuits.

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References

[1]. A. J. Menezes, P. C. Oorschot, and S. A. Vanstone, Handbook of applied cryptography, CRC press, **(1996)**.
[2]. K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey", Solid-State Circuits, IEEE Journal of, vol. 41, no. 3, **(2006)**, pp. 712-727.
[3]. K.-Y. Kim, S. Kim and J. Kang, "Construction of an RSFQ 4-bit ALU with half adder cells", Applied Superconductivity, IEEE Transactions on, vol. 15, no. 2, **(2005)**, pp. 308-311.
[4]. S. Pontarelli and O. Marco, "Error detection and correction in content addressable memories by using bloom filters", Computers, IEEE Transactions on, vol. 62, no. 6, **(2013)**, pp. 1111-1126.
[5]. J.-C. Jeon, Analysis of Hash Functions and Cellular Automata Based Schemes, International Journal of Security and Its Applications, vol. 7, no. 3, **(2013)**, pp. 303-316.
[6]. B. Pandey, Y. Jyotsana, K. S. Yogesh, K. Rohit, and P. Sourabh, "Energy efficient design and implementation of ALU on 40nm FPGA", In Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, **(2013)**, pp. 45-50.
[7]. L. Fiorin and S. Mariagiovanna, "Fault-Tolerant Network Interfaces for Networks-on-Chip", Dependable and Secure, IEEE Transaction on, vol. 11, no. 1, **(2014)**, pp. 16-29.
[8]. W. Xu, Z. Tong, and C. Yiran, "Design of spin-torque transfer magnetoresistive RAM and CAM/TCAM with high sensing and search speed", Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 18, no. 1, **(2010)**, pp. 66-74.
[9]. B.-D. Yang, Y.-K. Lee, S.-W. Sung, J.-J. Min, J.-M. Oh and H.-J. Kang. "A low power content addressable memory using low swing search lines", Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 58, no. 12, **(2011)**, pp. 2849-2858.
[10]. C. S. Lent, P D. Tougaw, W. Porod and G. H. Bernstein, "Quantum cellular automata", Nano-technology, vol. 4, no.1, **(1993)**, p. 49-57.
[11]. C. S. Lent, P. D. Tougaw and W. Porod, "Bistable saturation in coupled quantum dots for quantum cellular automata", Applied Physics Letters, vol. 62, no. 7, **(1993)**, pp. 714-716.
[12]. P. D. Tougaw and C. S. Lent. "Dynamic behavior of quantum cellular automata", Journal of Applied Physics, vol. 80, no. 8, **(1996)**, pp. 4722-4736.

[13]. W. Porod, "Quantum-dot devices and quantum-dot cellular automata", International Journal of Bifurcation and Chaos, vol. 7, no. 10, **(1997)**, pp. 2199-2218.
[14]. A. Gin, P. D. Tougaw and W. Sara, "An alternative geometry for quantum-dot cellular automata", Journal of Applied Physics, vol. 85, no. 12, **(1999)**, pp. 8281-8286.
[15]. M. R. Azghadi, O. Kavehie and N. Keivan, "A novel design for quantum-dot cellular automata cells and full adders", Journal of Applied Sciences, vol. 7, no. 22, **(2007)**, pp.1204-2048.
[16]. H. Cho and E. E. Swartzlander, "Adder designs and analyses for quantum-dot cellular automata", Nanotechnology, IEEE Transactions on, vol. 6, no. 3, **(2007)**, pp. 374-383.
[17]. N. Keivan, F. Razieh, S. Samira and R. A. Mostafa, "A new quantum-dot cellular automata full-adder", Microelectronics Journal, vol. 41, no.12, **(2010)**, pp. 820-826.
[18]. J. D. Wood and D. Tougaw, "Matrix multiplication using quantum-dot cellular automata to implement conventional microelectronics", Nanotechnology, IEEE Transactions on, vol. 10, no. 5, **(2011)**, pp. 1036-1042.
[19]. H. Cho and E. E. Swartzlander, "Adder and multiplier design in quantum-dot cellular automata," Computers, IEEE Transactions on, vol. 58, no. 6, **(2009)**, pp. 721-727.
[20]. A. Roohi, H. Khademolhosseini, S. Sayedsalehi and K. Navi, "A novel architecture for quantum-dot cellular automata multiplexer", International Journal of Computer Science Issues (IJCSI), vol. 8, no. 6, **(2011)**, pp. 55-60.
[21]. J. Huang, M. Momenzadeh and F. Lombardi, "Design of sequential circuits by quantum-dot cellular automata", Microelectronics Journal, vol. 38, no. 4, **(2007)**, pp. 525-537.
[22]. K. Kyosun, W. Kaijie and R. Karri, "Quantum-dot cellular automata design guideline", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, vol. 89, no. 6, **(2006)**, pp. 1607-1614.
[23]. V. Vankamamidi, M. Ottavi and F. Lombardi, "A serial memory by quantum-dot cellular automata (QCA)", Computers, IEEE Transactions on, vol. 57, No. 5, **(2008)**, pp. 606-618.
[24]. P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata", Journal of Applied physics, vol. 75, no. 3, **(1994)**, pp. 1818-1825.
[25]. K. Walus and G. Jullien, "Design tools for an emerging SOC technology: Quantum-dot cellular automata", Proceedings of the IEEE, vol. 94, no. 6, **(2006)**, pp. 1225-1244.
[26]. M. Mustafa and M. Beigh, "Design and implementation of quantum cellular automata based novel parity generator and checker circuits with minimum complexity and cell count", Indian Journal of Pure and Applied Physics, vol. 51, no. 1, **(2013)**, pp. 60-66.
[27]. M. R. Beigh, M. Mustafa and F. Ahmad, "Performance evaluation of efficient XOR structures in quantum-dot cellular automata (QCA)", Circuits & Systems, vol. 4, no. 2, **(2013)**, pp. 147-156.
[28]. S.-H. Shin, J.-C. Jeon and K.-Y. Yoo, "Design of Wire-Crossing Technique Based on Difference of Cell State in Quantum-Dot Cellular Automata", International Journal of Control and Automation, vol.7, no. 4, **(2014)**, pp. 153-164.
[29]. K. Walus, T. J. Dysart, G. A. Jullien and R. A. Budiman, "Qcadesigner: A rapid design and simulation tool for quantum-dot cellular automata," Nanotechnology, IEEE Transactions on, vol. 3, no. 1, **(2004)**, pp. 26-31.

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