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Extendable Quantum-Dot Cellular Automata Decoding Architecture Using 5-Input Majority Gate

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Abstract

This paper presents a decoder with enable input. This decoder is developed using quantum-dot cellular automata (QCA). QCA opens a completely radical way of microelectronics development and a potential replacement of CMOS based electronics. It ensures highly compact circuits, faster processing speeds, low power consumption. The use of clock in QCA provides power gain which is an important feature and this feature is not available in CMOS electronics. The proposed decoding architecture is designed using 5-input majority gate to keep a regularity so easily extendable for 3:8 or 4:16 decoders and also easy to connect with other circuits.

Keywords: *Quantum-dot cellular automata, decoder, majority gate*

1. Introduction

Since Gordon Moore said that number of transistors on integrated circuits doubles approximately every two years, the reduction of feature sizes and the increase of processing power have been successfully achieved by very large scale integration (VLSI) technology [1, 2]. The microprocessor is one of typical examples, based on VLSI technology, and it is being actively studied in order to increase the integration, performance, efficiency and to minimize the feature sizes. Although many techniques were proposed in order to increase the integration, the development of VLSI technology has reached its peak due to the fundamental physical limits of CMOS technology.

Continuous scaling down of CMOS technology is reaching its limiting levels. Further reduction in size has resulted in a number of problems for microelectronics although computing powers have increased at the same time. Some of the problems include interconnection of the circuit at such small scales and also high current leakage or inefficient power dissipation. All these problems require that an alternative technology be found that should replace CMOS technology. One such technology is quantum-dot cellular automata (QCA) [3-5].In order to overcome these, we need a new technology in nano-scale. One of solutions is a quantum-dot cellular automata (QCA). It not only gives a solution at nano-scale, but also offers new techniques of computation and data transmission [6-14].

A QCA is the computing with cellular automata composed of arrays of quantum-dot devices, and basic concepts of it were introduced by Tougaw and Lent in 1993 [5][15]. The unique feature is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits [10]. In order to transmit data, QCA uses a clocking technique. It is operated by a tunneling barrier. According to the raising or lowering

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of the tunneling barrier, the clocking technique consists of four stages: locking, locked, relaxing and relaxed.

QCA offers a number of advantages over CMOS technology. Some of the advantages include faster switching speeds, high density circuits and far less power dissipation. The assumption is that all these advantages will result in the development of highly powerful and efficient computers [16, 17].

A decoder is one of the most important parts that are used in computer circuits like in random access memories (RAM). In RAM it is used to select an output when enable is high. Several decoders have been proposed in QCA. In [18] they proposed a 2:4 decoder with enable. This decoder is similar to decoders that are used in typical CMOS memory. In this design they implemented row and column decoders that have row and column enable lines. This approach results in large unused area.

In [19] they also proposed a 2:4 decoder with enable using 3-input and 5-input majority gates. By using 3-input majority gates, they used 8 AND gates for the circuit (4 AND gates were used for enable/disable). By using the 5-input majority gate, they reduced the complexity of the 2:4 decoder.

This paper proposes a 2:4 decoder with enable line implemented using QCA, this scheme reduces the number of cells in the circuit than the circuit we compared with in [20]. It also reduced the number of clock phases in the circuit. In this paper we have also proposed a majority gate that we have used to implement an AND and OR gate.

There is also a need for circuits to be designed with regular clock zones so that they can easily be implemented but only a few circuits that consider regular clock zones have been designed [21]. We used the gate that we have proposed to implement a decoder that has uniform clocking zones along the column. The gate was rigorously tested to make sure that it is functioning properly. We used this gate to design a 2:4 decoder that had uniform clock zones. We hope this will make implementation of the 2:4 decoder circuit and other future circuits realizable.

The paper is organized as follows; section 2 gives the literature review. Section 3 discusses the proposed 2-input decoder with enable signal, section 4 gives the simulation and analysis of the results and finally section 5 gives the conclusions.

2. Related Works

In this section we look at the QCA basics and a brief description of decoders.

2.1. Quantum-Dot Cellular Automata Basics

QCA cells are made of nano scale structures and are able to encode information in electric charge configuration. A single QCA cell is made up of four quantum-dots that are diagonal to each other. The cells can tunnel within the cell but not outside the cell. Figure 1 shows the QCA cell. Moreover, the cells have two free electrons. Due to Coulombic interaction the two electrons tend to occupy the two opposite corners of the cell which results in polarization p+1 or polarization p-1 which are logical bits 1 and 0 respectively [21, 22].

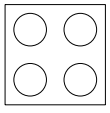


Figure 1. QCA Cell Having Four Quantum Dots Located on the Four Corners of the Cell

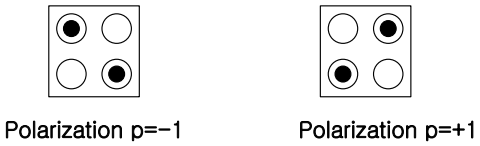


Figure 2. QCA Cells Having Two Ground State Electrons and their Polarization, Where Polarization P=-1 Represents Logical "0" and Polarization P=+1 Is Logical "1"

QCA structures are formed by placing cells together. A wire can be formed by placing cells one after another as in Figure 3(a). In the wire, information propagation takes the form of the input signal. If the input is a 0, then the information transferred from input to output will be zero or if the input is a one, then one will be transferred to the output.

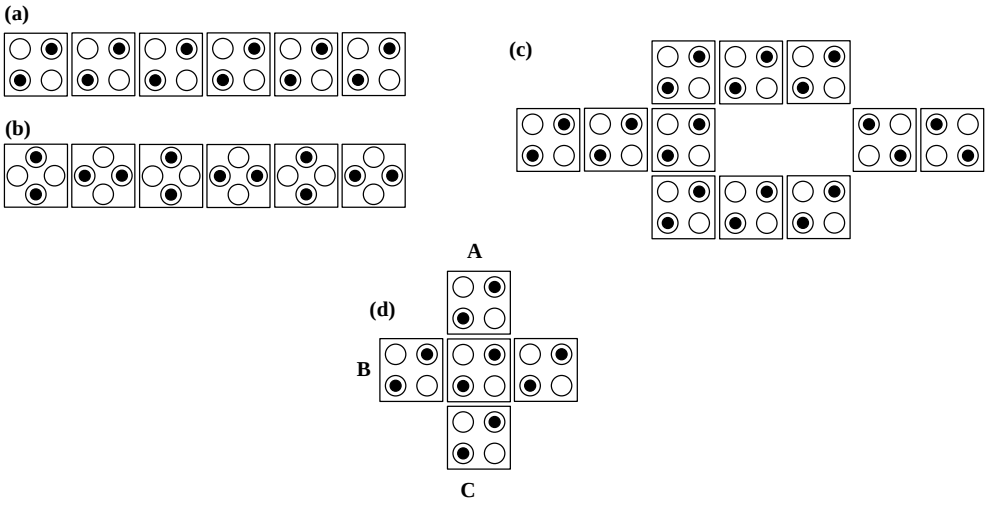


Figure 3. QCA Basic Structures. (A) QCA Wire, (B) Inverter Chain, (C) Inverter Gate, (D) Majority Gate

The other structure that is important is the inverter chain, shown in Figure 3(b). In the inverter chain, the information alternates between a 0 and 1 as it is being propagated in the chain and it depends on the initial input signal. The other QCA logic gate is the inverter gate (although there are several versions of inverters which we will not be shown in the paper) shown in Figure 3(c). The inverter changes an input of 0 to 1 and 1 to 0. The other important logical gate is the 3-input majority gate shown in Figure 3(d). Mathematically, it can be represented by equation (1). Using this gate, we can form an AND gate or an OR gate. To form an AND gate, equation (2), one of the input is fixed to logical 0 and to form an OR gate, one of the input is fixed to 1, equation (3) [23, 24].

$$M(A, B, C) = AB + BC + AC \tag{1}$$

$$M(A, B, 0) = AB \tag{2}$$

$$M(A, B, 1) = A + B \tag{3}$$

In QCA, the cells belong to one of the four clock zones and each clock zone has a different clock signal. The clock labeling convention is from 0 to 3. Figure 4 shows the four clock zones [25]. The four clock phases, shown in Figure 5, are switch, hold, release and relax are utilized in the four clock signals. In the switch phase, the cells begin to

compute the value; the cells are unpolarized and have low potential barriers which begin to be raised. In the hold phase, the value is held and the barriers are held high. In the release phase, the barriers are lowered and lastly, in the relax phase, the barriers remain lowered where the cells remain unpolarized. The phases allow for a reliable signal transmission and also functional gain which is of paramount importance in computational systems [25-27]. The clock phases can also summarized as Figure 6.

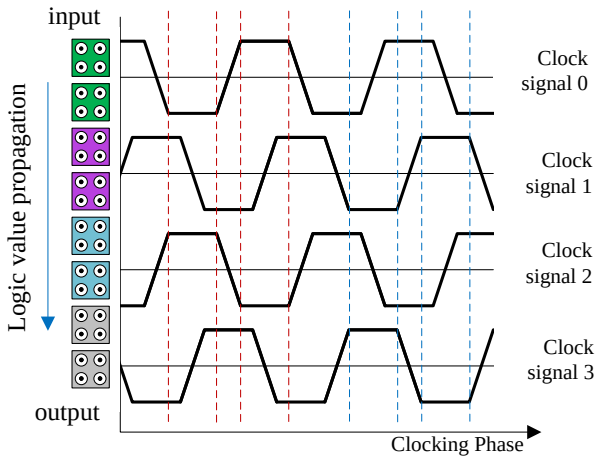


Figure 4. Four Clock Zones Showing the QCA Clock Signal Propagation

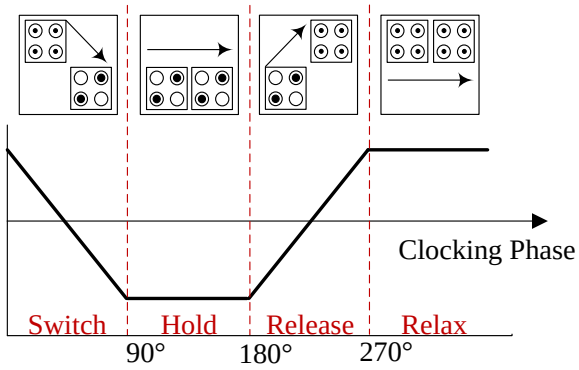


Figure 5. QCA Clock Phases of Switch, Hold, Release And Relax

In 2005, Graunke *et al.*, [28] proposed a new wire-crossing technique (this is called a crossbar network) based on parallel to serial conversion and time-dependent latching in order to improve the disadvantages of the previous two techniques. The characteristic of this technique is that two wires are crossed in coplanar without the rotation or translation of cells, and structure of the cell arrangement is regular because of using the parallel to serial conversion method. However, there exists a number of clocks because of time-dependent latching zones. If the clocking is going to be continuously maintained by time-dependent latching, the unexpected results can be occurred such as a difficulty of switching time, an increasing of cell temperature, and a noise of kink energy. Also, this technique requires additional devices such as a parallel-to-serial converter, a shift register and a time-dependent latching device.

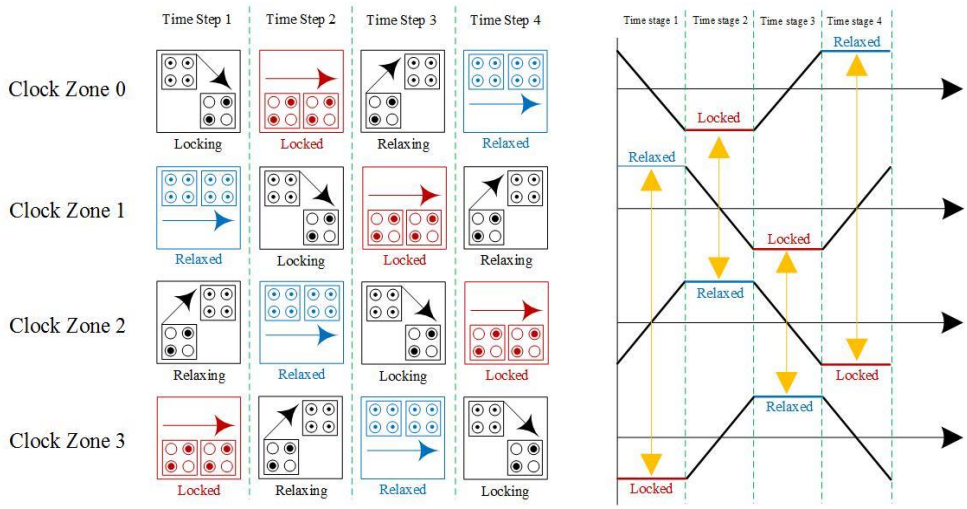
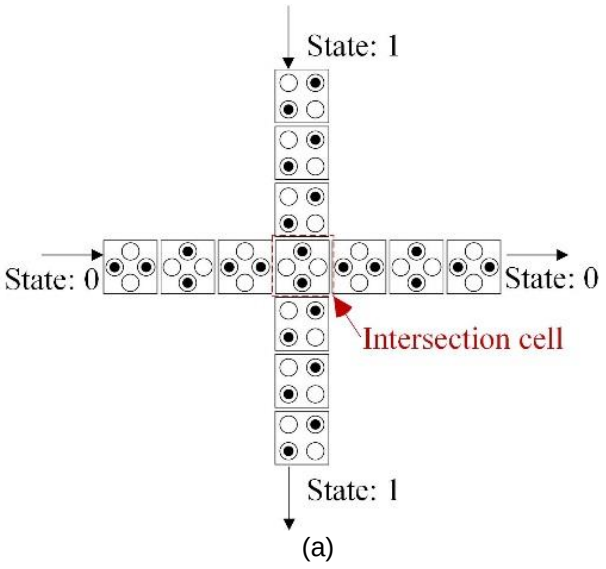
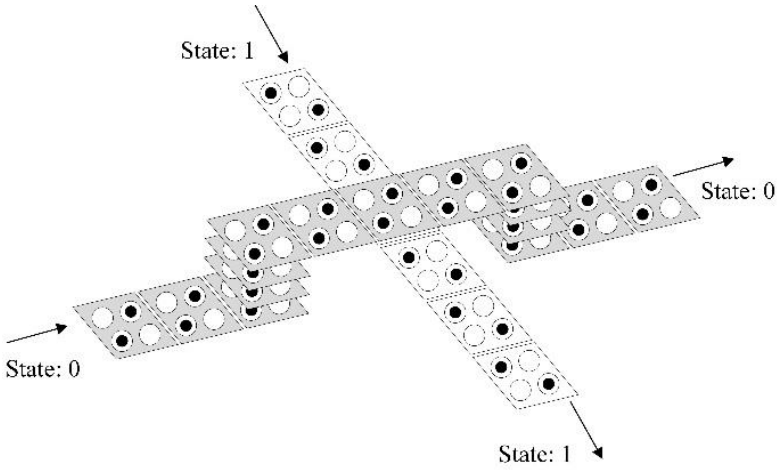


Figure 6. The Geometric Example of Relation of Stages for Four Clock Zones

In order to transmit data, QCA uses a clocking technique based on the raising or lowering of tunneling barriers in a cell. The tunneling barriers are typically modulated through four separate stages as shown in Figure 6: the locking stage that the tunneling barriers are raising, the locked stage that tunneling barriers are fully raised, relaxing stage that tunneling barriers are lowering, and the relaxed stage that tunneling barriers are completely lowered, allowing free electron movement within a cell. A clock cycle consists of four distinct stages, and a clock zone has an arbitrary clock signal. Data transmissions through two clock zones are performed as shown in Figure 6. When stages of clock zone 0 and clock zone 1 are locked and locking at the same time, there exists the data transmission from clock zone 0 to clock zone 1, respectively.





(b)

Figure 7. Typical QCA Wire-Crossing Techniques: (A) Geometry Example of Coplanar-Based QCA Wire-Crossing and (B) Geometry Example of Multilayer-Based QCA Wire-Crossing

There exist three representative wire-crossing techniques: a coplanar-based, a multilayer-based and a crossbar network. Tougaw and Lent [23] proposed a coplanar-based wire-crossing technique as shown in Figure 7(a). In this example, vertical and horizontal wires are transmitting the value '1' and '0', respectively.

In order to implement this wire-crossing, cells of horizontal wire are rotated by 45′. When the number of cells after an intersection in the vertical wire is sufficient (that is, the number of cells is greater than or equal to 3), a transmitting value is not affected by the other wire. The number of cells in the horizontal wire should be composed of odd because of the characteristic of rotated cells. 45′ rotated cells induce the additional space between cells. It significantly decreases the energy separation between the ground state and the first excited state, which degrades the performance of such a device in terms of maximum operating temperature, resistance to entropy, and minimum switching time [12].

The multilayer-based wire-crossing technique uses a crossover bridge method. This technique is similar to coplanar-based technique in the perspective of the floor plan because it looks like appearance of two wires crossing. In fact, it consists of the stereoscopic structure as shown in Figure 7(b). In this example, the horizontal chain is using a crossover bridge. The structure of this technique can be more miniaturized and generalized than coplanar-based technique because it does not need to rotate cells. Although this technique has some advantages, there exists the noise problem between intersection cells in crossover area [21].

2.2. Decoder

Decoders play an important role in computer architectures. They are used in different part of the computer like random access memory and they also form part of the Look up Table (LUT) [29]. The decoder selects one out of several outputs lines when it has been activated for output. For the 3-input and 8-output decoder, one of the inputs is used to select the output [30].

In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different *e.g.*, n-to-2n , binary-coded decimal decoders. Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding. The example decoder circuit would be an AND gate because the output of an AND gate is 'High' (1) only when all its inputs are 'High'. Such output is called as

'active High output'. If instead of AND gate, the NAND gate is connected the output will be 'Low' (0) only when all its inputs are 'High'. Such output is called as 'active low output'.

A slightly more complex decoder would be the n-to-2n type binary decoders. These types of decoders are combinational circuits that convert binary information from 'n' coded inputs to a maximum of 2n unique outputs. In case the 'n' bit coded information has unused bit combinations, the decoder may have less than 2n outputs. 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder are other examples. The input to a decoder is parallel binary number and it is used to detect the presence of a particular binary number at the input. The output indicates presence or absence of specific number at the decoder input [31].

Let us suppose that a logic network has 2 inputs A and B. They will give rise to 4 states. The truth table for this decoder is shown below.

Several studies have been done on decoders in QCA. In [32], they proposed a 2 to 4 decoder using a 5-input majority gate. In this method, they reduced the number of gates to only four. This resulted in reduced delay and complexity of the decoder.

In [33], they proposed a 2 to 4 decoder. This decoder uses 4 majority gates in its structure and also uses 7 clock phases. This was extended to build a 3 to 8 decoder by using two 2 to 4 decoders. The 3 to 8 decoder uses a total of 8 majority gates and 11 clock phases.

Table 1. The Truth Table of the Decoder with Enable (EN) Line

Input			Output			
A	B	EN	Y1	Y1	Y3	Y4
0	0	0	0	0	0	0
0	1	0	0	0	0	0
1	0	0	0	0	0	0
1	1	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

3. Proposed Decoder

We propose a QCA decoder shown in Figure 8. This decoder is made up of four 5-input majority gates. The gates were implemented as AND gates. As [32] pointed out, using traditional design methods will require a total of 8 gates. This will increase the complexity of the design as well as increase the delay time. The use of the four 5-input majority gate will result in the reduction in complexity of the circuit [34].

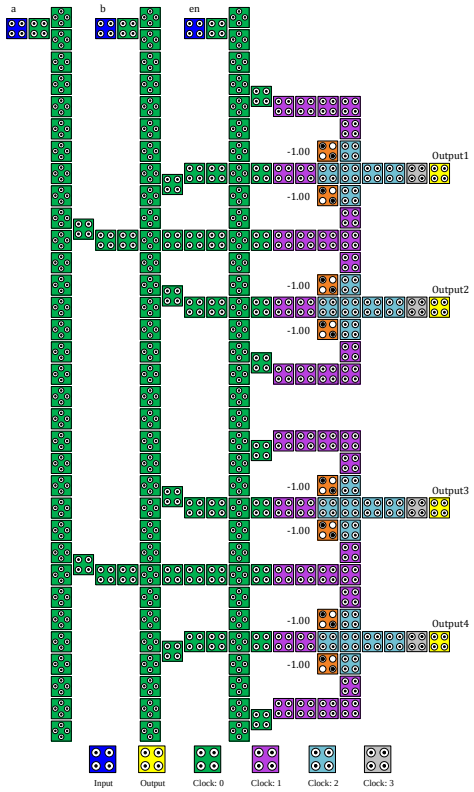


Figure 8. Proposed Structure of the QCA Decoder

This circuit was designed with the aim of reducing the delay time and thereby increasing the computational speeds. Therefore in this design we used only four clocks *i.e.*, clock 1 to clock 3 as depicted by Figure 6. In this circuit, we only used one layer (not multilayer) hence the use of the inverter chains with rotated cells to help in the signal to propagate properly.

4. Simulation and Analysis

The circuits in this paper were designed and simulated using QCADesigner [35]. The QCADesigner is to perform a design and simulation for QCA, and it is the product of an ongoing research effort by the Walus Group at University of British Columbia [36]. The objective of this tool is to create an easy to use simulation and layout tool available freely to the research community via the Internet. One of the most important design specifications is that other developers should be able to easily integrate their own utilities into this tool. It is accomplished by providing a standardized method of representing information within the software. As well, simulation engines can easily be integrated into QCADesigner using a standardized calling scheme and data types. It is written in C/C++ and employs a wide range of open source software such as GNU image manipulation program toolkit graphics library, and is maintained under the GNU's not Unix public license (GPL) for open source software [37].

In QCADesigner the cells are assumed to be 18nm in height and width. The cells are also placed in a grid with a center to center distance of 20nm [38]. The simulation resulted are given in Figure 7. The results show proper operation of the decoder and the results are produced after one clock cycle (four clock phases).

The comparison was done in terms of the number of cells and clock phases. As it can be seen from the simulation results in Figure 7, our circuit's output is produced after only four clock phases (the delay is only one clock cycle) where as the one proposed in [32]

produces its output after 7 clock phases. This makes our design faster. In terms of the number of cells used our design used only 219 cells where as the one proposed in [32] used a total of 367 cells. This makes our proposed scheme smaller and dense thereby reducing wasted area. The reduction in the number of cells used is approximately 40.33%.

In our design and the one proposed in [33], both of these designs used four 5-input majority gates. From Figure 9, the results are produced when 'en' is active i.e. the value of 'en' is 1 as highlighted in the figure. When 'en' is inactive (i.e. the value of 'en' is 0) the results are not produced. All the improvements make our proposed circuit a good option to connect to other larger circuits like the construction of random access memory [33]. The comparisons are summarized is Table 2.

Table 2. Comparison between the Proposed Circuit and [33]

Comparison parameter	Proposed Circuit	Proposed in [33]
Clock phases	4	7
Number of cells	219	367
Number of gates	4	4

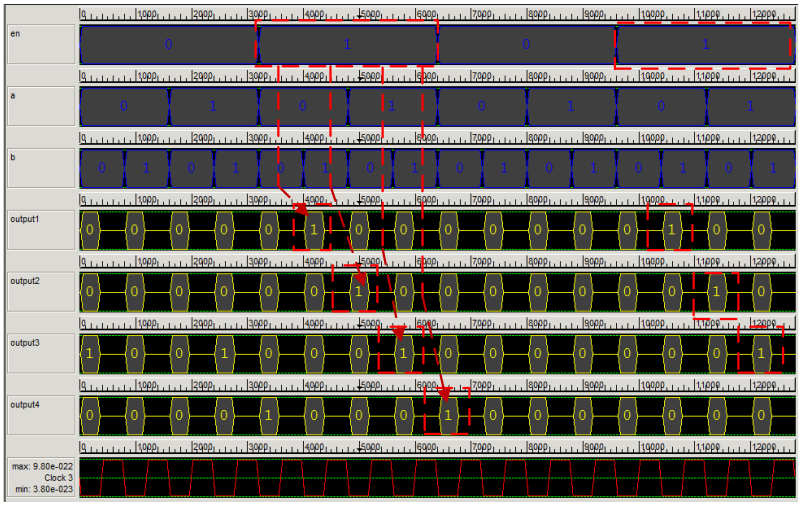


Figure 9. Simulation Results of the Proposed Decoder

5. Conclusions

In this paper, we have proposed a 2:4 decoder with enable line that has a number of advantages. The first advantage is the reduced delay time. Our circuit delay time is only four clock phases i.e. only one clock cycle. This makes our circuit ideal to connect to other larger circuits or circuits where reduction in time will result in faster computation speeds. This will help in reducing the total delay time of those other circuits that will use our circuit as part of it. we have also shown that, our proposed circuit has less number of cells as opposed to the circuit we compared with. This reduces the area that the circuit covers and this helps to reduce the overall area that the circuit covers when connected to other larger circuits. Our circuit also is regular and extendable, and easily connect to other circuits so that the circuit can be easily extended for 3:8 or 4:16 decoders.

Acknowledgments

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