

## Low-Power CMOS Programmable Gain Amplifier with a DC-offset Cancellation for a Direct Conversion Receiver

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### Abstract

*This paper presents low-power Programmable Gain Amplifier (PGA) with a DC-offset cancellation for a direct conversion receiver (DCR) to reduce chip area, cost and power. In the receiver stage, the direct conversion architecture has simplified scheme as compared to the conventional super-heterodyne architecture because IF stage could be omitted in the direct conversion architecture, and the system can be a single chip. The PGA controls 8-level gains from 4dB to 60dB using the CMOS switches and passive resistors in parallel, and DC-offset circuit is based on a Miller effect technique. It is fabricated using Magnachip/SK Hynix 0.18- $\mu\text{m}$  CMOS 1poly-6metal process. The proposed system showed excellent gain error of less than 0.24dB, very small die area of 0.015mm<sup>2</sup> and low power consumption of 1.137mW.*

**Keywords:** Programmable Gain Amplifier (PGA), 0.18- $\mu\text{m}$ , CMOS switches, DC-offset, direct conversion

### 1. Introduction

Recently, wireless communication field has rapidly developed, and the Radio Frequency (RF) components market is continuously increasing. Specially, CMOS RF integrated circuit research is actively being conducted for small chip area, low cost and low power consumption. In order to achieve these goals, the system can be a single chip using Direct Conversion Receiver (DCR) technique. The DCR technique as compared to the conventional super-heterodyne receiver technique has no intermediate frequency (IF), the removed image problem, and bulky external filter. Thanks to these advantages, it is possible to make small chip size and low power consumption [1].

Despite these advantages, the DC-offset phenomenon can degrade the system performance. The DC-offset occurred in the analog baseband is amplified as a gain of the variable amplifier. Since this problem is effected on the operation area of the analog-to-digital converter (ADC), the system performance is degraded and signal demodulation may not be generated. The PGA has been used in a variety of fields such as disk drive, hearing aids, optical receiver and wireless communication system, etc.

A PGA is essential to maximize the dynamic output range of the system, and it is possible to adjust the gain. There are two gain control techniques of analog and digital using a type of programmable gain signal. An analog gain control technique generally utilizes a variable transconductance and resistor, and a digital technique uses CMOS switches. Recently, the PGA is often controlled and embodied as a feedback loop by Digital Signal Processor (DSP).

In this paper, a PGA with DC-offset cancellation circuit (DCOC) for wireless local area network (LAN) DCR is proposed. The PGA adjusts the programmable gain using digital control technique. The suitable PGA still remains to be the major issues to make affordable commercial systems [2-5]. To solve DC-offset problem, this paper proposes continuous time feedback calibration loop using Miller effect to reduce the DC-offset level without large capacitance [4]. We also present a low power CMOS PGA with a DC-offset cancellation for a wireless LAN DCR. This circuit controls gains of 8 levels with 4dB ~ 60dB by steps of 8dB.

## 2. PGA with DC-offset Cancellation Circuit

### 2.1. PGA Circuit Design

The proposed PGA is based on Gm-boosting amplifier. Figure 1 shows a Gm-boosting differential amplifier with a negative feedback technique. The output of  $M_1$  forms the negative feedback loop into the gate terminal of  $M_2$ . If the drain voltage of  $M_1$  is increased due to the external impact, the gate voltage of  $M_2$  also increases so that the drain voltage of  $M_2$  is decreased. This means the increase of the overdrive voltage of  $M_1$ . Eventually, the circuit becomes less sensitive to external influences because the output voltage of  $M_1$  is decreased due to the negative feedback effect.

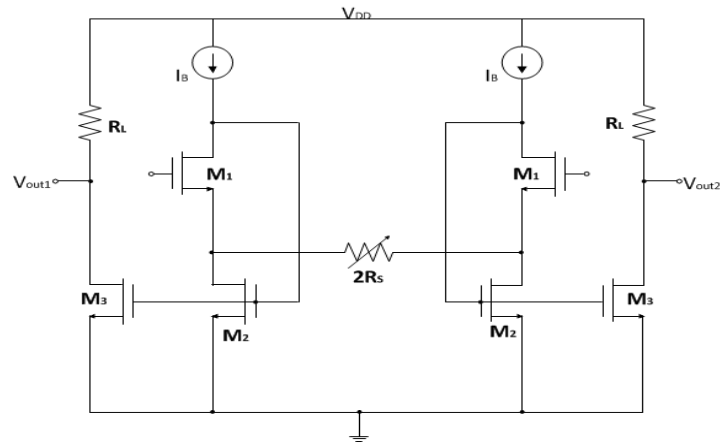


Figure 1. Gm-boosting Amplifier

### 2.2. DC-offset Cancellation Circuit Design

In the DCR architecture, DC-offset phenomenon can be divided into two reasons. First, as shown in Figure 2, when DCR Local Oscillator (LO) leakage signal is applied to the RF input stage of the mixer via the unintended path, undesirable DC component occurs due to the self-mixing. In addition, the DC-offset occurs when the LO leakage component is applied to the input stage of the Low Noise Amplifier (LNA). In this case, the leakage signal is amplified as a strong signal, and it provides self-mixing. DC offset component effects on proceeding baseband block.

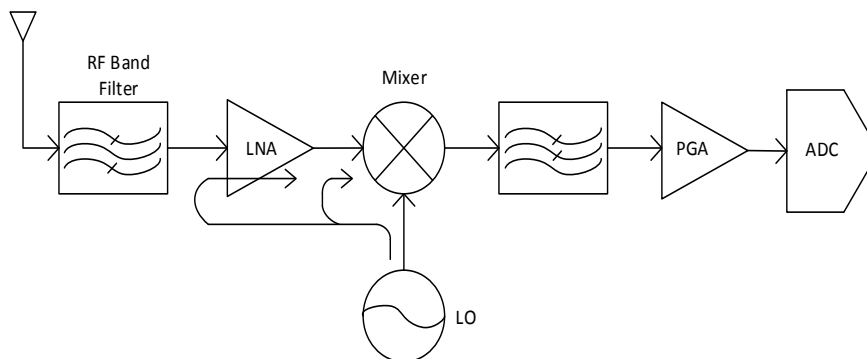
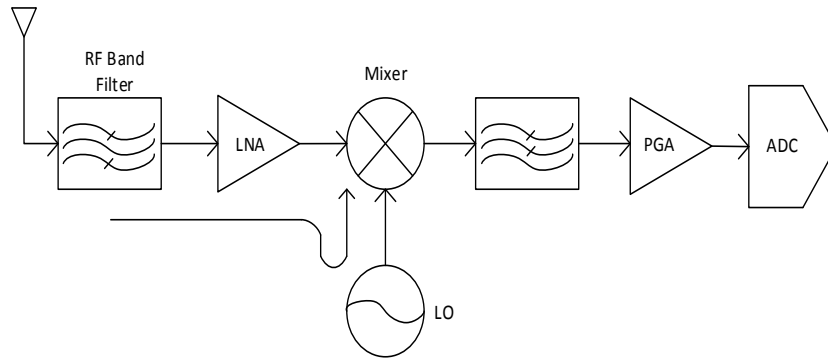


Figure 2. DC-offset by LO Leakage

Second, the DC-offset component comes from a strong interference signal in the band. It is amplified in the LNA, and then it is applied to the LO input stage by self-mixing as shown in Figure 3.

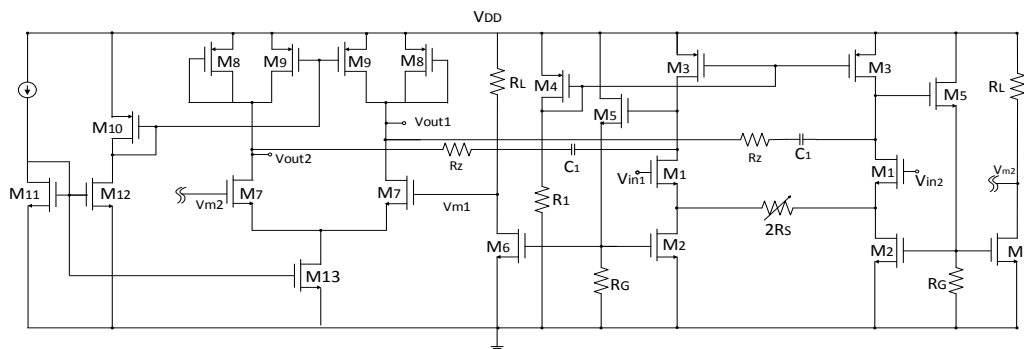


**Figure 3. DC-offset by Strong Interference Signal**

### 2.3. Proposed PGA with DC-offset Cancellation Circuit

The proposed PGA circuit is shown in Figure 4. It has fully symmetrical structure at differential mode, and sources of transistors,  $M_1$ - $M_2$  have an opposite voltage when two inputs with opposite phases are inserted into the circuit. The amplifier gain can be selected by using a ratio of degeneration resistor or a load resistor. Both sides of the symmetrical structure have the same value of direct current at the source node, and then the gain is adjustable by changing the degeneration resistor. To get higher gain, the value of the total degeneration resistor must be lower, thus it leads to the increment of gain errors. Therefore, to obtain a more accurate and higher gain, the proposed PGA includes Gm-boosting source-degenerated differential pair and an additional amplifier stage [6].

The DC-offset cancellation circuit (DCOC) is based on Miller effect with continuous time feedback as shown Figure 4. It is realized in capacitor and resistor of the large value using the Miller effect. Comparing the difference between a continuous time feedback method and AC-coupling method using Miller effect, continuous time feedback method has advantage for realizing the low-pass filter with a low cut-off frequency. However, a larger resistor or capacitor should be realized by off-chip in order to minimize the chip size. The external components need the additional pin and increase the whole system dimensions. To solve the problem, this paper uses the Miller capacitors based on the continuous time feedback technique. The Miller effect is used to realize a large value capacitor. Using this technique, it is possible to reduce chip size and power consumption [7].



**Figure 4. Proposed PGA with DC-offset Cancellation**

Figure 5 shows the simplified block diagram of the Figure 4. Considering damage of the desired signal due to the DC-offset, the system requires a lower cut-off frequency ( $f_c$ ), and fundamental frequency ( $f_0$ ) must be small enough. The equation of cut-off frequency is expressed as in Equation (1)

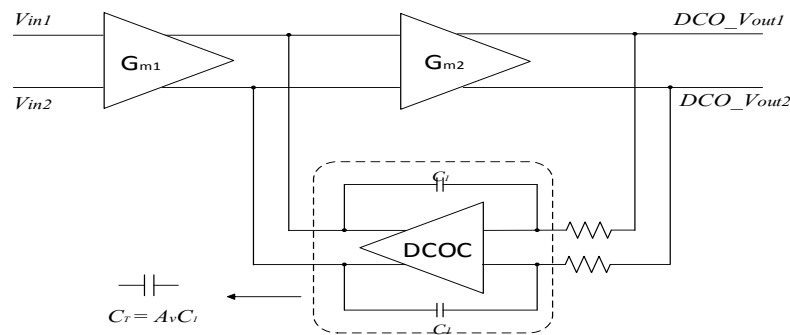
$$f_c = \frac{1}{2\pi RC} \quad (1)$$

The resistance,  $R$  and capacitance,  $C$  must be increased in order to obtain a lower  $f_c$ , but a large  $RC$  requires a large area. To reduce the  $RC$  area, this paper utilizes the Miller capacitor. The Miller effect can increase the value of total capacitance  $C_T$ , since the capacitance for the Miller effect is described in Equation (2).

$$C_T = (1 + A_v)C_I \approx A_v C_I \quad (2)$$

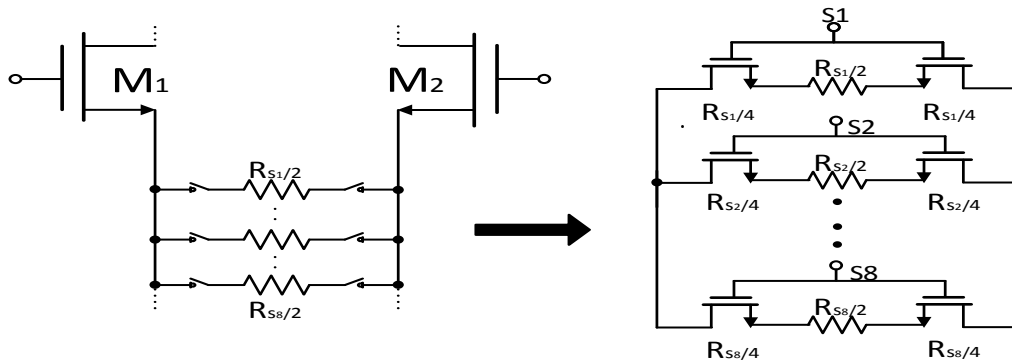
where  $A_v$  is a gain of PGA, and  $A_v$  is bigger than 1.

The DC-offset voltage of the PGA at the low frequency is detected and stored in an equivalent capacitance,  $A_v C_I$ . The capacitor value of the circuit is calculated using the Equation (2). If a capacitor of 1pF and a gain of 1,000 are used in the circuit, we can obtain large capacitor value of 1,000pF using the Miller effect.



**Figure 5. Block Diagram of the Proposed Circuit**

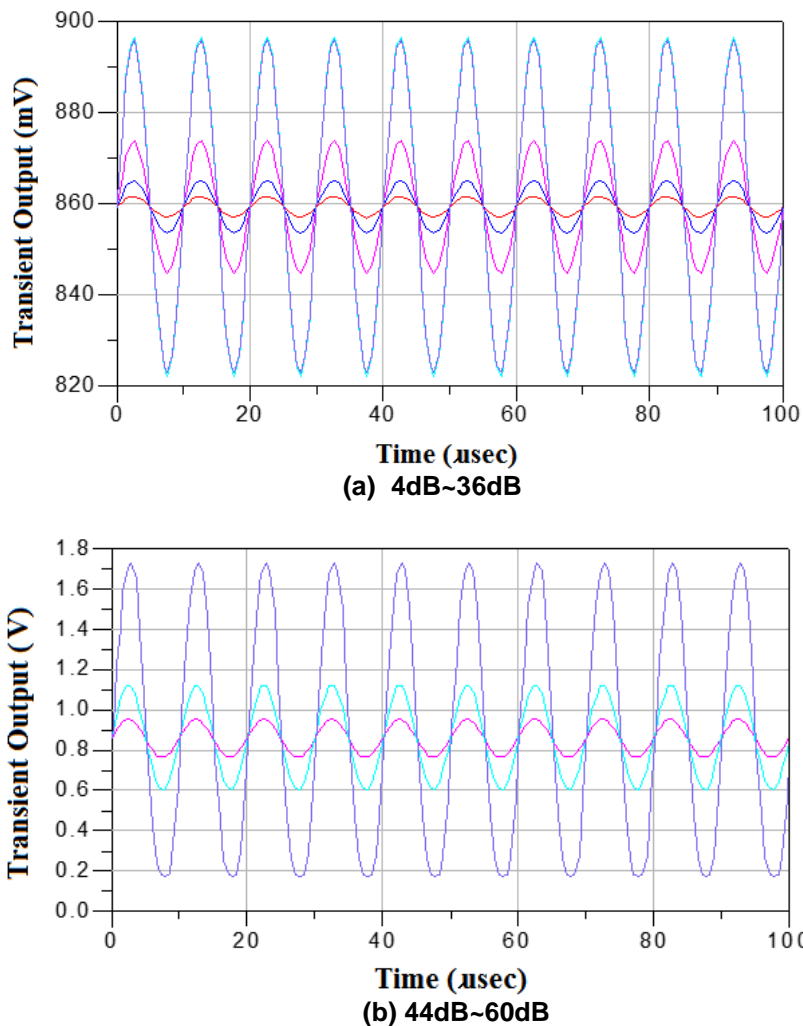
Fig. 6 shows gain adjustment stage of PGA using degeneration resistor ( $2R_s$ ) consisting of resistors and CMOS switches. The gain adjustment stage has a disadvantage of large chip area due to the large size of passive element. If it is designed to minimum on-resistor effect, the linearity is improved, and vice versa. Therefore, the gain adjustment stage of proposed PGA is designed using half of the size of the passive elements and on-resistor of the switch for the degeneration resistor. The gain of the proposed PGA is determined by the value of degeneration resistor [8]. To increase linearity of switch and decrease chip size, we used CMOS switches and resistors. It consists of 16 CMOS switches and 8 resistors to provide various gains such as 4dB, 12dB, 20dB, 28dB, 36dB, 44dB, 52dB and 60dB.



**Figure 6. Gain Adjustment Stage Using Switches and Resistors**

### 3. Results

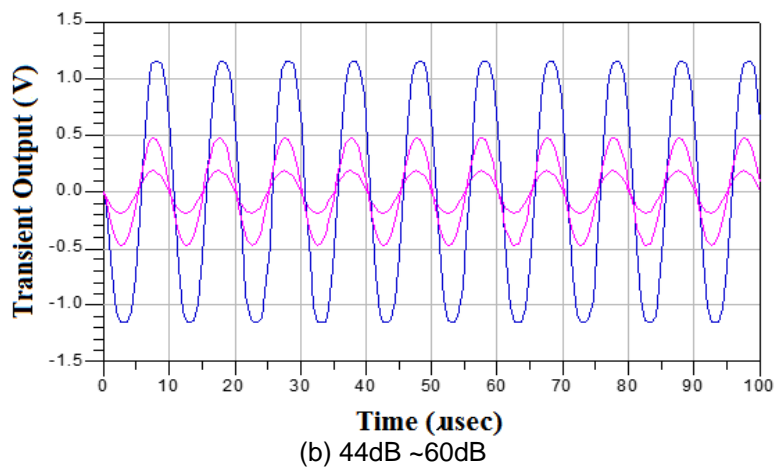
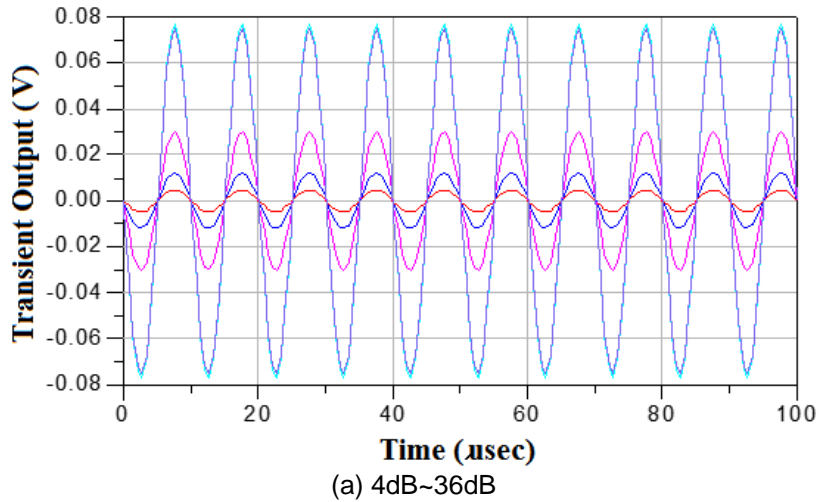
Figure 7 shows transient results for the proposed PGA without DCOC. It is designed by providing various gains such as 4dB, 12dB, 20dB, 28dB, 36dB, 44dB, 52dB and 60dB, etc. The bias voltage of 0.8V is injected with the DC-offset voltage of  $0.8 \pm 0.1V$ . The results showed the large output DC-offset level of approximately 860mV without DCOC.



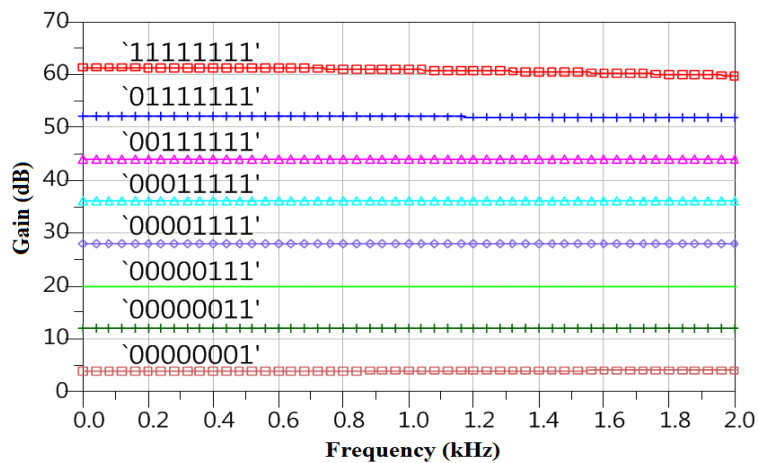
**Figure 7. Transient Results without DCOC**

Figure 8 shows transient results for the proposed PGA with DCOC. It is also designed by providing various gains of 4dB~60dB by 8 steps of 8dB. The bias voltage has 0.8V with the DC-offset of  $0.8 \pm 0.1V$ . The results showed very small time variations of less than  $\pm 2\%$  and the output DC-offset level of only  $39 \mu V$  for average values from 10 times experiments. These results verify that proposed PGA with DCOC shown in Figure 4 has excellent DC-offset cancellation effect.

Figure 9 shows AC results of frequency domain with various gains for the proposed PGA. It is simulated from 0Hz to 100kHz in 5kHz scale by changing the output signal. The gain is controlled by the open status (logical 'low') and the closed status (logical 'high') of the switches ( $S_1S_2S_3S_4S_5S_6S_7S_8$ ). When the all switches are closed, the gain is 60dB, and only one switch is closed for the gain of 4dB. As shown in this Figure, the PGA showed stable gains of 4dB~60dB by 8 steps of 8dB for the switching operation.



**Figure 8. Transient Results with DCOC**



**Figure 9. AC Results**

Figure 10 and Table 1 show results of differential-mode gain ( $A_{dm}$ ), common-mode gain ( $A_{cm}$ ) and common-mode-rejection ratio (CMRR) for the proposed PGA. In differential amplifiers with perfect symmetry, each component on the side of one output corresponds to an identical component on the side of the other output. With such perfectly balanced amplifiers, when  $v_{in1} = -v_{in2}$ ,  $v_{out1} = -v_{out2}$ . Similarly, pure common-mode inputs (for which

differential-mode input,  $v_{id} = 0$ ) produce pure common-mode outputs in perfectly balanced differential amplifiers. Therefore, the ratio  $A_{dm}/A_{cm}$  is one figure of merit for a differential amplifier, giving the ratio of the desired differential-mode gain to the undesired common-mode gain. CMRR is defined by the magnitude of this ratio as the common-mode-rejection ratio. As shown in Figure 10 and Table 1, the PGA showed excellent CMRR of 80.80dB for 4dB gain and of 131.71dB for 60dB gain, respectively. It shows excellent frequency characteristic when the CMRR rejection ratio is bigger. The proposed PGA also showed very small gain error of less than 0.24dB.

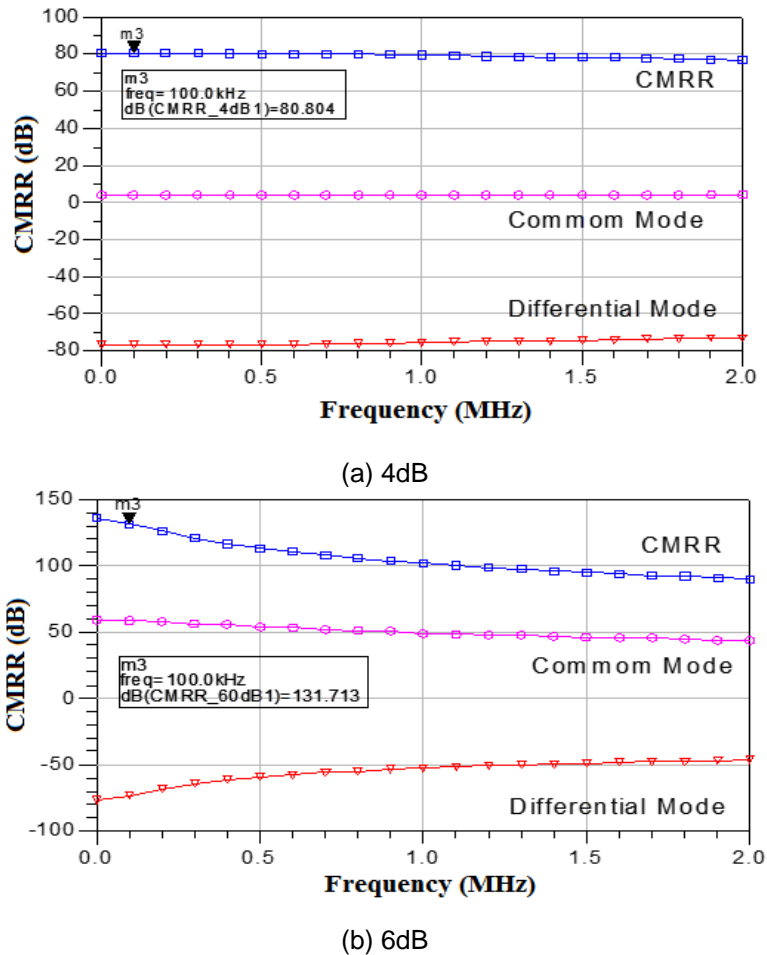


Figure 10. Common Mode Rejection Ratio

Table 1. Results of  $A_{dm}$ ,  $A_{cm}$  and CMRR for the Proposed PGA

	$A_{dm}$ (dB)	$A_{cm}$ (dB)	CMRR (dB)
6dB	4.06	-76.74	80.80
12dB	12.11	-76.73	88.84
20dB	20.22	-76.72	96.94
28dB	28.11	-76.71	104.82
36dB	35.99	-76.10	112.09
44dB	44.24	-75.93	120.17
52dB	52.17	-75.76	127.93
60dB	59.81	-75.51	135.32

Table 2 shows comparison results for recently reported PGA. The proposed PGA showed very small gain error of less than 0.24dB, and very low power consumption of 1.137mW, and very small chip area of 0.015mm<sup>2</sup> as compared to conventional results [9-12].

**Table 2. Comparison Results for Recently Reported PGA**

	This work	[9]	[10]	[11]	[12]
Process (μm)	0.18	0.18	0.18	0.18	0.13
Gain range (dB)	4/60	0/70	-15/60	-22/32	0/60
Gain error (dB)	< 0.24	< 0.7	< 0.3	< 0.5	< 0.3
Power dissipation (mW)	1.137	4	11.85	2.16	9
Bandwidth (MHz)	2	15	140	65	90
Chip size (mm <sup>2</sup> )	0.015	1.2	0.06	0.385	-

#### 4. Conclusions

In this paper, we proposed a low-power Programmable Gain Amplifier (PGA) with DC-offset cancellation circuit for Direct Conversion Receiver (DCR). The PGA is realized for wireless local area network (LAN) DCR. The PGA consisted of differential amplifier stage, buffer stage, 8 CMOS switches, 16 passive resistors and DC-offset cancellation circuit (DCOC) using the Miller effect. It had perfectly balanced amplifier scheme to reduce input and power supply noises, and the output DC-level is almost zero with 23.9μV. We fabricated PGA using Magnachip/SK Hynix 0.18-μm CMOS 1poly-6metal process. The proposed system showed very low power consumption of 1.137mW, very small gain error of less than 0.24dB, and very small chip area of 0.015mm<sup>2</sup> compared to conventional results.

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