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A 1.8-V operation Analog CMOS Baseband for Direct Conversion Receiver of IEEE 802.11a

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Abstract

This paper describes a CMOS analog baseband circuits for direct-conversion receiver of5GHz IEEE 802.11a. The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA). An active-RC channel selection filter for WLAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover IEEE802.11a (20MHz) including the effect of process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feed forward frequency compensation scheme. For high linearity, the PGA is constructed with op-amp and resistor based inverting amplifiers. For minimum power consumption, the op-amps employ the current re-using feedforward frequency compensation. The input third-order intercept point (iIP3) is 20dBV at the highest gain mode. The input referred noise is $13nV/\sqrt{Hz}$ *at the lowest gain mode. Implemented in a 0.18 m CMOS technology, the gain of the programmable gain amplifier (PGA) can be controlled from 2.5dB to 52.5dB with 0.5dB step.*

Keywords: *WLAN(Wireless Local Area Network), Receiver analog baseband, Channel Selection filter, PGA (Programmable gain amplifier), OP-amp*

1. Introduction

Wireless local area network (WLAN) operating at unlicensed bands has been rapidly gaining its acceptance in the communication infrastructure both in home and office. While the maximum data rate of IEEE 802.11b operating at 2.4GHz band is 11Mbps, 802.11a and 802.11g operating at 5GHz and 2.4GHz band, respectively provides 54Mbps maximum data rate with orthogonal frequency division multiplexing (OFDM) technology [1]. Although both 2.4GHz and 5GHz bands are unlicensed ones, 5GHz band is relatively cleaner than 2.4GHz band which is crowded with various RF systems. Therefore, it is thought that 802.11a will have better chance to dominate the market.

The key requirement on a WLAN transceiver to be accepted in the market is low power consumption and low cost. Therefore, the research efforts are mainly towards a fully

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integrated transceiver mostly in CMOS. Among various receiver architectures, direct-conversion structure provides most highly integrated solution with minimum number of external components, enabling a low-cost and low-power transceiver system [2-4].

RF front end with DCR architecture can be far simpler if ADC has sufficiently large dynamic range so the channel selection filter can be eliminated. However, the power consumption would become extremely large because ADC is normally a power hungry device. The challenge of analog channel selection filter for WLAN is the fact the channel bandwidth can vary in a very wide frequency range depending on the wireless standard. The simplest approach is to have a channel selection filter whose cut-off frequency is fixed at the value for the wireless standard with widest channel bandwidth among the standards being supported. Then, the information is not lost in the channel selection filter even for the other wireless standards. The performance requirements of ADC such as dynamic range and effective resolution become stringent [5]. Therefore, the cut-off frequency of channel selection filter should be tunable depending on the channel bandwidth of each wireless standard. For WLAN to cover multiple wireless standards including PDC(channel bandwidth = 25kHz), GSM, DECT, Bluetooth, and802.11a, the tunable frequency range of channel selection filter should be larger than 3decades. Several research results on dual-mode analog channel selection filter have been reported [6-7], but to the authors' knowledge there has been no true software definable channel selection filter tunable for multiple wireless standards.

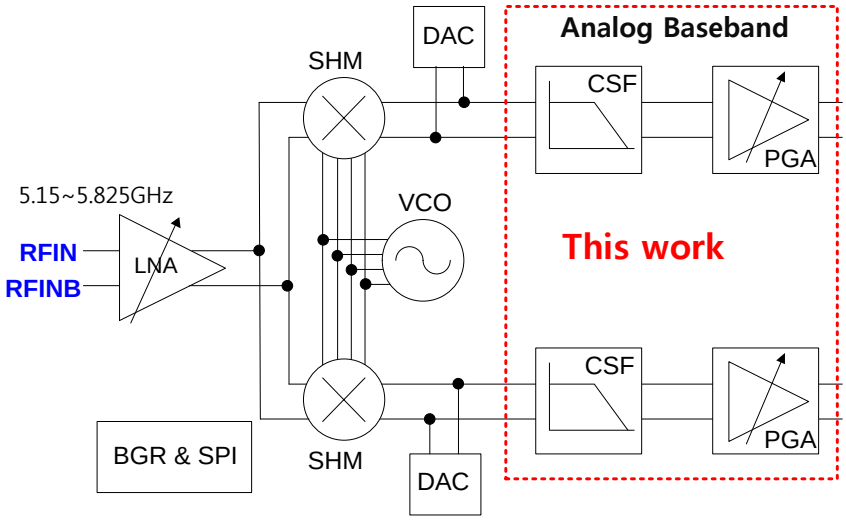

Figure 1. Direct-conversion Receiver for 5GHz WLAN

2. Related Study

The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA), and digital-to-analog converter (DAC) for DC-offset cancellation. At the input of the channel selection filter, I- and Q-paths have separate DC-offset canceling R-2R ladder type DAC with 7-bit resolution shown in Figure 1. For channel selection filtering, a fifth-order chebyshev filter shown in Figure 2 is used because it provides relatively large stop band attenuation with moderate group delay variation within pass band. The dynamic range of the filter is maximized by scaling the resistor values to have the same maximum signal swing for all internal nodes. The simulated cut-off frequency of channel selection filter can be controlled from 6.3MHz to 20MHz as shown in Figure 4.

The gain of the programmable gain amplifier (PGA) in Figure 8 can be controlled from 2.5dB to 52.5dB with 0.5dB step.

2.1. Channel Selection Filter

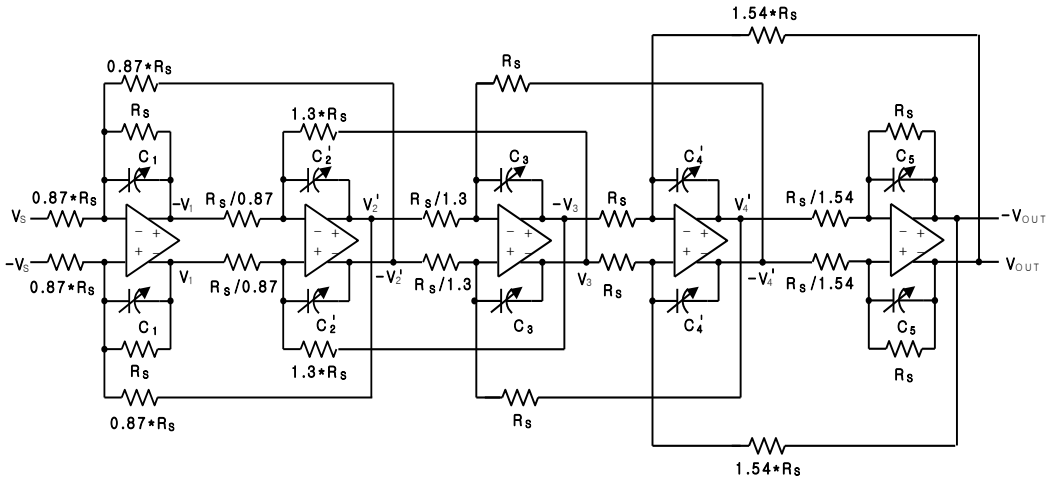

Figure 2. Fifth-order Chebyshev Active-RC filter

For channel selection filtering, a fifth-order Chebyshev filter shown in Figure 2 is used because it provides relatively large stop-band attenuation with moderate group delay variation within the pass-band [8]. Among Gm-C and active-RC type implementation options, active-RC type is adopted for its better linearity. The cut-off frequency of active-RC filter can be tuned by varying the unity-gain frequency of active-RC integrators. The dynamic range of the filter is maximized by scaling the resistor values to have the same maximum signal swing for all internal nodes. The filter's element values after voltage scaling is shown in Table 1. This frequency tuning range is sufficient to cover from DC to IEEE802.11a (10MHz) and process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feed forward frequency compensation scheme [9].

Table 1. Voltage Scaling Element Values

Rs	10KΩ
C1	2.0711pF
C2	2.4763pF
C3	3.5668pF
C4	2.4763pF
C5	2.0711pF

The linearity of the filter is characterized by the third order input intercept point (iIP3) for out-of-band signal (see Figure 3), the filter can achieve IIP3 of 23dBv for simulated result and 18dBv for measured result, respectively. The cut-off frequency of CSF can be controlled from

6.3MHz to 20MHz and the stop-band rejection is larger than 40dBas shown in Figure 4. The results of the linearity simulation and measurement are summarized in Table 2 with other performance parameters.

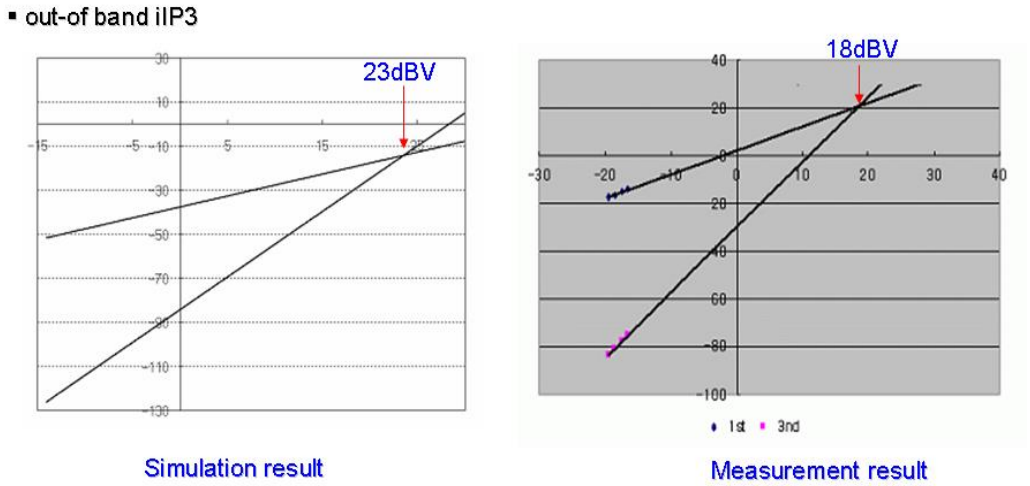

Figure 3. Simulated and Measured IIP3 of LPF

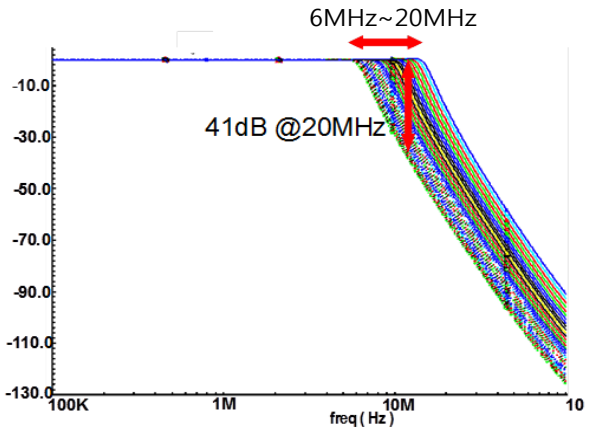

Figure 4. Frequency Response of the LPF for some Control Code

Table 2. Summarized Performance of LPF

Spec.	Target	Simulation	Measurement
DC-gain	0dB	0dB	0dB
Cut-off Freq.	10MHz	10MHz(code 56)	10MHz(code 15)
Pass-band Ripple	0.5dB	0.3dB	0.3dB
Stop-band Rejection	> 35dB @20MHz	38dB @20MHz	38dB @20MHz
Tuning Range	5MHz ~ 15MHz	5MHz ~ 20MHz	6MHz ~ 20MHz
iIP3 (Out-of-band)	20dBV	23dBV	18dBV

2.2. Operational Amplifier

Because the operational amplifier (op-amp) for CSF and PGA should be able to provide virtual ground for out-of-band signals, the required bandwidth of op-amp is much larger than the channel bandwidth. With conventional frequency compensation method using Miller capacitor, however, large bandwidth can be obtained only with large power consumption. The op-amp of this work employs feed forward frequency compensation method shown in Figure 5 whose transfer function is given as;

$$H(s) = -\frac{g_{m1}r_1 g_{m2}r_2 + g_{m3}r_2 + sC_1 r_1 g_{m3}r_2}{(1+sC_1r_1)(1+sC_2r_2)} = -(A_1A_2 + A_3)\times\frac{1+s/z_1}{(1+s/p_1)(1+s/p_2)} \quad (1)$$

where$A_1=g_{m1}r_1$, $A_2=g_{m2}r_2$, $A_3=g_{m3}r_2$, $p_1=1/C_1r_1$, $p_2=1/C_2\,r_2$, and z_1 is given as ;

$$z_1 = p_1\left(1+\frac{A_1A_2}{A_3}\right) \quad (2)$$

There are two choices in compensation the op-amp with the feed forward compensation method; canceling either the first-stage pole p1 or the second stage pole p2 with the zero z1. Since p2 is a function of the load capacitance, it would be better choice to cancel the first-stage pole p1 with z1. Therefore, our choice is to have z1 as close at p1 as possible. It can be achieved by large enough gm3. Since the trans conductance is proportional to the bias current, large gm3 means large current consumption. From the above equations (1) and (2), the phase shift of the poles can be compensated with a left-half plane zero whose position can be varied by controlling A_3. In Figure 6, the op-amp employing the feed forward frequency compensation scheme is shown. In order to save the current consumption, the differential pair (M6 and M7) generating g_{m3} is re-using the bias current of g_{m2} [9]. The simulation results including all the parasitic capacitance indicate 57.4dB DC gain and 332MHz unity gain frequency with 6pF load capacitance as shown in Figure 7.

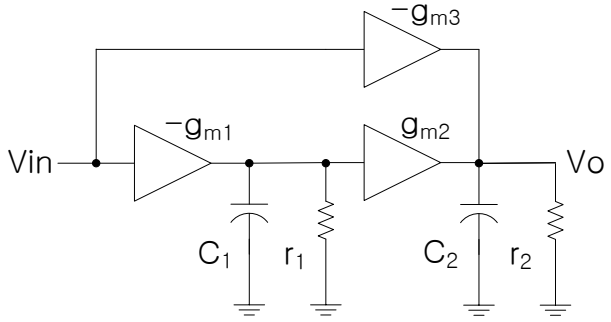

Figure 5. Feed Forward Frequency Compensation of op-amp

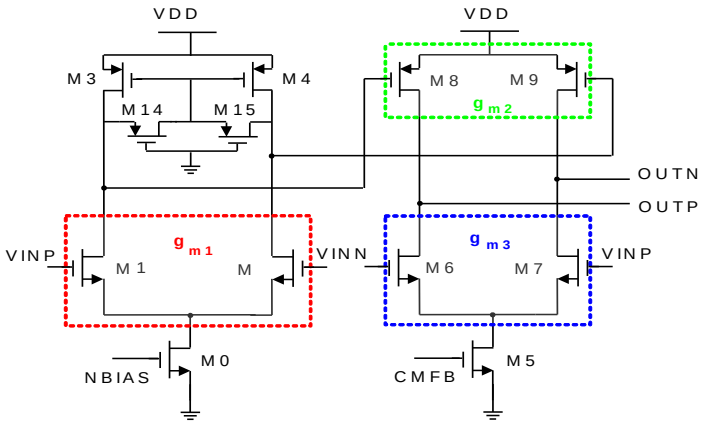

Figure 6. Operational Amplifier for Filter and PGA

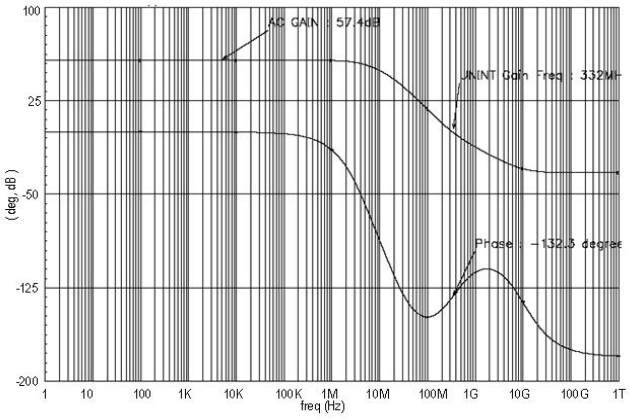

Figure 7. Simulated Frequency Response of Operation Amplifier

2.3. Programmable Gain Amplifier

The PGA is placed between the channel selection filter and the ADC. This arrangement relaxes the linearity requirement on the PGA because the out-of-band interferers are attenuated by the filter. But according to the system simulation result, still the linearity requirement on the PGA is very high and thus the op-amp and resistor based inverting amplifiers are used for the implementation of the PGA as shown in Figure 8.

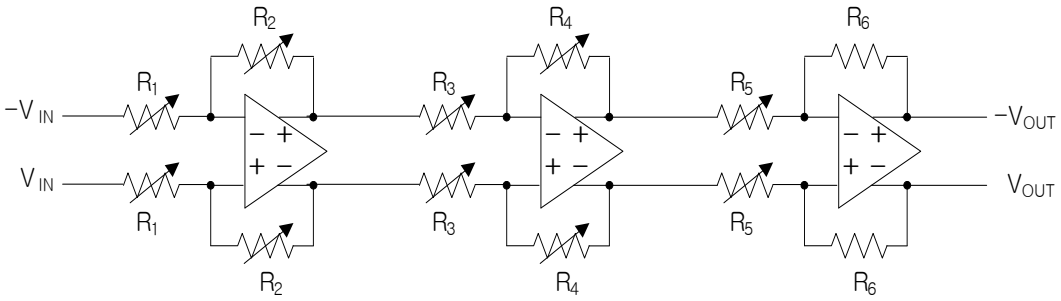

Figure 8. Programmable Gain Amplifier

It is desired to have high-gain op-amp to get the accurate control of the gain of the PGA. For high-gain op-amp, it is usual to have multi-stage architecture which requires the frequency compensation. The most popular method of frequency compensation is the pole-splitting using a Miller capacitor. With the Miller compensation, however, it is very difficult to achieve high-frequency operation with low supply voltage. Therefore, the feed forward frequency compensation method is used instead [9, 10]. In the feed forward frequency compensation, the phase shift of the second pole is compensated by the left half plane (LHP) zero generated by the feed forward path as above mention. As shown in Table 3, the PGA has 50dB gain of the control range with 0.5dB step size. The control of the gain of each stage is illustrated in the Table 3. In order to achieve the accurate gain value, the resistors are implemented with the array of unit resistance. To minimize the variation and silicon area, high-resistivity poly-Si layer is used for the implementation of the resistors. To minimize the gain error and maximize the linearity, the PGA is constructed with op-amp and resistor based inverting amplifiers. With the Op-amps employing the current re-using feed forward frequency compensation method, the current consumption is reduced. For stable operation under all corners, constant current reference is used to bias the PGA.

Table 3. PGA Gain Distribution

Parameter	R1	R2	R3	R4	R5	R6	Total
Gain[dB]	0~18	0~1.5	0~1	0~2	2.5~14.5	fixed	2.5~52.5
Step[dB]	6	0.5	6	2	4	fixed	0.5

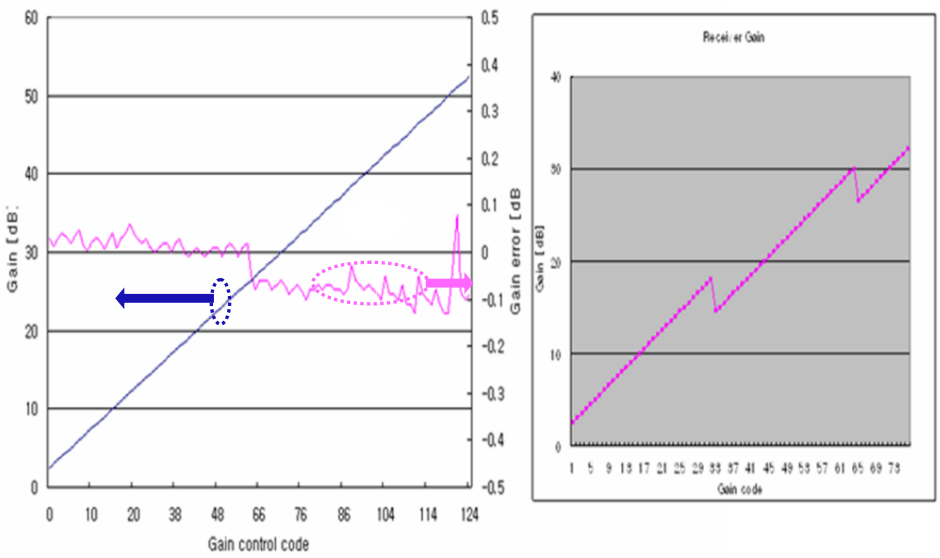

Figure 9. Gain Error of Programmable Gain Amplifier

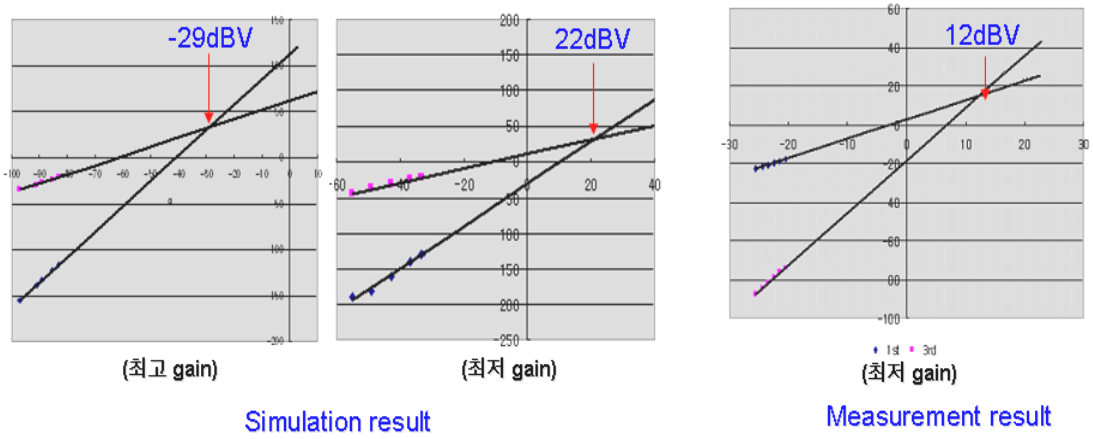

Figure 10. IIP3 of Programmable Gain Amplifier

The simulated gain and gain error of the PGA are shown in Figure 9. The gain error of PGA is smaller than 0.25dB for whole gain control range. The in-band iIP3 is 22dBV and -29dBV, respectively for the highest and lowest gain modes as shown in Figure 10. The input-referred noise voltage is 3.7nV/$\sqrt{\text{Hz}}$ at the highest gain mode. The detailed corner simulation results of the PGA are summarized in Table 4. The MIN corner means -25% variation of the resistance, FF corner of the MOS transistors, 0℃, and 2.0V supply voltage. The MAX corner is +25% variation of the resistance, SS corner of the MOS transistors, 100°C, and 1.6V supply voltage.

The 5GHz direct-conversion receiver baseband has been implemented in a 0.18μm CMOS technology whose microphotograph is shown in Figure 11. The chip occupies a core area of 2.76mm^2 and is packaged in a 48-pin MLF package with exposed die.

Table 4. Summarized Performance of PGA

Spec.		MIN	TYP	MAX
Gain error [dB]		≤ -0.25dB	0.1dB	≤ 0.25dB
iIP3	lowest gain	18dBV	20dBV	23dBV
	highest gain	-30dBV	-29dBV	-27dBV
Input referred noise	highest gain	3.3nV/$\sqrt{\text{Hz}}$	3.7nV/$\sqrt{\text{Hz}}$	4.6nV/$\sqrt{\text{Hz}}$
	lowest gain	10nV/$\sqrt{\text{Hz}}$	13nV/$\sqrt{\text{Hz}}$	21nV/$\sqrt{\text{Hz}}$
Gain range [dB]		2.5~52.5 (0.5dB step)		

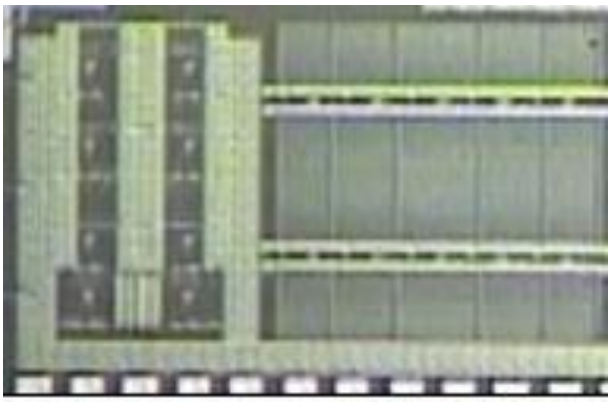

Figure 11. Die Microphotograph of the Direct Conversion Receiver Baseband

5. Conclusion

This paper describes a CMOS direct-conversion receiver analog baseband circuits for 5GHz wireless LAN. The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA). An active-RC channel selection filter for WLAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover IEEE802.11a (20MHz) including the effect of process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feed forward frequency compensation scheme.

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Acknowledgements

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