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Sorting Control System Design of New Materials Sorter Based on FPGA

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Abstract

A new sorting control system in field programmable gate array (FPGA) — the core of control — was proposed because the previous one couldn't meet the requirements of the multi-channel and high yield. It focused on designs of both hardware circuit and FPGA programming module. In the system, the accurate lossless delay of multiple signals was applied by using of RAM and its control module in FPGA. The sorting signals were generated based on the parallel execution characteristics of FPGA program. Real-time communication was realized between CAN controller of SPI and human-computer interface. A large number of experiments were done to test the proposed system. Results showed that the sorting control system could process multi-channel and higher-yield signals significantly. And the materials sorter was improved both in detectable level and yield.

Keywords: *Sorting control system, lossless delay, parallel execution, real-time communication*

1. Introduction

Currently the rapid development of industrial technology, control system design is becoming an important research content [1]. The materials sorter is a processing system used to identify and sort out materials in different colors or shapes, and widely applied for sorting materials such as grain, salt, tobacco, *etc* [2]. The sorting control system in materials sorter mainly processes detection signals from the detection system, and then outputs corresponding driving signals for the sorting solenoid valve [3]. Based on data of different sorted materials, it generally needs tens of millisecond from detecting abnormal materials by the detection system to actuating the sorting solenoid valve [4]. Because the sorter should process materials in dozens or hundreds of channels simultaneously, multi-way as well as parallel processing of detection signals at higher speed is deadly required [5-6].

The previous sorting control system is realized by using counters [7], so its structure and design are too complicated and cumbersome to prevent signal delays. On the other hand, when many abnormal materials at the same channel go through the valve continuously or at a short interval, the delayed signal will lose abnormal materials [8-9]. As a result, the previous sorting control system can't detect effectively.

A FPGA-based multichannel sorting control system with a higher yield has been put forth. In the system, the high-speed processing of multiple signals and accurate delay of multiple signals are available by the dual-port RAM in FPGA [10-11]. By this way, the requirement of highly processing signals by the sorting control system can be satisfied fully for the materials sorter.

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2. System Design

The structure of the new sorting control system in this paper is shown in Figure 1. The sorting control system can be communicated with the human-computer interface through CAN bus, which can connect to FPGA by CAN controller and transceiver in SPI. Therefore, sorting parameters can realize real-time adjustment and control, including delay time and actuation time. By receiving detection signals and communication data, FPGA can conduct accurate lossless delay for detection signals, and generate sorting signals. And then the sorting signals drive the sorting solenoid valve via the drive circuit to realize the sorting of materials.

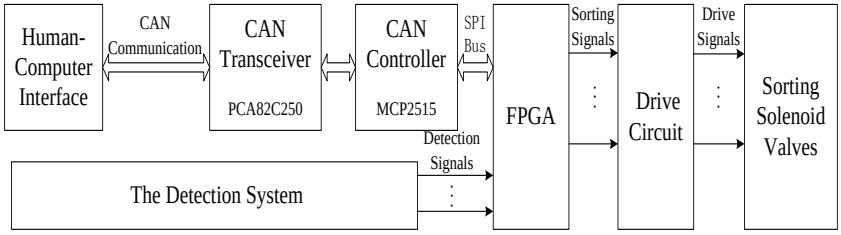

Figure 1. The Structural Chart of Sorting Control System

2.1. Hardware Circuit Design

The hardware of the sorting control system mainly consists of three parts, namely, communication circuit, FPGA signal generation circuit and drive circuit.

2.1.1. Communication Circuit

The data is exchanged through CAN bus and sorting control system on the human-computer interface. After receiving the data set on the human-computer interface, such as delay time and actuation time, the sorting control system sends the display information, for example system status and fault, to the human-computer interface. The CAN communication drive chip adopts PCA82C250, and CAN controller chip MCP2515 with SPI [12-13]. Its SDO, SDI, SCLK and CS pins are connected to the corresponding pins of the SPI module in FPGA respectively; RXCAN and TXCAN pins of MCP2515 are connected to RXD and TXD pins of PCA82C250 accordingly, and the CANH and CANL pins of PCA82C250 are connected to CAN bus.

2.1.2. FPGA Signal Generation Circuit

FPGA adopts the ALTER's EP3C10F256C8 chip, which owns a reputation of a low cost but high performance. It consists of an interior RAM of 400K, more than 10,000 LEs, 2 PLL phase-locked loops and 182 I/O ports, among them, 68 I/O ports with differential input function can satisfy the performance requirement of this control system [14]. Therefore, the FPGA module has the following functions: detecting signal delay, sorting signal generation, communicating of the SPI serial interface module, and so on.

2.1.3. Drive Circuit

The drive-circuit schematic diagram for the sorting solenoid valve is shown in Figure 2, where L1 stands for the sorting solenoid valve, D2 the fly-wheel diode, and Q1 the CMOS tube of the drive sorting solenoid valve. What's more, IN is the sorting signal output by

FPGA, and U1 is the optoelectronic isolator, which can prevent FPGA circuit from being disturbed by drive circuit.

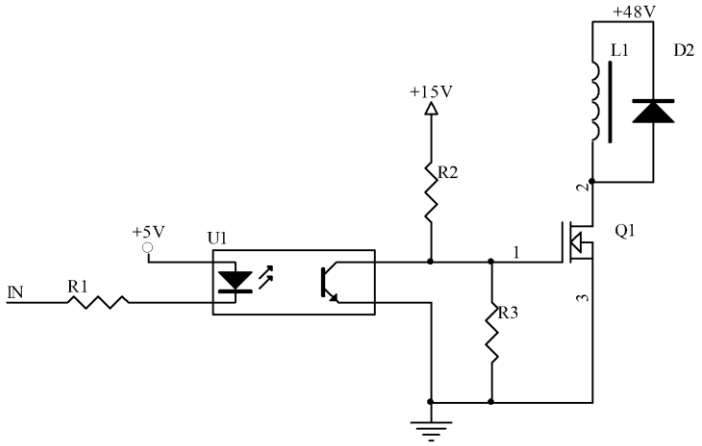

Figure 2. Drive Circuit

2.2. FPGA Programming Design

The FPGA programming structure is shown in Figure 3, mainly including three sub-modules: SPI serial interface, signal delay and sorting signal generation.

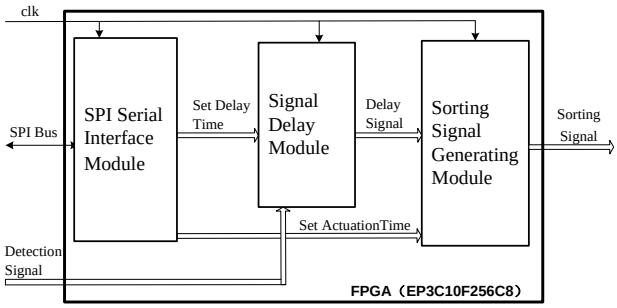

Figure 3. The FPGA Programming Structure Diagram

2.2.1. SPI Serial Interface Module

This sorting control system achieves SPI serial communications in the FPGA. SPI is a serial synchronous communication protocol, which is applicable for connection of primary and slave devices. In this system, the FPGA programmable chip is used as the primary device, while MCP2515, used as a peripheral slave device, is connected to FPGA chip by SPI [15].

SPI consists of SDI (serial data input), SDO (serial data output), SCK (serial shift clock) and CS (chip-selection signal). The CS is the chip-selection signal of the slave device, and its data is output by SDO and input by SDI in communications. The data at the SCK rising edge or falling edge is output from SDO, and then read in by SDI at the falling or rising edge. So the serial transmission of the 16-bit data is finished with 16 times of changes of the clock, after that, these data is converted into 16-bit parallel data by FPGA parallel-serial conversion. The SPI serial interface module is compiled in VHDL language so as to realize exchange of data between FPGA and CAN controller.

2.2.2. Signal Delay Module

In the new sorting control system, the signal delay function is realized by the RAM and its control module in FPGA [16]. Signal delay module is shown in Digure 4.

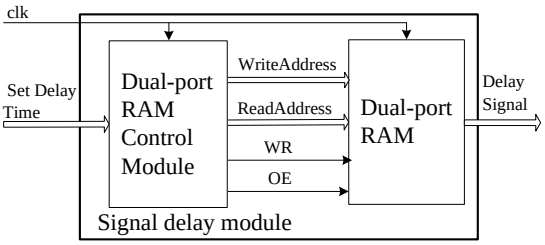

Figure 4. Signal Delay Module

The bits of RAM in FPGA are determined by the number of channel of the sorting system. Taking an example of the N-channel sorting control system, each channel is corresponding to a single-bit datum. The N-channel detection signals makes up a N-bit datum. Therefore, RAM in FPGA is configured as the N-bit RAM. The datum is written in RAM at the rising edge of each clock, and the datum inside of RAM is read out at the same time. RAM in FPGA is configured as the dual-port RAM in order to read and write datum at the same time.

The data-writing and data-reading addresses, read-write signals, and output of enable signals are generated by the dual-port RAM control module. The data-writing addresses generation is shown in Figure 5, where clk stands for the clock signal of the data-writing address counter, and DelayCount the delay counting value. The product of DelayCount and clk periods is the set delay time. The data-writing address counter adds 1 at the rising edge of each clk. The WriteAddress—output of the counter is just the data-writing address, while the data-reading address is the data-writing address plus 1. When the value of the counter is larger than the delay counting value (DelayCount), the counter will start from zero repeatedly.

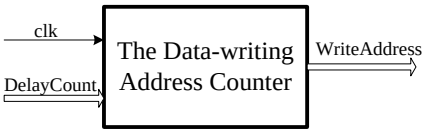

Figure 5. The Data-writing Addresses Generation Module

Reading and writing dataum process in the dual-port RAM is shown in figure 6, where Signal1 stands for writing the data in the first clock, SignalM writing the data in M-clock, and the value of M is DelayCount. So the readout data is just the detection signal written in advance the set delay time.

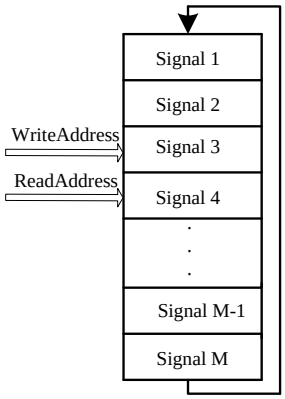

Figure 6. Reading and Writing Dataum in the Dual-port RAM

2.2.3. Sorting Signal Generating Module

The sorting signal generating module is used to generate sorting signals of the solenoid valve based on delay signals and the set actuation time.

Based on sizes of materials to be sorted and their different speeds at the solenoid valve jet nozzle, the actuation time for the sorting solenoid valve varies, and it can be set by the human-computer interface. A counter is set in FPGA for the actuation of each valve. This counter starts to work at the rising edge of delay signals, and outputs sorting signals. It will stop counting when it reaches the set actuating time, and closes the sorting signals. By using the FPGA programming parallel execution, the counters in channels can work separately and accurately to fully satisfy requirements of sorting solenoid valve control in each channel.

3. Results

3.1. The Simulation Diagram of Delay Signals

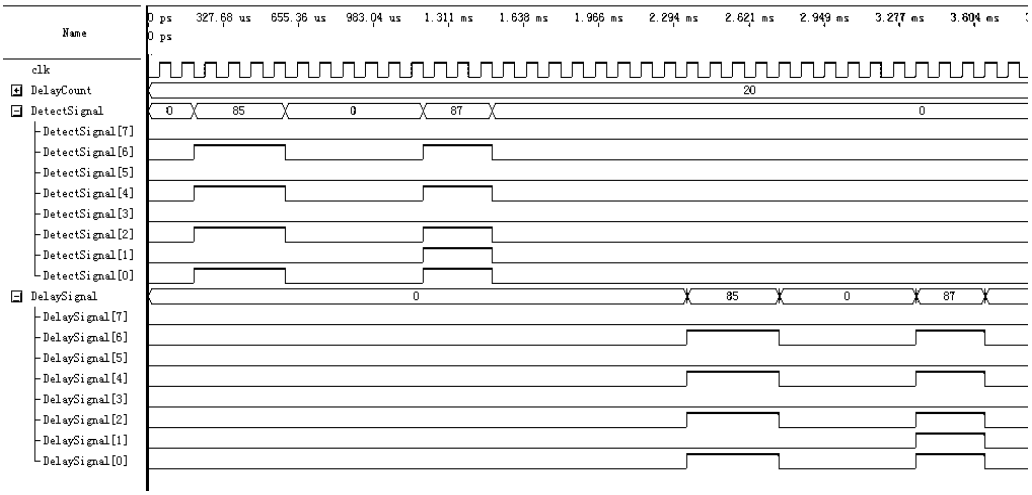

Figure 7. The Simulation Diagram of Delay Signals for the New Sorting Control System

3.2. The Simulation Diagram of Sorting Signals

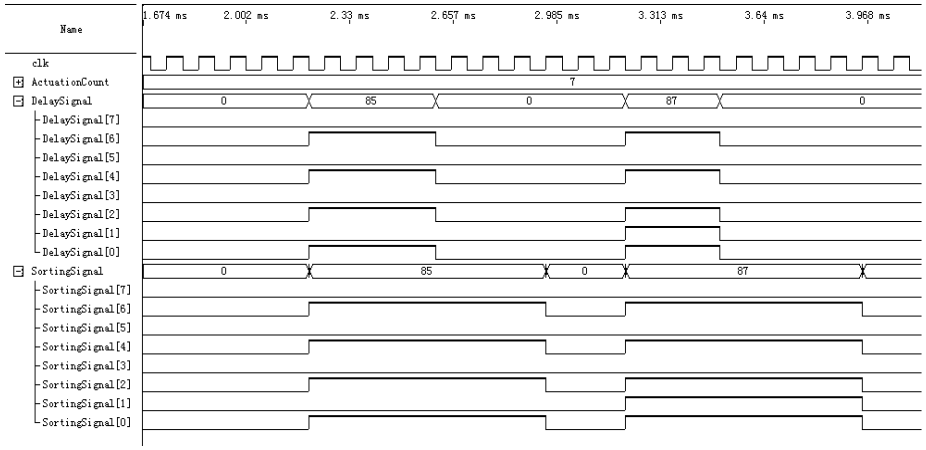

Figure 8. The Simulation Diagram of Sorting Signals for the New Sorting Control System

3.3. Experiment Platform

According to the design described as above, build 64-channel material sorting machine as the experiment platform. The sorting system FPGA of this experiment material sorting machine has procedures as shown in Figure 9: RAM_CONTROL_MODULE is the controlling module that generates dual-port RAM read-write address and control signal; lpm_ram-dp1 is the internal RAM of FPGA, and it configures to 2,084 pieces of 64-bit data dual-port RAM; SPI_MODULE is the interface module for CAN controller MCP2515, in order to realize the setting of parameter data; and Sort SIGNAL MODULE is the produce module for sorting signals.

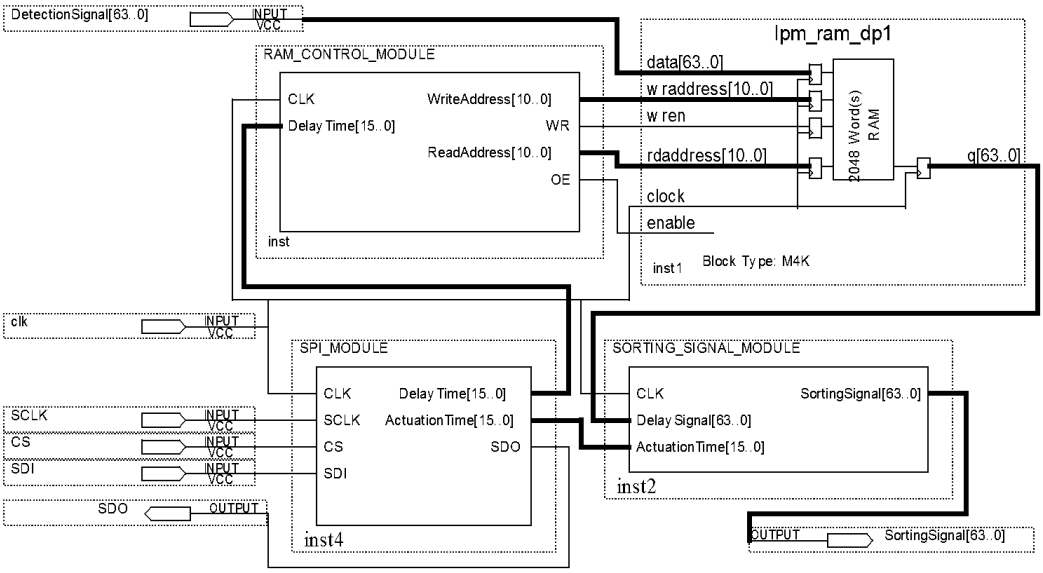

Figure 9. FPGA Program for the Sorting System of Experiment Material Sorting Machine

3.4. Experiment Results

Table 1. Results of Material Sorting Experiment

Output(T/h)	Bad Material Check-Out Ratio (%)	Good Material Carry-Out Ratio (%)
4.0	99.7	5.0
5.0	99.5	8.2
6.0	99.0	14.3
6.5	98.3	18.2
7.0	97.6	25.5
8.0	93.8	39.2
9.0	86.2	50.1

4. Discussion

4.1. Delay Signals

Based on different sorted materials, it needs tens of millisecond generally from detecting abnormal materials by the detection system to actuating sorting solenoid valve, while the sorter should process materials in dozens or hundreds of channels simultaneously. For this reason, the sorting control system requires delaying all channel detection signals for a while, and then, driving the sorting solenoid valve to open the jet nozzle and finish the sortout of abnormal materials [17].

When the detected materials are very small, they go through the jet nozzle in a short time, only 0.5-5ms. Once the time is greater than 0.1ms, the abnormal materials are unable to be sorted out or the normal materials are wrongly sorted out, so that the level of detection is affected seriously. Thus, the delay time of the sorting control system should be set in higher control precision.

The signal delay of previous sorting control system is realized by counting the rising and falling edges of each channel's signal respectively [18]. For example, supposing the delay time is 10ms, the system outputs the signal rising edge after 10ms when the counter 1 at the rising edge of 0 ms starts to count, and the system outputs the signal falling edge after 10ms when the counter 2 at the falling edge of 1ms starts to count, as shown in Figure 10(a). For this delay there are two counters for each channel. The former sorting system can handle the case of two channels. But with more channels, these counters will be null unless a lot of FPGA hardware resources can be supplied.

On the other hand, when the materials sorter has a high yield, the material at the same channel will go through the sorting solenoid valve continuously. Then, it is possible for some abnormal materials to go through the valve continuously without detection. For example, it is 0-1ms for the first abnormal material passing through the sorting solenoid valve, 1-3ms for normal material, and 3-4ms for the second abnormal material. When the second abnormal material signal reaches, the delay counter for the first abnormal material is still working. And

then, the delay counter for second abnormal material is unable to be started effectively. As a result, the signal for the second abnormal material gets lost, leaving the second abnormal material undetected, as shown in Figure 10 (b).

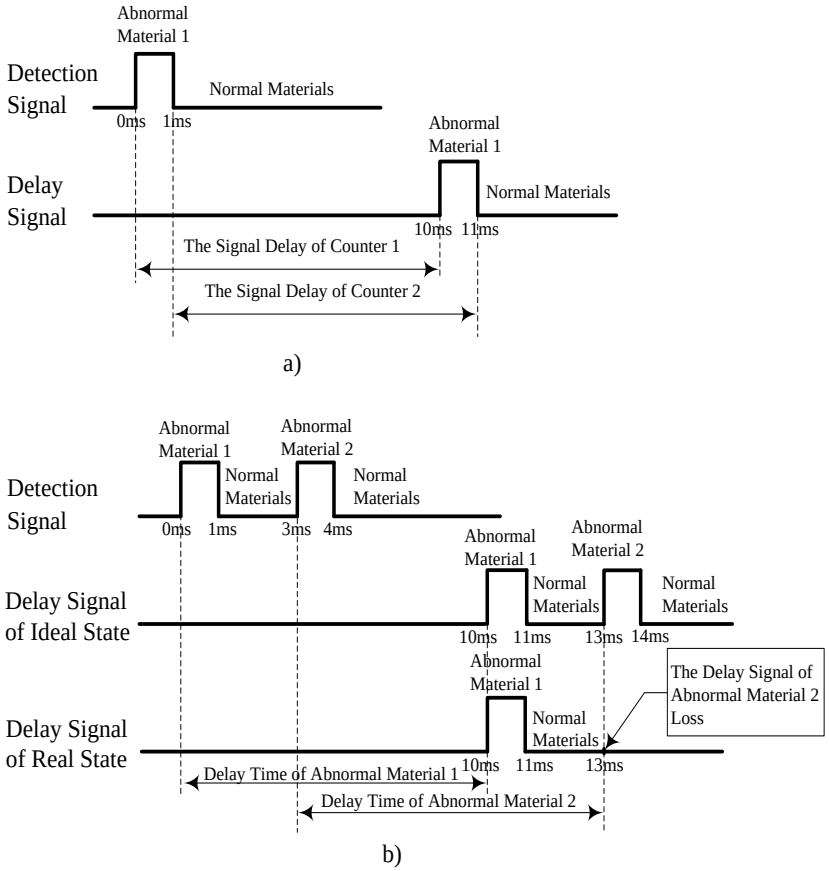

Figure 10. The Signal Delay for Previous Sorting Control System

In the new sorting control system, the signal delay function is realized by the RAM and its control module in FPGA. Taking an example of the 8-channel sorting control system, the simulation diagram of delay signals is shown in Figure 7, where clk stands for the clock signal at the period of 0.1ms, DelayCount the delay counting value, DetectSignal the detection signal, and DelaySignal the signal after delay.

It is seen from the simulation diagram that the value of DelayCount is 20, therefore the delay time is 2ms. The value of the first detection signal is 85 whose effective range is from 0.2ms to 0.6ms. The second detection signal is 87 whose effective range is from 1.2ms to 1.5ms. The interval time of the two detection signals is 1 ms which is less than the delay time. After 2 ms delay, the first delay signal value is 85 whose effective time is from 2.2ms to 2.6 ms, and the second delay signal value is 87 whose effective time is from 3.2 ms to 3.5 ms. the delayed signal is highly consistent with the signal before delay. As a result, the loss of continuous abnormal material signals in the previous sorting control systems can be avoided. The delay precision is 0.1ms in clock period. This meets requirement of the sorting control system completely.

4.2. Sorting Signals

Taking an example of the 8-channel sorting control system, the simulation diagram of sorting signals is shown in figure 8, where clk stands for the clock signal at the period of 0.1ms, ActuationCount the counting value of actuation time for the sorting solenoid valve, DelaySignal the signal after delay, and SortingSignal the sorting signal.

It is seen from the simulation diagram that the value of Actuationtime is 7, so the set actuation time is 0.7ms. The value of the first delay signal is 85 whose effective range is from 2.2ms to 2.6 ms. the second delay signal is 87 whose effective range is from 3.2 ms to 3.5 ms. the value of the first sorting signal is 85 whose effective range is from 2.2ms to 2.9ms. The second sorting signal is 87 whose effective range is from 3.2ms to 3.9ms. Therefore, 0.7ms sorting signals are generated when the delay signals are effective. The sorting signals drive the sorting solenoid valve via the drive circuit to realize the sortout of abnormal materials.

4.3. Experiment Result Analysis

The sorting material of the experiment is rice and the ratio of bad material is about 2%. The horizontal frequency of DetectionSignal that the sorting system input is 8000Hz. According to the machinery and material characteristics, set the DelayTime as 6.2ms, and the ActuationTime as 2ms. Experiment results of different output are as shown in Table 1.

When the output is 4.0T/h, the bad material check-out ratio is 99.7% and the good material carry-out ratio is 5.0%. When the output is 6T/h, the bad material check-out ratio is 99.0% and the good material carry-out ratio is 14.3%. As the output gradually increases, the bad material check-out ratio declines and the good material carry-out ratio increases. When the output is 7T/h, the bad material check-out ratio is 97.6% and the good material carry-out ratio is 25.5%, which has met users' actual requirements. When the output is 8T/h, the bad material check-out ratio is 93.8% and the good material carry-out ratio is 39.2%, which hasn't met users' actual requirements. The result shows that this machine has made great improvements, as compared with traditional 64-channel material sorting machine (maximum output of 5T/h).

5. Conclusions

With a low cost and high performance, the FPGA chip is adopted for the sorting control system of materials sorter, and the accurate delay of multiple signals is realized by its inner RAM and RAM control module. This new design overcomes faults in the previous sorting control system such as losses of continuous abnormal material signals, resources consuming in multichannel signals, and high-cost hardware. In addition, the FPGA chip contains SPI interface module, sorting signal generating module, *etc.*, and owns following functions: the real-time adjustment of parameters with the human-computer interface, and parallel generation of sorting solenoid signals. The results show that the bottleneck has been eliminated in multi-channel and high-yield sorting of the materials sorter. It is of significance to improve the sorting-out level and yield of the materials sorter.

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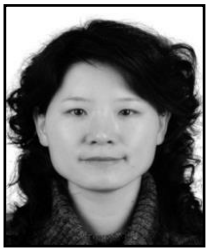

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