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Combinational Circuit Design Based on Quantum-Dot Cellular Automata

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Abstract

Quantum-dot cellular automata(QCA) provides a new approach in computer circuit design and development at nanotechnology level. This technology promises extraordinary high computing speeds, low heat dissipation and highly dense circuits. In this paper,two 2:4 decodersare proposed. The proposed structures reduce the clock phases to only three phases making them faster than the designs currently available in literature.The first proposed structure has reduced number of cells and hence covers a small area.The second proposed method although it has more cells, has regular clock zones that can facilitate the implementation of this circuit.Simulation of the circuits was done using QCADesigner.

Keywords: *Quantum-dot cellular automata, Decoder, Combinational Circuit*

1. Introduction

A trend towards nanotechnology is an inevitable path due to the scaling of down of CMOS technology. This scaling down has resulted in an increase in computing powers but at the same time as a number of problems have been discovered which have prompted the need to find an alternative to CMOS [1, 2]. Quantum-dot cellular automata (QCA) is one such nanotechnology that is proposed to take over CMOS circuit designs. This technology offers low power consumption, very high density circuits and very high computation speeds than current CMOS technologies [3].

Currently a number of research on QCA decoders and their implementation in circuits have been done. In [4], Kianpour *et al.* implemented a 2:4 decoder using a five input majority gate with the aim of simplifying the structure. In this architecture particular emphasis was placed on the circuit stability i.e. the maximum number of cells in awire length per clocking zone was set to 15.

In [5], they implemented a decoder in the design of a field programmable logic array (FPGA). The 2:4 decoders were used in two stages, the first stage uses four 2-input AND gates and the second stage uses eight 2-input AND gates. In the eight 2-input AND gates four were used to enable or disable the output. In [6], they used decoders in a 2-dimensional manner i.e. row decoder and column decoder. This approach results in large unused area [5].

The 2:4 decoder that was presented in [7] uses three majority gates, two inverters and a coupled majority minority gate (CMVMIN) that outputs a majority and minority result simultaneously. This architecture produces an output after five clock phases.

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The organization of this paper is as follows, in Section 2, QCA preliminaries are discussed, in Section 3, proposed QCA decoders are presented, simulation and analysis are given in Section 3 and finally Section 5 provides the conclusion.

2. QCA Preliminaries

2.1 QCA Basics

The basic building block of QCA is a cell. The cell is made up of 4 dots and two electrons. The electrons can tunnel around the cell but they cannot tunnel outside the cell.These electrons repel each other due to Coulombic interaction and occupy two opposite sites. This gives the cells stable states. Logical '0' and logical '1' can be realized using this cell as Figure 1shows (polarization p=-1 and polarization p=+1 respectively) in their ground state position [8, 9, 10].

polarization -1 polarization +1

Figure 1. Ground State Electrons and their Polarization, where Polarization *p*=-1 Represents Logic "0" and Polarization *p*=+1 is Logic "1"

In QCA, wires can also be formed by arranging cells one after the other in line as in Figure 2(a). In QCA neighboring cells also influence each other. In the wire, signals propagate from the input (left hand side) to the output (right hand side) and the wire will have polarization of the input cell. Figure 2(b) shows an inverter chain. This chain is formed by aligning the quantum dots to be at 45 degrees. The value in an inverter chain changes from '1' to '0' and vice versa as it moves along the wire. Figure 2(c) shows the inverter gate. This inverts an input (*i.e.*, '1' to '0' and vice versa) as it moves in the gate. Lastly, Figure 2(d) shows the majority voting gate. This outputs the majority of the three input values A, B, C. Equation 1 gives the majority function of Figure 2(d) [11, 12].

$$M(A,B,C) = AB + BC + AC \quad (1)$$

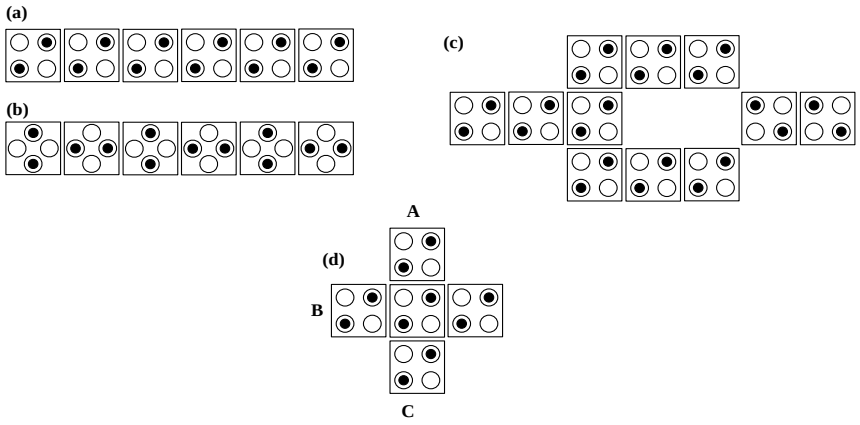

Figure 2. QCA Basic Structures (a)QCA Wire(b)Inverter Chain (c)Inverter Gate (d)Majority Gate

Using the majority gate shown in Figure 2(d), an AND gate and an OR can be implemented. An AND gate can be implemented by fixing one of the input values to 0 and an OR gate can be implemented by fixing one of the input values to 1 [11]. This is important in the design of logical gates in QCA circuits.

2.2 QCA Clocking

In QCA, the flow and direction of information is controlled by the clock signal. In total there are four clock phases which are shifted by 90 degrees from the previous clock phase [9]. The cells in QCA are assigned to one of the clocking regions. Each clock cycle is made up of four clock phases which are switch, hold, release and relax phases. In switch phase, the electrons are free to tunnel between the quantum-dots, this results in computations being performed and also data propagation.

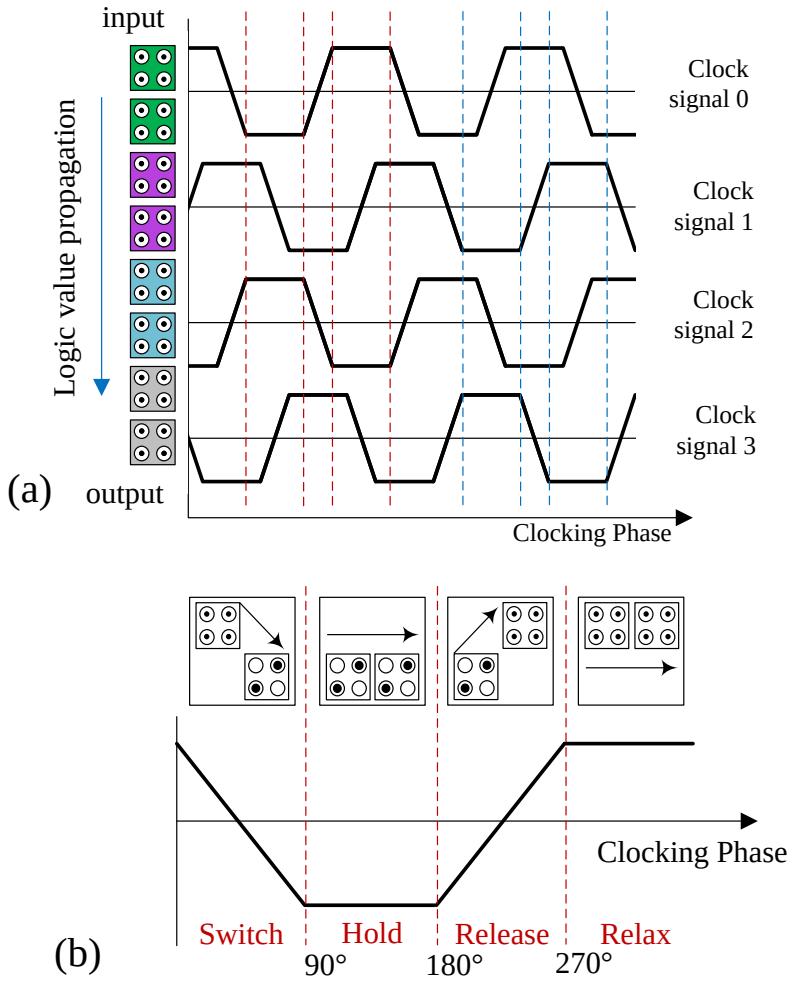

Figure 3. The Clocking Scheme in QCA Showing Four Phases and Four Phases of Operation of the QCA Cells in a Clock Cycle (a)QCA Four Phase Clocking Method (b)Actual QCA Operation in a Clock Cycle

In hold phase, the clock signal remains high thereby preventing tunneling of electrons and resulting in latching the information inside the cell. In release phase, the QCA cells start to lose their stored value, *i.e.*, becomes unpolarized. The last phase is the relax phase. In this phase, the QCA cells lose their value and become unpolarized [13].

3. Proposed Methods

A decoder is a device that selects one out of several output lines when activated for output. Most decoders have *n*-inputs and 2^n outputs. Some decoders have an enable signal that selects the output line [14]. The block diagram for the 2:4 decoder is given in Figure 4. This diagram is made up of four AND gates and two inverters. The outputs Y0, Y1,Y2 and Y3 are produced to meet the equations (2) thru (5) below. Table 1 shows the truth table of an active high decoder of Figure 4 [14]. In this paper we proposeenable high decoders where the enable signal is assumed to be 1 or high. When using a decoder with enable high, the implementation of the actual enable signal in the circuit is ignored.

$$Y1 = \overline{A}\,\overline{B} \quad (2)$$

$$Y2 = \overline{A}B \quad (3)$$

$$Y3 = A\overline{B} \quad (4)$$

$$Y4 = AB \quad (5)$$

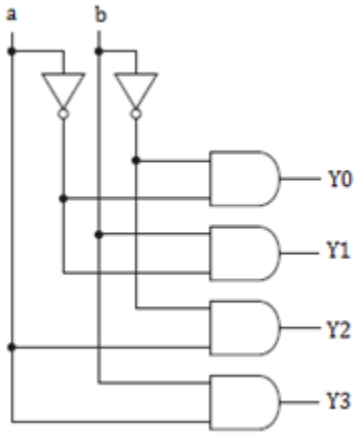

Figure 4. Block Diagram of an Active High 2:4 Decoder

Table 1. Truth Table of an Active High Decoder

(	Y 0	Y 1	Y 2	Y 3
(	1	0	0	0
(	0	1	0	0
1	0	0	1	0
1	0	0	0	1

The block diagram of the first proposed QCA structure is shown in Figure 5. In the block diagram, four AND gates and four inverter gates were used. The first proposed circuit is shown in Figure 6. This structure uses four majority gates and an inverter chain. Due to the

behavior of the inverter chain, the purely inverter gates (like in Figure 2(c)) were not used. The inverter chain alternates the input signal from either 0 to 1 or vice versa as explained above. The layout of the circuit was done so that the outputs to the gates should meet equations (2) through (5) for each specific gate. The outputs for the decoder were placed outside of the main circuits to allow easy scalability and extension of the circuit.

The main advantage of the first proposed structure in Figure 6 is that, it has a fewer number of cells which results in reduced area and hence occupying a small area on the circuit. The second advantage is that the output is produced after three clock phases so that it makes the circuit faster and compact and also it is stable. The circuit was also designed to make sure that it is easy to extend with other circuits hence the outputs were arranged in the proper order.

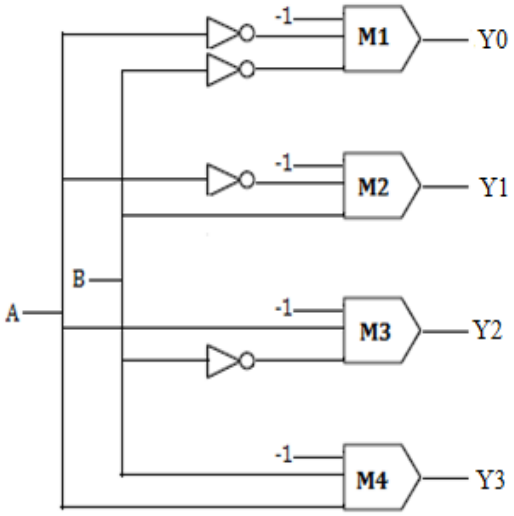

Figure 5. Block Diagram of the Proposed 2:4 Decoder

The second proposed circuit is shown in Figure 8. This circuit was developed using a novel majority gate which was proposed in [15]. In this circuit, four AND gates were used and the inverter chain was used instead of the inverter gates. The most important thing about this circuit is that it has uniform clock zones in its column and hence making manufacturing of this circuit a reality although it has more number of cells than all the circuits presented [15].

4. Simulation and Analysis

The simulation of the circuits was done using QCADesigner tool [16]. This is a CAD tool designed to be specifically used in QCA logic design and simulation. All the cells in a QCA circuit are assigned to a particular clock. In QCADesigner, there are two simulation engines, the coherent vector simulation engine and the bistable simulation engine. The coherence vector simulation is based on a density matrix approach. This can perform time dependent simulation as well as modeling dissipative effects. The bistable simulation engine assumes that each cell is a simple two-state system [16]. In this paper we used the bistable approximation engine for simulation.

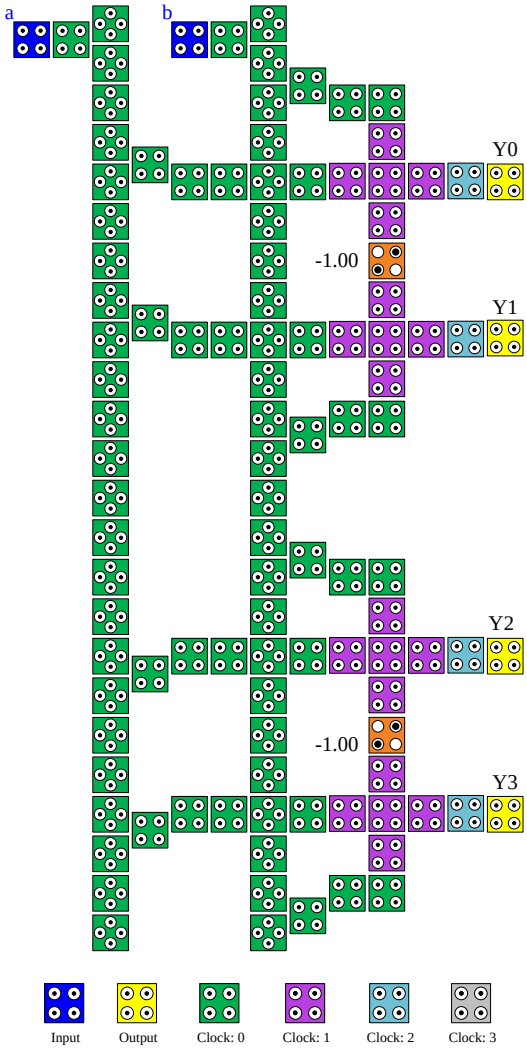

Figure 6. First Proposed Circuit

In QCADesigner, cells are assumed to have width and height of 18nm. The quantum-dots are also assumed to be 5nm in diameter and the cells are placed on a grid with center-to-center distance of 20nm [17].

The simulation results for the proposed structures is shown in Figure 9. The simulation results show that the outputs are produced after three clock phases for our designs which is an improvement of Figure 8.This makes the proposed circuits faster. The results show a correct operation of the circuits. In Table 2, the comparisons between the two proposed methods and the proposal in [7] are given. The comparisons were based on the following criteria, the number of cells, the area covered, number of gates, regular clock zones and the number of clock phases.

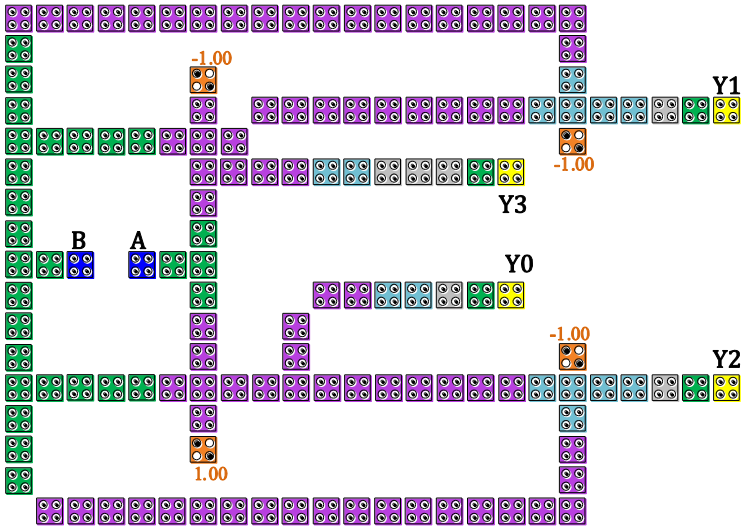

Figure 7. Circuit by Zhou *et al.* in [7]

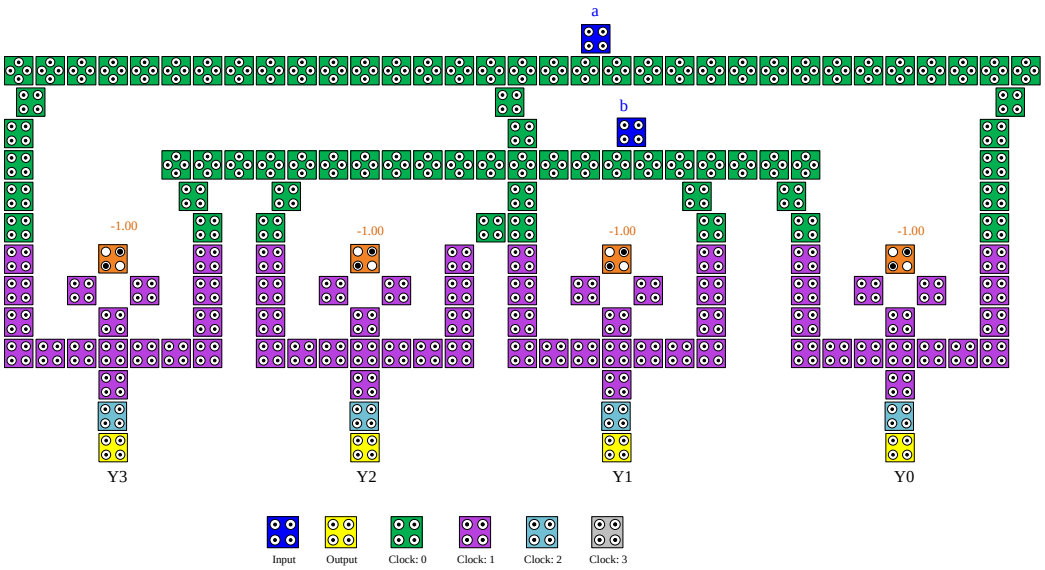

Figure 8. Second proposed Structure

Table 2. Comparison between the proposed methods and the proposal in [7]

	Proposed in [7]	First proposal Figure 6	Second proposal Figure 8
Number of cells	139	110	159
Area covered (nm^2)	163, 592.00	129, 624.00	186, 872.00
Number of gates	6	4	4
Number of clock phases	5	3	3
Regular clock zone	No	No	Yes

Table 2 shows that the first proposed design has an improvement in terms of the number of cells used (110 cells) where as the proposal in [7] has 139 cells. This is an improvement of approximately 21 percent in cell reduction. From Table 2, the number of gates of two proposed designs have also been reduced to only 4 gates. This makes the proposed methods less complex in terms of design and implementation. The second method has one main advantage in having regular clock regions to facilitate actual manufacturing of the circuits and this can lead to improvements in many aspects of computing like [18].

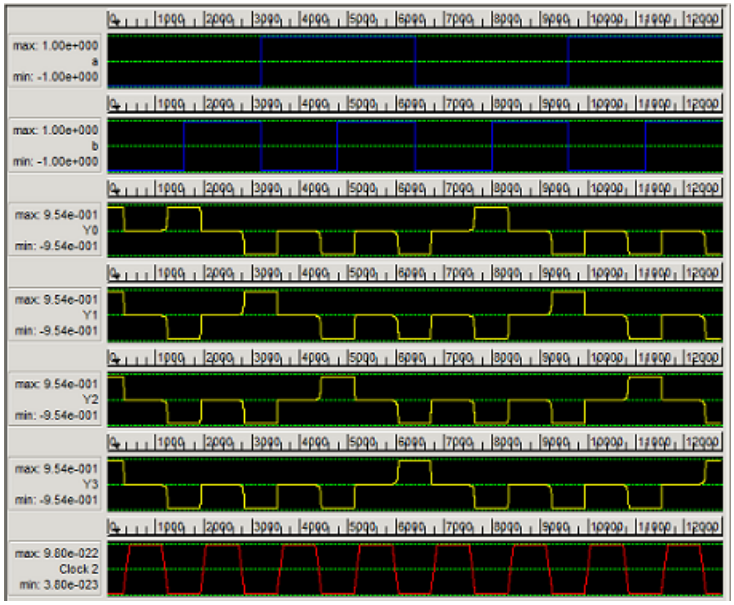

Figure 9. Simulation Results of the Proposed Designs in Figure 6 and Figure 8

5. Conclusion

In this paper, two 2:4 decoders have been proposed. Our proposals were simulated using QCADesigner and these circuits show an improvement in both area and time complexity. In terms of area complexity, the first proposed method has few numbers of cells and this reduction in number of cells makes it more compact and stable. The main reason for designing the second structure was to show that circuits that that have regular clock zones can also be designed and hence making manufacturing of the circuits possible. The improvements in the circuits have been done to make sure that the circuits are easily extended with other structures like RAM and help their performance.

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