International Journal of Control and Automation
Vol.7, No.5 (2014), pp.259-268
http://dx.doi.org/10.14257/ijca.2014.7.5.28

Charge Pump Circuit Design for a Low Input Voltage

Sung-Dae Yeo[1], Young-Jin Jang[1], Kyoung-Kun Lee[2], Seong-Jong Kim[3] and Seong-Kweon Kim[1]*

[1]*Seoul National University of Science & Technology, Seoul, Korea*
[2]*Intelligence and Robot Research Team, ETRI*
[3]*Mokpo National Maritime University, Korea*

ysd1009@seoultech.ac.kr,jyj0129@seoultech.ac.kr,leekk@etri.re.kr, ksj@mmu.ac.kr, kim12632@seoultech.ac.kr
**Corresponding Author: kim12632@seoultech.ac.kr*

Abstract

In this paper, it is a proposal for a charge pump circuit design techniques for boosting the low voltage obtained from energy harvest techniques such as thermoelectric elements. In order to boost the low voltage, it did attempt to minimize the impact of high on-resistance and Clock-Feedthrough. CMOS switch was used, and was controlled not to occur the overlap during operation of the circuit. Charge pump circuit was designed for 4-stage as the condition for boosting low voltage. The simulation result shows, C_n=0.4pF, C_{n+1}=0.3pF, C_{n+2}=0.2pF, C_{n+3}=0.1pF and when load Capacitor was designed by 10pF, 0.3V input voltage became 1.4V about five times by boosting.

Keywords: *Charge Pump, Energy Harvest, CMOS switch, Clock-Feedthrough, On-resistance*

1. Introduction

Due to excessive energy consumption and global warming, energy harvest technology to make use of energy resources efficiently has attracts attentions recently. In particular, energy harvest technology is rapidly growing in the whole industrial and academic world through higher interest, intensive research and development.

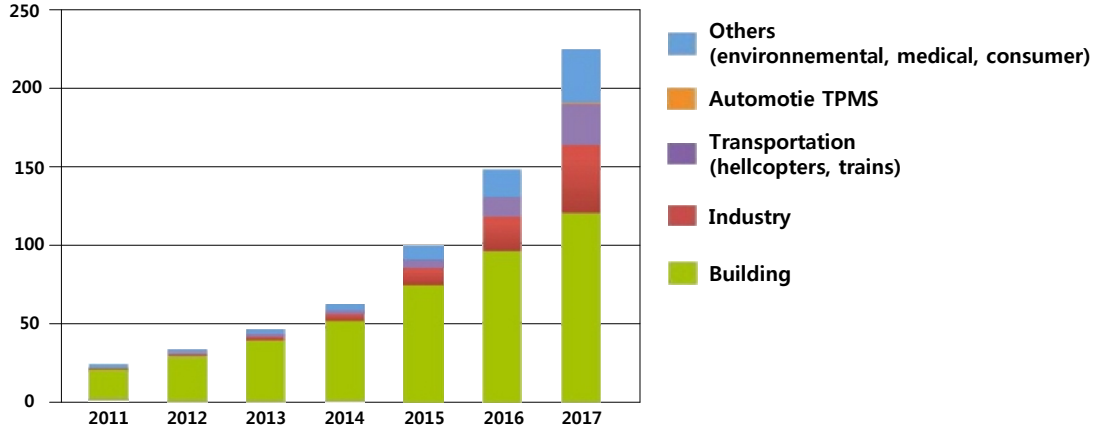

Figure 1. Energy harvest module market forecast by annual value and application [1]

ISSN: 2005-4297 IJCA

Figure 1 Energy harvest module market forecast by annual value and application. It shows building, industry, transportation and othersare growing rapidly.In recent years, the higher energy research is being proceeding, because of electrical energy by energy harvest technology. Utilization of low voltage DC-DC converter is essential in the energy harvest technology. There are several types of DC-DC converter, but boost converter isusually used for raising voltage level. BOOST converter is generally occurs the problem of larger circuit size, because the inductor is used in it. Therefore, in this paper,it is proposed the charge pump circuit for low input voltage to reduce the circuit size and, to induce the use of energy harvest.

2. Problems and Solutions of Charge Pump Circuit Operation for Low Voltage Input

Charge pump circuit is used to boost the DC Voltage for use as power supply of separate application for voltage of 0.3V obtained from energy harvest technique.In case of boosting low voltage, the problem of circuit performance degradation happens due to the influence by the overlap timing of the switch, Clock-Feedthrough and the high on-resistance.

2.1. Concept and Solution for Overlap by Switch Timing

Charge pump circuit is boosting voltage by performing switch ON/OFFoperation. If switchessimultaneously turned ON during other operations,circuit switch timing overlap occurs and the performance degradation will be happened.

Figure 2 shows the operation timing of the designed charge pump circuit.

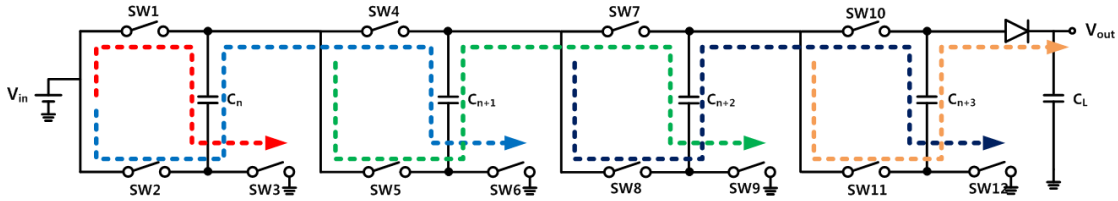

Figure 2. Operation flowchart of charge pump circuit

Designed charge pump circuit has five kinds of the operation are motion. SW1 and SW3 are simultaneously turned ON at the first action.SW2, SW4 and SW6are simultaneously turned ON at the second action. SW5, SW7 and SW9are simultaneously turned ON at the third action.SW8, SW10 and SW12are simultaneously turned ON at the Fourth action. SW11 is turned ON at the operation lastly. Circuit should have been design the not to overlap mutually during each switch operates.

2.2. Concept and Solution of Clock-Feedthrough

Clock-Feedthrough shows performance degradation of charge pump circuit, when electric charge stored V_{in} in capacitor leaks to a parasitic capacitor during the OFF operation of switch MOSFET [6].

Figure3 is a diagram showing a parasitic capacitor of the charge pump circuit.

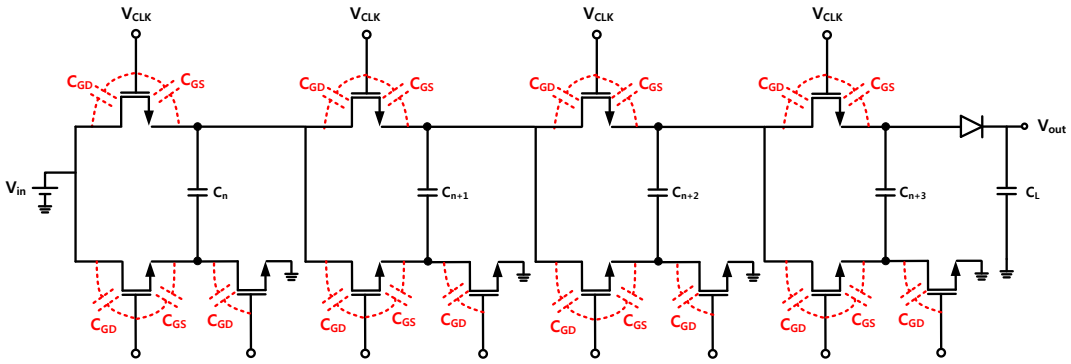

Figure 3. Chargepump circuit'sparasitic capacitor

The capacitor and a parasitic capacitor become to connect in parallelin the case of switch MOSFET OFF operation, after a parasitic capacitor in switch MOSFET. There are happens. At this time, in capacitor(C_n, C_{n+1}, C_{n+2}, C_{n+3}) storing V_{in}switch MOSFET, the electric charge move to parasitic capacitor.

Figure 4 is a diagram illustrating the operation of the Clock-Feedthrough and modifications circuit by parasitic capacitor the switch MOSFET.

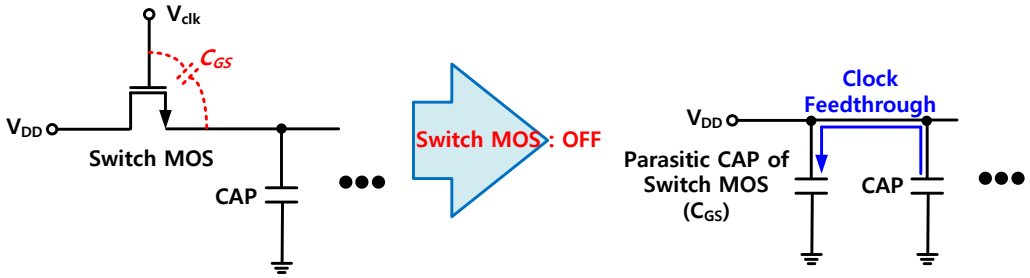

Figure 4. Clock-Feedthrough and operation circuit deformation byparasitic capacitor ofswitchMOSFET

Electric chargeis constant,the parasitic capacitor by OFF operation of switch MOSFET and capacitor (C_n, C_{n+1}, C_{n+2}, C_{n+3}) are connected in parallel each other, the performance of charge pump circuit is reduced. Investigated the CMOS switch connection in the way to minimize this Clock-Feedthrough effect.

Figure 5 shows the connection of the CMOS switch.

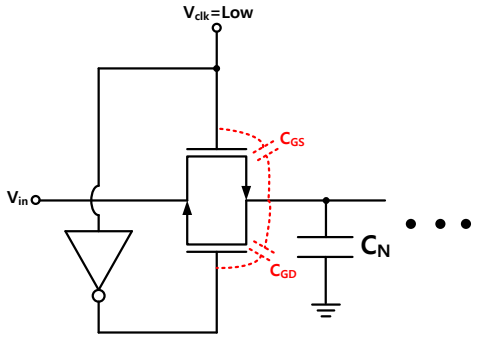

Figure 5. Connection with CMOS Switch

Figure 6 shows the Clock-Feedthrough reduction operation of the CMOS switch.

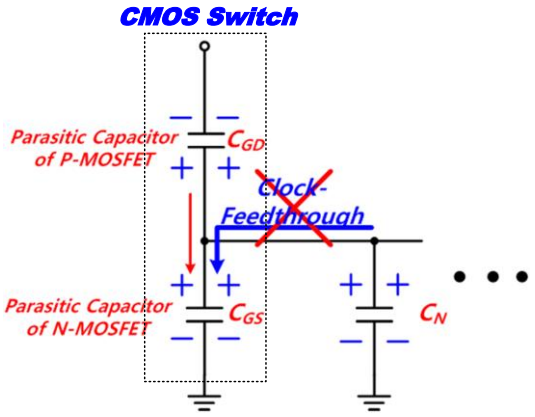

Figure 6. Clock-Feedthrough reduction operationof CMOS Switch

To take advantage of CMOS switch P-MOSFET and N-MOSFET were connected in parallel.The parasitic capacitor generated in OFF operation of the N-MOSFET and the parasitic capacitor of P-MOSFET cancel out the effect. As a result, the effect of the parasitic capacitor by OFF operation of switch MOSFET is ignored. And the influence of Clock-Feedthroughcould be minimized.

Figure 7 shows the simulation results of the V_{OUT} in the N-MOSFET switch and CMOS switch at1-stage of charge pump circuit.

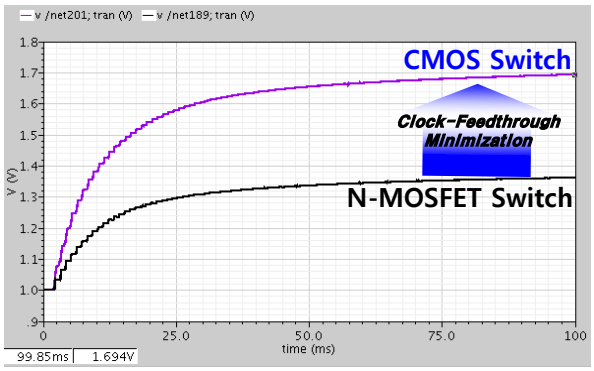

Figure 7. V_{OUT} simulation results from the 4-stage charge pump circuit when the N-MOSFET Switch and CMOS Switch used.

Parasitic capacitor is proportional to the area and inversely proportional to the distance. Therefore, in order to eliminate the parasitic capacitor of the switch MOSFET, it is necessary to design a value which can be adjusted the width of the P-MOSFET, thereby it can cancel out the parasitic capacitor of the switch MOSFET.

2.3. The Concept and Solution of High On-resistance

If a single MOSFET switch designed, transfer characteristic of logic high is lowered due to high on-resistance when it is N-MOSFET.In case of P-MOSFET, the transfer characteristic of the logic Low decreases due to high on-resistance.

Figure 8 shows the reduction of the transmission characteristics due to high on-resistance.

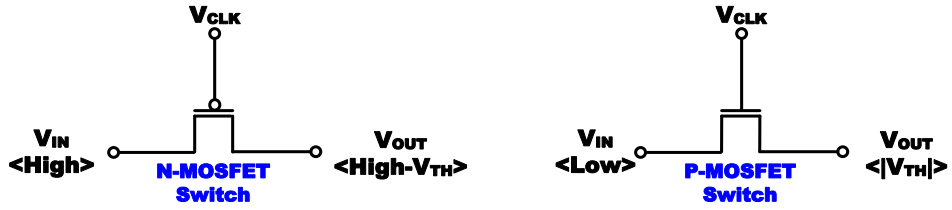

Figure 8. Reduction of the transmission characteristics due to high on-resistance

Figure 9 shows the graph of the MOSFETon-resistance.

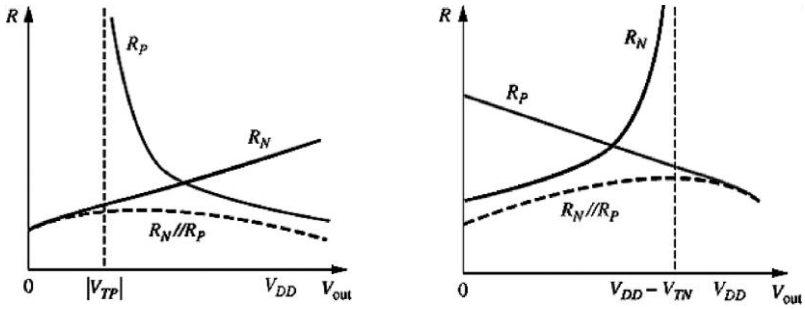

Figure 9. Graph of the MOSFET on-resistance [10]

The use of the CMOS switchwas regarded in order to solve the deterioration of transmission characteristics by high on-resistance.

3. Proposed Charge Pump Circuit Design

Figure 10 shows the structure of the thermoelectric element for voltageacquisition. Voltage obtained from the thermoelectric element is a 0.3 V.

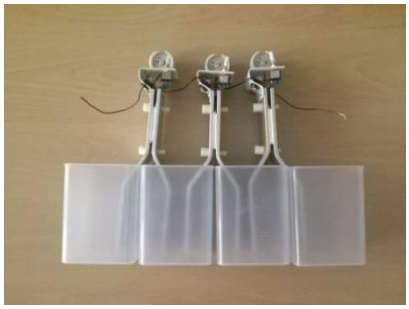

Figure 10. Structure of the thermoelectric element for voltage acquisition

In this paper, it is designed to 4-stage for boosting the low input voltage.Designed charge pump circuit has three of CMOS switch at each stage. And DC voltage of 0.3V is supplied for modeling voltage from obtained by energy harvest.

Figure 11 shows the charge pump circuit designed in this paper.

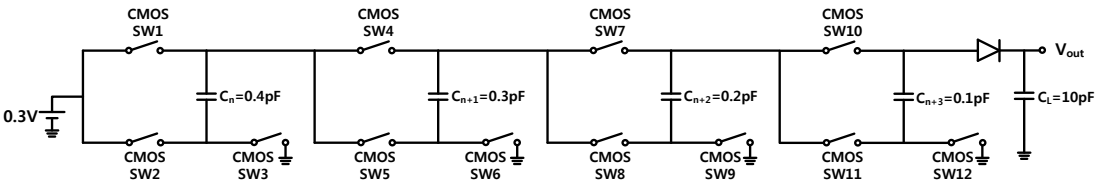

Figure 11. TheCharge PumpCircuitDesign

Do modeling 0.3V of the input voltageobtained by energy harvest.In order to boost the input voltage, it is designed thatC_n of 0.4pF, C_{n+1} of 0.3pF, C_{n+2} of 0.2pF, C_{n+3} of 0.1p and load capacitor of 10pF. Designed circuit is not to make overlap in switch ON/OFF timing to solve the problem of performance degradation.In addition, should connect a CMOS Switch for solving the high on-resistance problem and Clock-Feedthrough.

Figure 12 is shows switch signals for non-overlap operation.

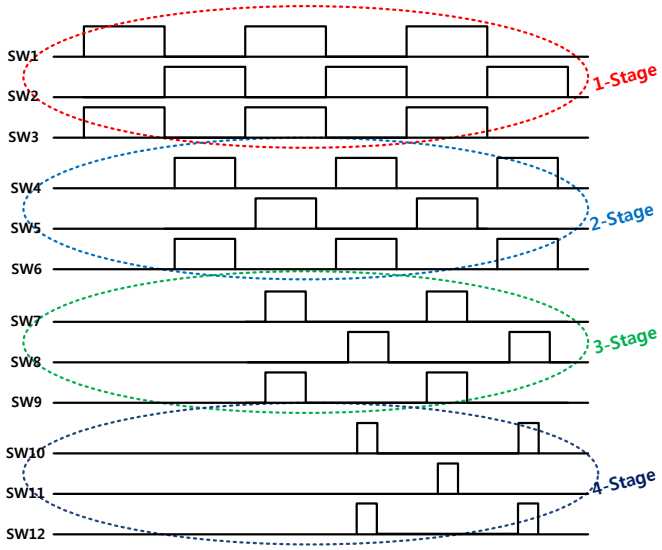

Figure 12. Switch signals for non overlap operation

Figure 13 shows the simulation result of the charge pump circuit.

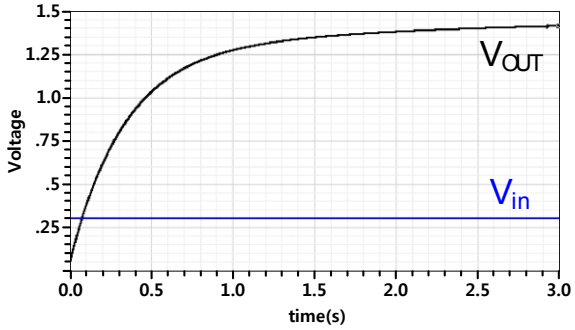

Figure 13. Simulation results of charge pump circuit

It is confirmed that the input signal of 0.3V has been raised to 1.4V in this result of the simulation.

Figure14 shows the layout that contains the capacitor in chip. Effective size is 0.32mm * 0.07mm.

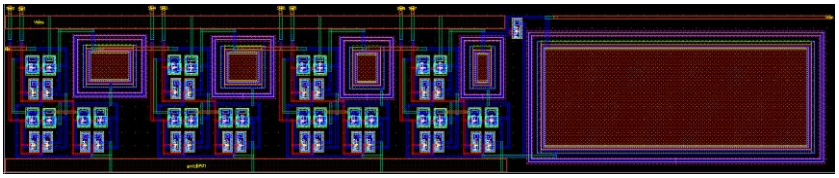

Figure 14. Layout that contains the Capacitor in chip (0.32mm * 0.07mm)

4. Conclusion

In this paper, it is designed the CMOS charge pump circuit for energy harvest. In order to boost low voltage to the stable supply voltage, it is designed that C_n of 0.4pF, C_{n+1} of 0.3pF, C_{n+2} of 0.2pF, C_{n+3} of 0.1pF and load capacitor of 10pF. Then, in order to minimize the impact of the high on-resistance and Clock-Feedthrough, we used a CMOS switch.The pulse width of switch was designed to be a non-overlap. In simulation result, It is confirmed that the 0.3V of input signal has been boosted to 1.4V. This study for charge pump circuit design boosting the low-voltage is expected to be a useful design guidelines.

Acknowledgements

This article is a revised and expanded version of a paper entitled Design of Charge Pump Circuit for Energy Harvest presented at International Symposium on Advanced and Applied Convergence held on November 14-16, 2013 at Seoul, Korea.

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Authors

Sung-Dae Yeoreceived B.S. degree in Electronic Engineering from Mokpo National Maritime University,Mokpo, South Korea in 2011. He received M.S. degree in Electronic Engineering from Seoul National University of Science and Technology, Seoul, South Korea in 2013. Since 2013, he has been Electronic Engineering Ph.D. course in same University. His research interest includes IC Design, Mixed Circuit Design, Low-Power Circuit Design.

Young-Jin Jang received B.S. degree in Electronic Engineering from NamSeoul University, korea in 2012. Since 2013, he has been Electronic Engineering M.S. course in Seoul National University of Science and Technology, Korea. His research interest includes DC-DC Converter, Boost Circuit.

Kyoung-Kun Lee received the M.S degree from the School of Information and Communication Engineering, SungKyunKwan University in Seoul, Korea. He is working to Robot Research Team in ETRI. His research interests include embedded computing system, performance evaluation of intelligence robot.

Seong-Jong Kim received the B.E, M.E and Ph. D degree from Korea Maritime University, Korea.He received the Ph. D degree from Nagoya University, Japan.He is currently a professor in the division of marine engineering at Mokpo maritime university.

Seong-Kweon Kim received Ph.D. in Electronic Engineering from Electronic Engineering Department, TOHOKU University, Japan in 2002. Until 2004, He had been Assistant Professor & Research Fellow in same University. From 2004 to 2009 he worked as Assistant Professor in National Maritime University.Since 2009, he has been Professorin Seoul National University of Science and Technology, South Korea. His research interest includes Wireless Communication IC Design, Analog Circuit Design.