International Journal of Control and Automation
Vol.7, No.4 (2014), pp.153-164
http://dx.doi.org/10.14257/ijca.2014.7.4.14

Design of Wire-Crossing Technique Based on Difference of Cell State in Quantum-Dot Cellular Automata

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Abstract

A wire-crossing is very important technique in quantum-dot cellular automata (*QCA*) *design. Typical wire-crossing techniques have many disadvantages such as demanding of additional tasks and noise occurrence. In this paper, we use a relation between the locked and relaxed stages in order to achieve an efficient wire-crossing. The locked and relaxed stages have a fixed state such as a ground state or an excited state. We control the relation between two stages so that two crossed wires do not have any interference to each other. We design and simulate a simple wire-crossing and a XOR logic gate using the proposed wire-crossing. As a result of it, we can design and construct a regular and noiseless architecture.*

Keywords: *Wire-crossing; quantum-dot cellular automata;QCADesigner; XOR logic gate*

1. Introduction

Since Gordon Moore said that number of transistors on integrated circuits doubles approximately every two years, the reduction of feature sizes and the increase of processing power have been successfully achieved by very large scale integration (VLSI) technology [1, 2]. The microprocessor is one of typical examples, based on VLSI technology, and it is being actively studied in order to increase the integration, performance, efficiency and to minimize the feature sizes. Although many techniques were proposed in order to increase the integration, the development of VLSI technology has reached its peak due to the fundamental physical limits of CMOS technology. In order to overcome these, we need a new technology in nano-scale. One of solutions is a quantum-dot cellular automata (QCA). It not only gives a solution at nano-scale, but also offers new techniques of computation and data transmission [3-9].

A QCA is the computing with cellular automata composed of arrays of quantum-dot devices, and basic concepts of it were introduced by Tougaw and Lent in 1993 [10-11]. The unique feature is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits [7]. In order to transmit data, QCA uses a clocking technique. It is operated by a tunneling barrier.

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ISSN: 2005-4297 IJCA

According to the raising or lowering of the tunneling barrier, the clocking technique consists of four stages: locking, locked, relaxing and relaxed.

In conventional logic design, a wire-crossing was not an important issue because the crossing of two wires is achieved by physically passing one wire over the other with an insulator placed between them. But it is very important in QCA-based logic design because of the properties of cells. Most designs of combinational and sequential logic devices used wire-crossing techniques in order to minimize the time and area complexities [12-19]. According to the state of cells, the number of layers and control of clock phase, wire-crossing techniques are divided into three cases: coplanar-based technique [11, 20, 21], multilayer-based technique [22-24] and crossbar network [8, 9, 25, 26]. Even if these techniques have a lot of advantages depending on the point of each view, there exist many problems such as translation, rotation, consideration of time-dependent latching, additional layers, and so on. Due to these problems, the design based on these techniques demands additional time or area complexity.

Typical state of a cell is two cases by clocking stages: a ground state which has a fixed polarization value '$+1$' or '-1' (this state is that tunneling barriers are completely raised, and called a locked stage) and an excited state which has a free electron (this state is that tunneling barriers are fully lowered, and called a relaxed stage). For any cells $A$and B, if states of A and B are a ground and excited, respectively, they cannot transmit data and also do not affect each other. In this paper, we propose a new wire-crossing technique based on the relation of the ground and excited states. In the proposed technique, there does not exist the problems as mentioned above because we only use the characteristic of cell states. We design and simulate a XOR logic gate using the proposed technique, and it is compared with the previous techniques in terms of efficiency. As the simulation results, we analyze the efficiency and performance between the proposed and previous techniques by QCADesigner [21, 27].

This paper is organized as follows. Section 2 introduces QCA concepts and the previous wire-crossing techniques. The proposed wire-crossing technique is discussed in section 3. Section 4 simulates XOR logic and analyzes the efficiency and performance between the proposed and previous techniques. Finally, section 5 gives the conclusions.

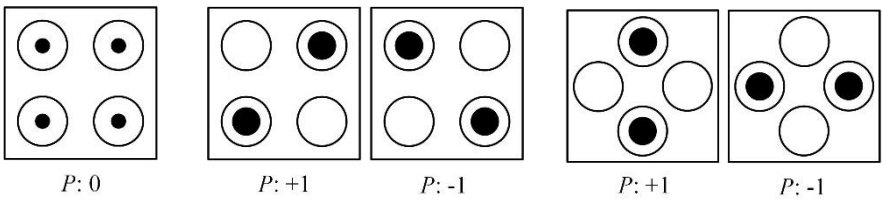


Figure 1. Basic concepts of QCA cell: (a) an unpolarized cell with excited state configuration, (b) standard cells with two ground state configurations and (c) 45° rotated cells with two ground state configurations

2. Preliminary

In this section, we introduce the concepts of QCA and previous wire-crossing techniques.

2.1. Quantum-dot cellular automata

A QCA cell typically consists of four quantum dots placed at the four corners of a square as shown in Figure 1(a).Electrons repulse each other owing to Coulomb interaction, they tend to attain maximal separation by occupying the dots in opposite corners. Two diagonal electron configurations correspond to two energetically equivalent ground states of a cell as shown in Figure 1(b) and (c). The demonstrated bistability allows representation of two binary logic values. The state of a cell is characterized with polarization$P$. The ground state configurations have polarization values of $P = +1$and$P = -1$, which correspond to binary logic values '1' and '0', respectively [4, 10, 11].

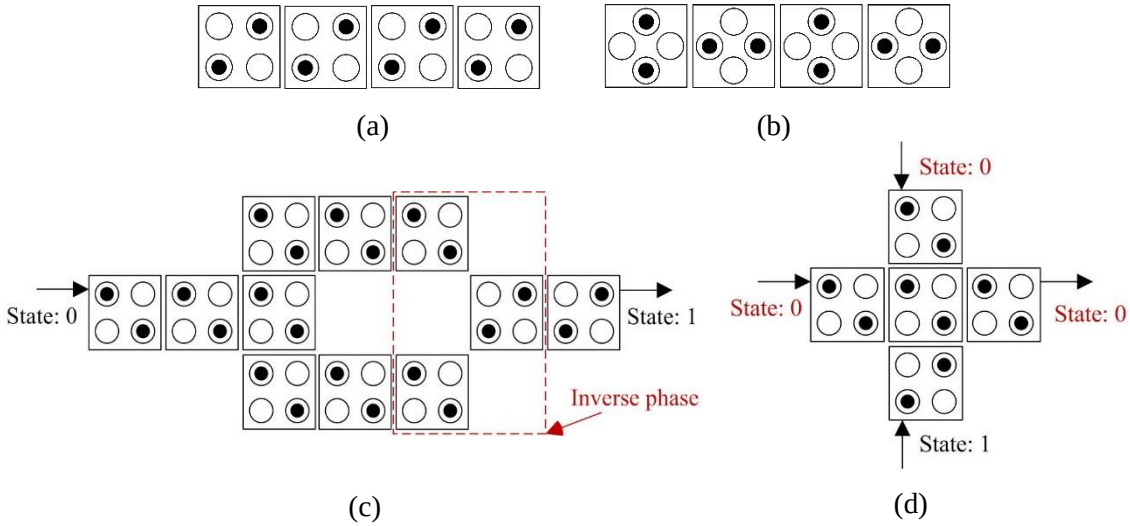


Figure 2. Basic QCA structures: (a) binary wire, (b) invertor wire, (c) formal invertor and (d) majority voting logic with 3input/1output

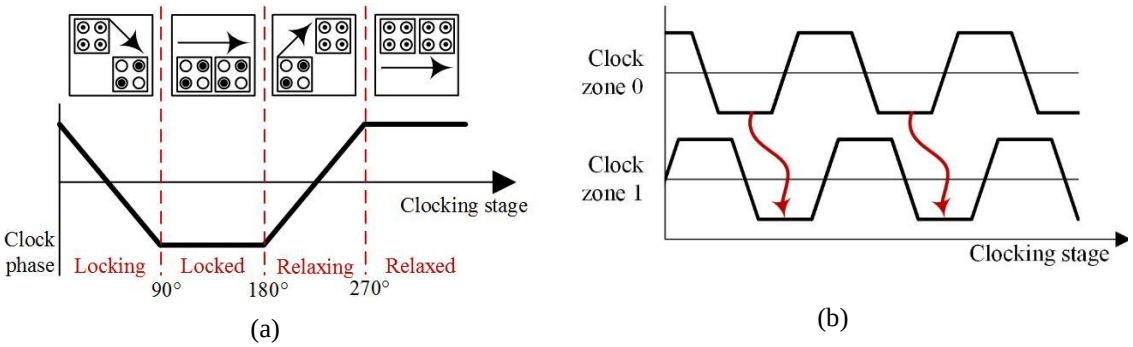


Figure 3. A concept of QCA clocking: (a) four distinct QCA clock stages and (b) data transmission between two clock zones

When cells are placed in a linear array as shown in Figure 2(a), they tend to keep the polarization of the input cell. Such arrangement acts as a binary wire, transmitting the logic value from input to output cell. Also, when 45° rotated cells are placed in a linear array as shown in Figure 2(b), they tend to keep the opposite polarization of the input cell and this arrangement is called an invertor wire. Two basic logic gates on QCA are the invertor and the

majority voting (MV) gate as shown in Figure 2(c) and (d), respectively. The former inverts the logic value of the input signal and the latter calculates the three-input majority logic function $MV(A,B,C) = A \cdot B + B \cdot C + C \cdot A$, where '$\cdot$' and '$+$' indicate AND and OR Boolean logic function. Logic function AND is realized by majority gate with one of its inputs fixed to a permanent logic value 0. Similarly, if one of inputs is a constant 1, the majority gate implements a logic function OR. Thus, an arbitrary QCA circuit can be realized using wire, inverters and majority gates [20, 23, 28].

In order to transmit data, QCA uses a clocking technique based on the raising or lowering of tunneling barriers in a cell. The tunneling barriers are typically modulated through four separate stages as shown in Figure 3(a): the locking stage that the tunneling barriers are raising, the locked stage that tunneling barriers are fully raised, therelaxing stage that tunneling barriers are lowering, and the relaxed stage that tunneling barriers are completely lowered, allowing free electron movement within a cell. A clock cycle consists of four distinct stages, and a clock zone has an arbitrary clock signal. Data transmissions through two clock zones are performed as shown in Figure 3(b). When stages of clock zone 0 and clock zone 1 are locked and locking at the same time, there exists the data transmission from clock zone 0 to clock zone 1, respectively.

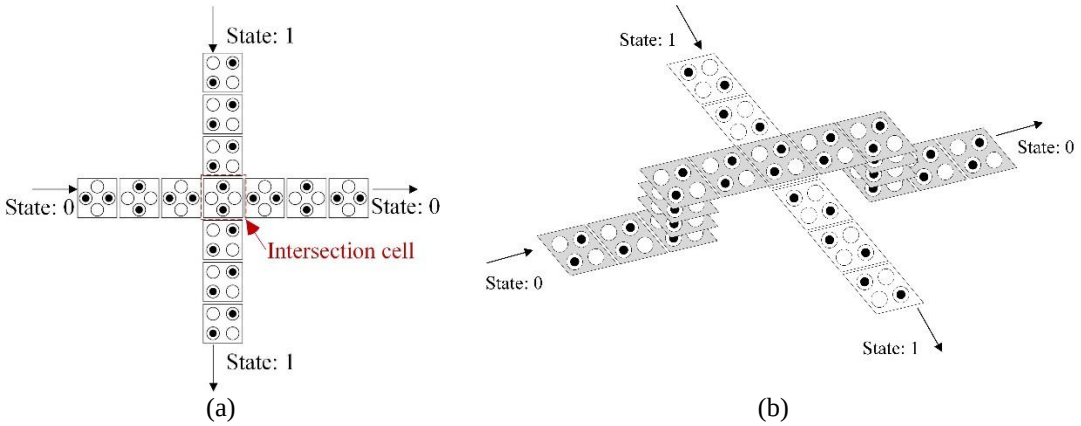


Figure 4.Typical QCA wire-crossing techniques: (a) Geometry example of coplanar-based QCA wire-crossing and (b) Geometry example of multilayer-based QCA wire-crossing

2.2. The previous wire-crossing

There exist three representative wire-crossing techniques: a coplanar-based, a multilayer-based and a crossbar network. Tougaw and Lent [20] proposed a coplanar-based wire-crossing technique as shown in Figure 4(a). In this example, vertical and horizontal wires are transmitting the value '1' and '0', respectively.

In order to implement this wire-crossing, cells of horizontal wire are rotated by 45°. When the number of cells after an intersection in the vertical wire is sufficient (that is, the number of cells is greater than or equal to 3), a transmitting value is not affected by the other wire. The number of cells in the horizontal wire should be composed of odd because of the characteristic of rotated cells. 45°rotated cells induce the additional space between cells. It significantly decreases the energy separation between the ground state and the first excited state, which degrades the performance of such a device in terms of maximum operating temperature, resistance to entropy, and minimum switching time [9].

The multilayer-based wire-crossing technique uses a crossover bridge method. This technique is similar to coplanar-based technique in the perspective of the floor plan because it looks like appearance of two wires crossing. In fact, it consists of the stereoscopic structure as shown in Figure 4(b). In this example, the horizontal chain is using a crossover bridge. The structure of this technique can be more miniaturized and generalized than coplanar-based technique because it does not need to rotate cells. Although this technique has some advantages, there exists the noise problem between intersection cells in crossover area [23]. There are also several things to consider for design and simulation in QCADesigner such as the number of layers, crossover and vertical cells [21].

In 2005, Graunke *et al.* [9] proposed a new wire-crossing technique (this is called a crossbar network) based on parallel to serial conversion and time-dependent latching in order to improve the disadvantages of the previous two techniques. The characteristic of this technique is that two wires are crossed in coplanar without the rotation or translation of cells, and structure of the cell arrangement is regular because of using the parallel to serial conversion method. However, there exists a number of clocks because of time-dependent latching zones. If the clocking is going to be continuously maintained by time-dependent latching, the unexpected results can be occurred such as a difficulty of switching time, an increasing of cell temperature, and a noise of kink energy. Also, this technique requires additional devices such as a parallel-to-serial converter, a shift register and a time-dependent latching device.

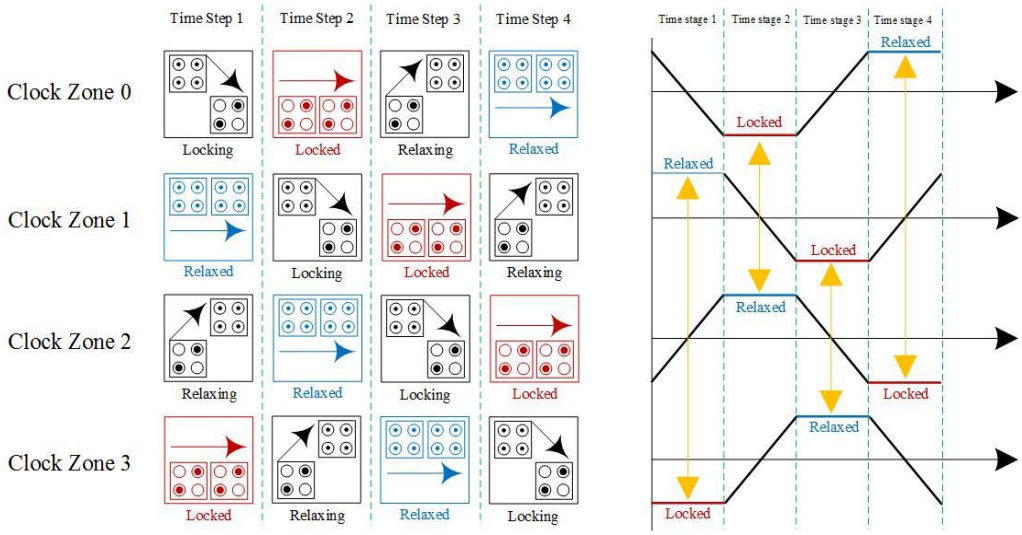


Figure 5. The geometric example of relation of stages for four clock zones

3. The Proposed Wire-Crossing

In this section, we discuss the main concept, design and simulation of the proposed wire-crossing technique.

3.1. The main concept

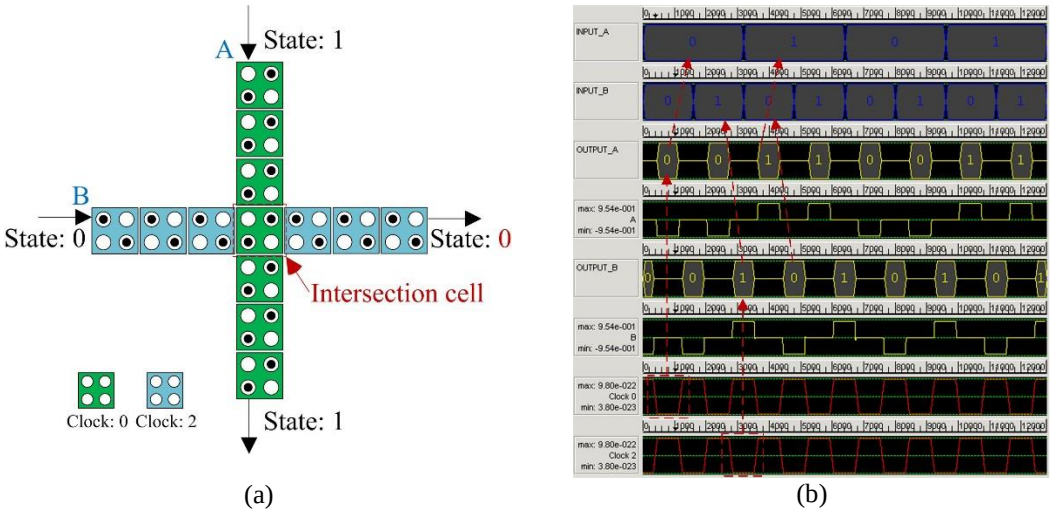
The previous wire-crossing techniques have many structural and temporal problems as mentioned in Section 2.2. In order to solve these problems, we propose a new wire-crossing technique using the relation between the ground and excited states. The principle of the relation between a ground and excited states is as follow.

Typical QCA clocking is divided into four stages by movements of tunneling barriers. In locking and relaxing stages, there exist duplicated states between the ground and excited because tunneling barriers of each stage are still raising and lowering, respectively. The locked and relaxed stages have a fixed state such as a ground state or an excited state. Because tunneling barriers of each stage are completely raised and lowered, respectively.

If two adjacent cells have different clock zones at the same time and each clock zone has the locked and locking stages pair, data transmission is performed within two cells. When a cell at locked stage has a fixed polarization value, the other cell at locking state has the same polarization value due to the Coulomb repulsion within two cells and transformation from an excited state to a ground state. On the contrary, if each clock zone for two adjacent cells has the locked and relaxing stages, the locking and relaxed stages or the locking and relaxing stages, data transmission does not operated within two cells. This is because each clock zone is transformed to a different state.

If each clock zone of two adjacent cells is the locked and relaxed stages pair, meantime, they have different states (that is, ground and excited states) and there does not exist the Coulomb repulsion between the two cells. So, data transmission does not performed without any interference.

In order to design the proposed wire-crossing, we control the relation of each stage as shown in Figure 5. If two adjacent cells have a clock zone 0 and 2 pair in Figure 5, they can perform the wire-crossing because there is no interference at time stage 2 and 4 pair. Also, if two adjacent cells have a clock zone 1 and 3 pair, they also perform the wire-crossing.



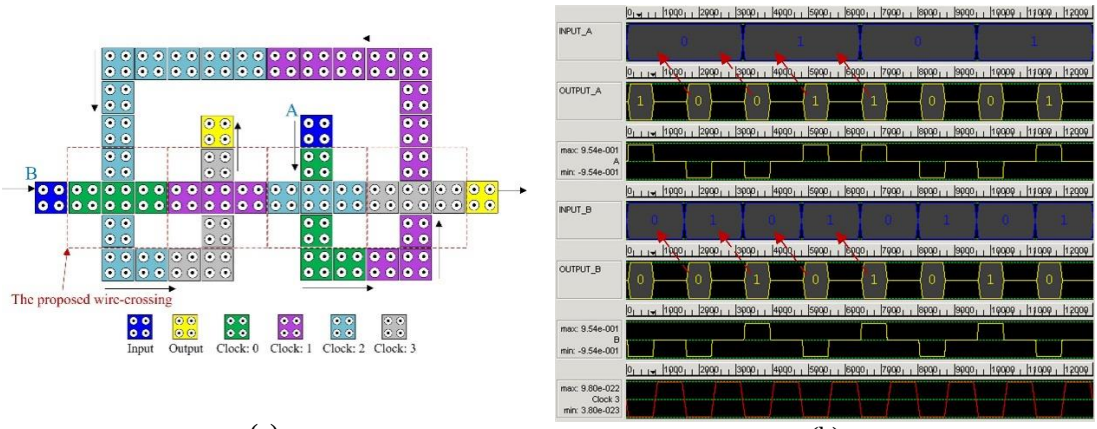
(a) (b)

Figure 6. Geometry examples of the proposed QCA wire-crossing: (a) an example of the wire-crossing using clock zone 0 and 2 pair, (b) a simulation result of (a)

3.2. The design and simulation of the proposed wire-crossing

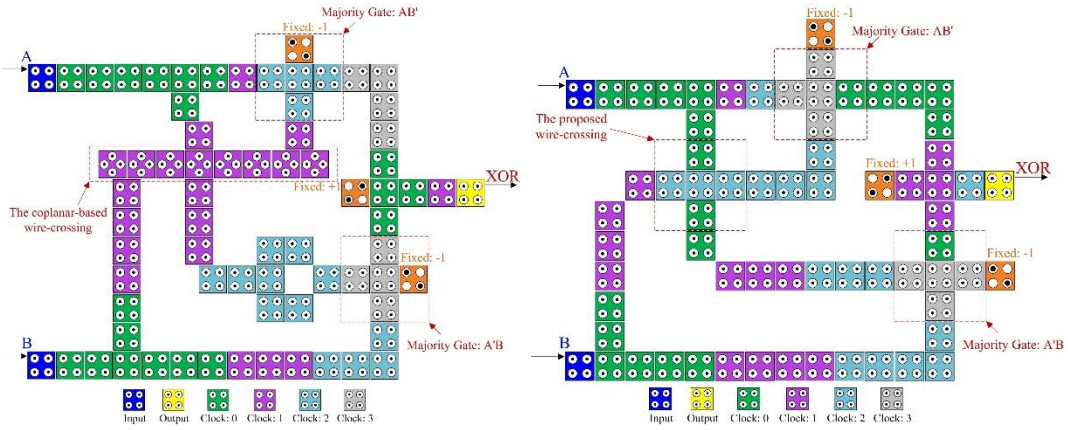
The geometry of the proposed QCA wire-crossing is shown in Figure 6. *A* and *B* wires are transmitting a specific value, respectively without any interference. Each wire-crossing has the relation between locked and relaxed stages such as a clock zone 0 and 2 pair. As shown in Figure 6(a), the intersection cell can be belong to any one of two wires (vertical or horizontal line), and there is no interference each other. In the simulation result as shown in Figure 6(a), we obtained the accurate output values with high polarization.

The simple wire-crossing has been designed using the proposed wire-crossing technique as shown in Figure 7(a). The simulation result in Figure 7(b) shows that two crossed wires do not affect each other without any interference.



(a) (b)

Figure 7. Geometry and simulation result of simple wire-crossing design using the proposed technique: (a) simple wire-crossing using the proposed technique and (b) the simulation result of (a)



(a) (b)

Figure 8. Geometry design of a XOR logic gate with 2inputs/1output: (a) XOR logic gate using the coplanar-based wire-crossing and (b) XOR logic gate using the proposed wire-crossing

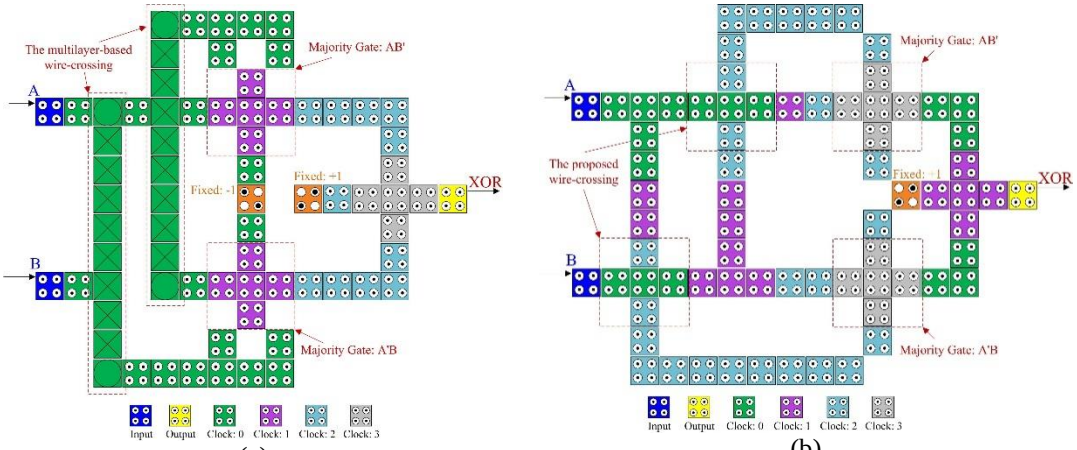


Figure 9. Geometry design of a XOR logic gate with 2inputs/1output: (a) XOR logic gate using the multilayer-based wire-crossing and (b) XOR logic gate using the proposed wire-crossing

Table 1. The comparison result of simple XOR logic gates using the previous and proposed wire-crossing techniques

Wire-crossing techniques		$\#CS$	$\#UC$	$\#CT$
Coplanar	Previous(Fig.8(a))	192 cells	71 cells	6 stages
	Proposed(Fig.8(b))	180 cells	71 cells	7 stages
Multilayer	Previous(Fig.9(a))	169 cells	87 cells	4 stages
	Proposed(Fig.9(b))	169 cells	72 cells	6 stages

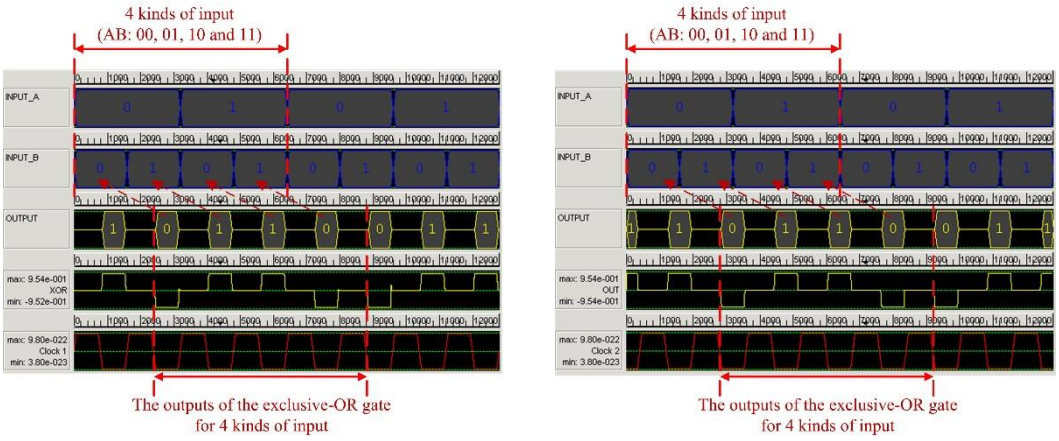


Figure 10. Simulation results of a XOR logic gate with 2inputs/1output: (a) a simulation result of Fig. 8(b) and (b) a simulation result of Fig. 9(b)

4. Design and Simulation of XOR Logic Gate

In this section, we have designed and simulated a XOR logic gate based on the proposed wire-crossing using QCADesigner [21, 27]. The simple XOR logic gate has been designed using the coplanar-based and proposed wire-crossing techniques as shown in Figure 8(a) and (b), respectively. In order to design a simple XOR logic gate in Figure 8(a), it demands a coplanar-based wire-crossing with three MV logic gates, one rotated invertor and one formal invertor. However, a XOR logic gate in Figure 8(b) demands a proposed wire-crossing with three MV logic gates, two simple invertors. We have reduced the number of cells compared with the coplanar-based circuit in Figure 8(a). Also, the cell arrangement of the proposed wire-crossing has more regular structure than the coplanar-based wire-crossing. It requires additional tasks such as a rotation and translation.

Other simple XOR logic gates have been designed using the multilayer-based and proposed wire-crossing techniques as shown in Figure 9(a) and (b), respectively. In order to design a simple XOR logic gate in Figure 9(a), it demands two multilayer-based wire-crossings with three MV logic gates and two formal invertor. But our designed XOR logic gate in Figure 9(b) demands two proposed wire-crossing with three MV logic gates and two simple invertor. The number of invertor cells in the proposed wire-crossing is also less than it of the multilayer-based. Although the cell arrangement of multilayer-based wire-crossing technique is regular, there exist the problems for consideration of the number of layers and the length of crossover. The simulation results of Figure 10(a) and (b) are shown that two crossed wires do not affect surrounding cells, and we obtained the accurate output values with high polarization.

The comparison result of simple XOR logic gates using the previous and proposed wire-crossing techniques was shown in Table 1. Although the number of clock stages of the coplanar-based wire-crossing is less than the proposed technique, we have reduced the number of cell spaces compared with the coplanar-based wire-crossing by 7%. Even if the number of clock stages of the multilayer-based wire-crossing is less than the proposed technique, likewise, we have reduced the number of used cells compared with the multilayer-based wire-crossing by 12%. The reason of increasing for the number of clock stages in the proposed XOR logic gate is because we have controlled clocking stages in order to design the proposed wire-crossing technique. As a result, the proposed wire-crossing has characteristics of very regular and noiseless architecture.

5. Conclusions

In this paper, we proposed a wire-crossing technique using the relation between the locked and relaxed stages. The locked and relaxed stages have a fixed state such as a ground state or an excited state. If each clock zone of two adjacent cells is the locked and relaxed stages pair, data transmission does not performed without any interference. We have shown that a wire-crossing and a XOR logic gate is simply designed and simulated using the relation between the locked and relaxed stages without any other additional tasks and considerations. Although the number of clock stages of the proposed wire-crossing was bigger than it of the previous wire-crossings, the result of the number of cell spaces and the number of used cells in the proposed wire-crossing is superior to it of the previous wire-crossings.

Acknowledgements

This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education, Science and Technology(NRF-

2012R1A1A2008348), and also partially supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Science, ICT & Future Planning (2011-0014977).

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