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A 1.1 V 81.8 dB Delta-Sigma ADC

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Abstract

A 1.1 V 81.8 dB delta-sigma analog-to-digital converter (ADC) is presented. The split time integration technique for implementing multi-bit digital-to-analog converter (DAC) without using DEM has been developed and used. In order to reduce power consumption and area, a successive approximation register (SAR) ADC is employed to function as both multi-bit quantizer and summing adder without using an additional amplifier. The proposed delta-sigma modulator operates at a 640 kHz clock rate and dissipates 850 μW with a 1.1 V supply. It achieves 81.8 dB dynamic range (DR), 76.8 dB signal-to-noise and distortion ratio (SNDR) over a 5 kHz signal bandwidth. The core area is 235 μm^2 in a 45-nm CMOS technology.

Keywords: *delta-sigma ADC, feed-forward, successive approximation register ADC*

1. Introduction

Today's mobile devices are equipped with a lot of embedded sensors, such as a temperature sensor, altimeter, barometer, accelerometer, gyroscope, microphone, and camera which are enabling new features of the devices. In these embedded sensor modules, analog-to-digital converter (ADC) is one of the most important building blocks of the analog front-end (AFE) circuitry. Since the complexity of the AFE is affected by the resolution of the ADC, delta-sigma topology, which provides high dynamic range (DR) by using an oversampling and a noise shaping, is a well suited candidate for sensor interface [1]. Even though the signal bandwidth of delta-sigma modulator is limited by oversampling, it is still wider than the signal bandwidth of sensor output [2, 3].

In this paper, a second-order feed-forward delta-sigma modulator with a 4-bit quantizer is proposed. To resolve nonlinearity caused by multi-bit digital-to-analog converter (DAC), a split time integration technique is proposed. A successive approximation register (SAR) type ADC is used to implement both a 4-bit quantizer and a summing adder without using an additional amplifier.

The paper is organized as follows. Section 2 discusses the architecture of the proposed delta-sigma modulator. In Section 3, the circuit implementation of the modulator is explained. Section 4 describes the measurement results. Finally, conclusions are drawn in Section 5.

2. Architecture

Figure 1 shows the proposed second-order delta-sigma modulator. The linearity requirements of the integrators are relaxed by using the feed-forward topology, since the integrators only process the quantization noise [4]. The transfer function of the proposed modulator is given by

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$$Y(z) = U(z) + (1 - z^{-1})^2 Q(z) \quad (1)$$

where Y(z) is an output of the modulator, U(z) is an input signal and Q(z) is a quantization noise. In the proposed modulator, a multi-bit quantizer is employed to optimize the performance. However, the nonlinear transfer characteristics of the multi-bit feedback DAC result in performance degradation. To alleviate nonlinear error, dynamic element matching (DEM) technique which randomizes a sequence of mismatch error is commonly used [5-7]. But, the distortion is only converted into random noise and still affects the overall performance [8]. In this paper, split time integration technique using 1-bit DAC is proposed to implement multi-bit DAC without using a DEM. Moreover, a SAR type ADC is used to implement both a 4-bit quantizer and a summing adder without using an additional amplifier.

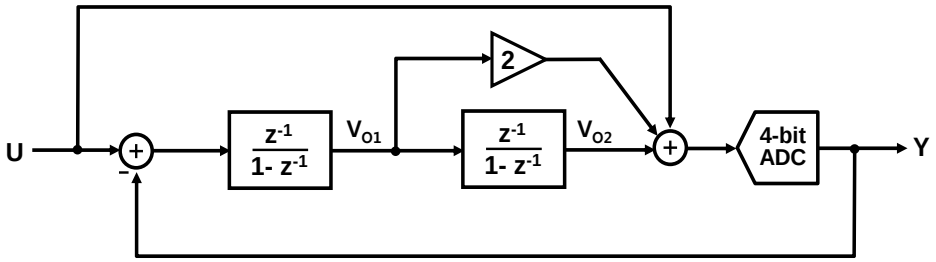

Figure 1. Second-order multi-bit feed-forward DSM

3. Circuit Implementation

The proposed delta-sigma modulator which consists of two integrators, a 4-bit SAR ADC is illustrated in Figure 2.

3.1. Integrator with the proposed multi-bit DAC

The circuit implementation of the integrator with the proposed multi-bit feedback DAC is shown in Figure 3. The operation is as follows. During the ϕ_1 phase, input signal is sampled into the sampling capacitors C_S while the 8-bit control signal for DAC operation is generated from 4-bit output of the quantizer.During the next ϕ_2 phase, integrating DAC operates with ϕ_3 and ϕ_4 clocks, while sampled input signal is transferred to feedback capacitor C_F with ϕ_2 clock. During the ϕ_3 phase, reference voltage is sampled into DAC capacitor C_D according to 1-bit control signal, D_k, and sampled charge in C_D is integrated into C_F during the ϕ_4 phase. These 1-bit DAC operation repeats 8 times during the ϕ_2 phase. The output of the proposed integrator with an ideal opamp is given by

$$V_{OUT}(n) = V_{OUT}(n-1) + \frac{C_S + \Delta C_S}{C_F} V_{IN}(n-1) + \frac{C_D + \Delta C_D}{C_F} \sum_{k=0}^{7} D_k V_{REF} \quad (2)$$

whereΔC_D is the mismatch error of DAC capacitor, ΔC_S is the mismatch error of the sampling capacitor. The gain of the proposed split time integration DAC can be found from (2) as

$$G_{DAC} = \frac{C_D + \Delta C_D}{C_F} \quad (3)$$

As shown in (3), it provides a constant gain error for DAC operation which has a linear transfer characteristic [9].

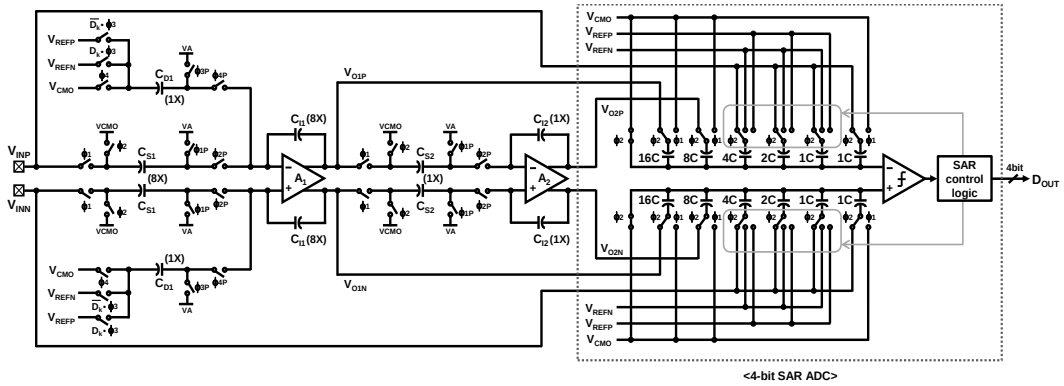

Figure 2. Circuit implementation of the proposed delta-sigma modulator

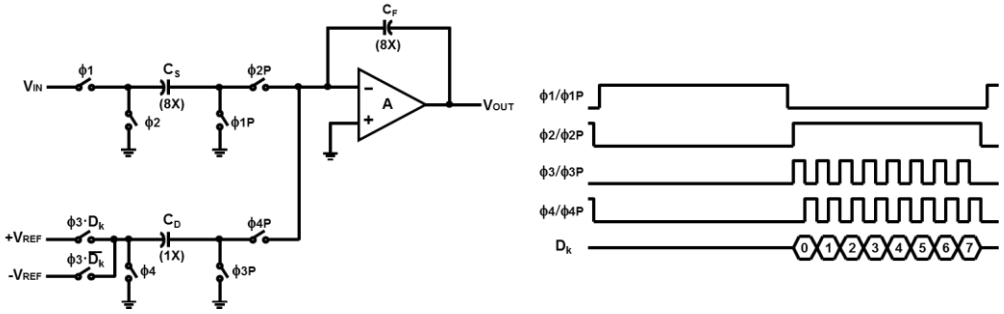

Figure 3. Circuit implementation of the integrator with the proposed multi-bit DAC

3.2. Proposed multi-bit quantizer using SAR ADC

The proposed 4-bit SAR ADC which includes a summing adder is shown in Figure 2. It consists of a binary weighted capacitor array, a comparator and SAR control logic. The operation of the proposed SAR ADC is as follows. During the ϕ_2 phase, the top plates are reset to the common-mode voltage, V_{CMO}, while the bottom plates are connected to each signal. During the next ϕ_1 phase, the top plates are disconnected from V_{CMO} and the bottom plates of the capacitors are switched to V_{CMO} and then comparator decides most significant bit (MSB). After the decision of MSB, bottom plates of 4C, 2C and C are switched to V_{REFP} or V_{REFN} according to the previous comparator output [10]. The comparator input signal after the completion of the conversion is given

$$V_+ - V_- = \frac{1}{4}\left[\left(V_{IN} + 2V_{O1} + V_{O2}\right) - \left(\frac{1}{2}D_3 + \frac{1}{4}D_2 + \frac{1}{8}D_1\right)\cdot V_{REF}\right] \quad (4)$$

where, $V_{IN}=V_{INP}-V_{INN}$, $V_{O1}=V_{O1P}-V_{O1N}$ and $V_{O2}=V_{O2P}-V_{O2N}$. A timing generation for the proposed SAR ADC is facilitated by using an asynchronous control using internal loop delay.

4. Measurement Results

The prototype delta-sigma modulator was fabricated in a 45-nm CMOS technology. Figure 4 shows a measured output spectrum for a 1 kHz 640 mV peak-to-peak differential input sine wave, with a 1.1-V power supply. The SNR and SNDR versus input level curve is illustrated in Figure 5. This prototype IC achieves 76.8 dB of SNDR, 82.2 dB of SFDR and 81.8 dB of DR. Figure 6 shows the layout of the proposed ADC. The core area occupies 235 μm^2. The total power consumption is 850 μW. The overall measured results are summarized in Table 1.

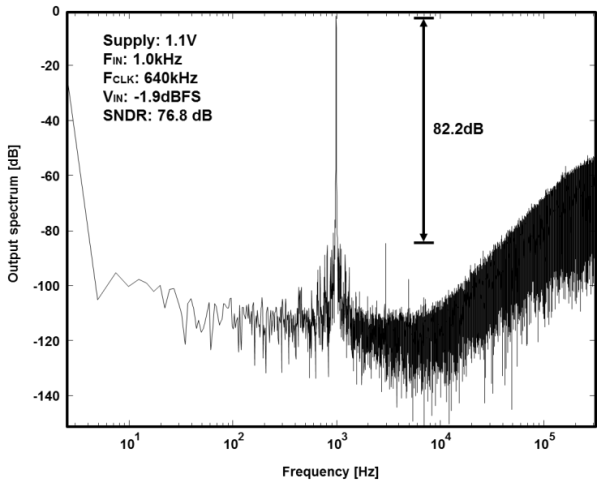

Figure 4. Measured output spectrum

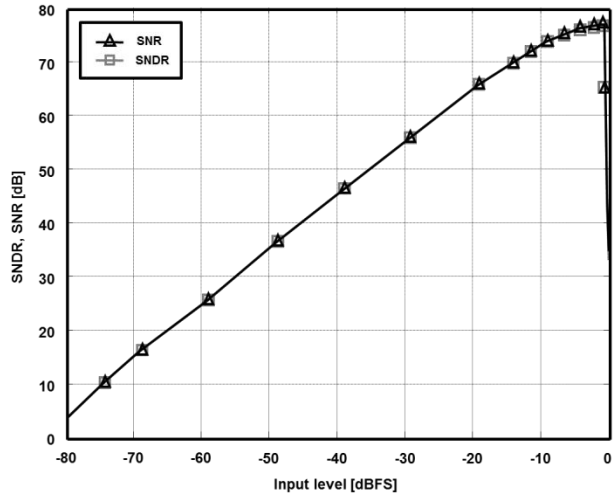

Figure 5. SNR and SNDR versus input level

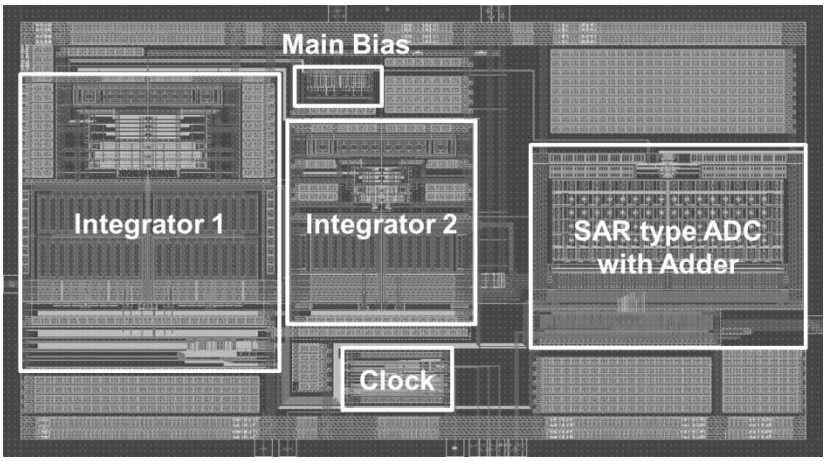

Figure 6. Chip layout

Table 1. Performance summary

Process	45-nm CMOS	Peak SNR	77.8 dB
Power supply	1.1 V	Peak SNDR	76.8 dB
Clock	640 kHz	Peak SFDR	82.2 dB
Signal bandwidth	5 kHz	Power consumption	590 μW (Analog)
OSR	64		260 μW (Digital)
DR	81.8 dB	Chip Area	235 μm^2

5. Conclusion

A 1.1 V 81.8 dB delta-sigma modulator is presented in this paper. The split time integration technique is adopted to implement a multi-bit DAC without using a DEM. In order to minimize power consumption and area, a 4-bit asynchronous SAR ADC is used for quantizer with summing operation. The measurement results of the prototype ADC fabricated in a 45-nm CMOS technology verify the validity of the proposed design technique.

Acknowledgements

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