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FPGA Based Implementation of Gain Control Block for OFDM System

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Abstract

In the OFDM (Orthogonal Frequency Division Multiplexing) system, the fast synchronization is required which in general could be achieved using the preamble located in the header part of the data packet. The modulated and transmitted signal experiences the frequency selective fading due to the multipath channel. As the recent OFDM systems have been applied to the various application areas, the coverage increases which can be translated into the wide range of the signal power variation observed at the receiver side. To obtain the optimum signal level the gain control block at the receiver front-end should be capable of processing wider range of the signal power than the conventional systems. If the signal power is not controlled properly, the overall system performance is expected to be deteriorated due to the quantization errors generated in the process of the analog to digital signal conversion. Therefore it is required to control the received signal power at the optimum level. In this paper, the gain control block is implemented based on the FPGA (Field Programmable Gate Array) hardware. The implemented block adopts multiple gain steps which are optimized by using the statistical characteristics of the quantized signal at the ADC (Analog to Digital Converter) output. The proposed design is shown to provide the enhanced convergence speed and reduced processing time while the hardware complexity is increased marginally compared with the conventional system.

Keywords: *Gain control, quantization noise, loop gain, convergence*

1. Introduction

Demands for wireless internet services continue to increase due to the rapid spreads of mobile information and communication devices and the fast advancement of the network infrastructures. With these emerging trends, the effective use and distribution of the limited radio frequency resource becomes a mandatory consideration for the transmission system design. The wireless local area network (WLAN) which is represented by the IEEE 802.11 standard and also known as the WiFi has been introduced to provide the wireless internet service in the short-range at low cost [1-3]. Although the initial target for this system was to cover the relatively near distance network including the home, the office and the hotspot areas, the application areas are being expanded to the other areas including the outdoor environments. One of the applications for the long distance outdoor transmission is so called Super WiFi which operates in the TV white space band. The TV white space is the idle

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frequency band originally allocated for the TV broadcast. The distance between the transmitter and the receiver is three or four times longer than the conventional coverage of the legacy system. This range could be up to a few kilometers. It is also expected to have a better propagation characteristic especially in the environments with many geographical obstacles [4-5]. This is because the TV white space is located around 700MHz while the normal WiFi operates in the ISM (Industrial Scientific and Medical equipment) band which is either 2.4GHz or 5.0GHz band.

One of the main transmission technologies for the recent high speed communication system is the OFDM scheme which is also adopted for the various types of the WiFi systems. The motivation of these popularity comes from the robustness to ISI (Inter-Symbol Interference) where the longer symbol interval is used utilizing the multiples of narrowband orthogonal sub-channels to transmit the data stream in parallel [6-7]. The OFDM system requires more sophisticated signal processing algorithm compared with the single carrier case to utilize the advantages of the multi-carrier modulation scheme. Some of the unique characteristics to be taken care of include the high PAPR (peak to average power ratio) and the sensitivity to the ICI (Inter-Carrier Interference) [8]. These characteristics come from the superposition of the multiples of narrow band carriers which are orthogonal to each other. The receiver blocks should find the optimum signal level and the offset values of the carrier frequency to avoid the interferences due to the quantization noise and the ICI.

The received signal level varies due to the relative movement of the user devices as well as the multipath propagation. As the coverage of the system extends to longer distances the fluctuation of the signal level as a function of time becomes one of the most important factors affecting the data recovery performance. If the received signal power is not controlled properly at the very first stage of the receiver, the overall system performance is likely to be degraded due to the possible signal distortion and the inaccurate synchronization [13]. The received signal level should fit in the fixed dynamic range associated with the ADC (Analog to Digital Converter) located in the receiver signal path. To reduce the quantization error or equivalently maximize the signal to quantization noise ratio, the input voltage level should be adjusted optimally within the dynamic range of the ADC. In other words the optimum level of signal power should be maintained at the input of the ADC even though the level of incoming signal changes randomly [9-12]. The main mission of the gain control block is to determine the optimum gain for the incoming signal based on the observation signal samples at the output of the ADC.

In the previous research works, the AGC with multiple gain update loops is proposed for the MIMO-OFDM system [15]. In this previous work the existence of saturation over the ADC dynamic range is detected based on four samples for the fast convergence time. Although this scheme can reduce the convergence time over the conventional one, relatively longer processing time is required when the signal power level is quite big which might occur in the long range transmission. In other previous research work the saturation level estimation is performed based on more samples of the preamble part to get faster processing time. The effect of the number of gain loops on the convergence speed is analyzed through the extensive simulation [16]. The brief introduction related to the proposed design method has been presented in [17].

In this paper the design of the AGC with four gain loops is discussed in more detail based on the FPGA hardware platform. The RTL (Register Transfer Logic) level simulation is performed and the designed block is verified on the FPGA device. Hardware complexity is evaluated for the cases with different number of gain loops. The results show that the increase of the hardware complexity is negligible for the higher number of loops while we can achieve faster convergence to the optimum level especially in the case of the high power level of the

received signal. This paper is organized as follows. In the following section the baseline algorithm of AGC with four gain loops is discussed. The parameter configuration method for the hardware design follows. The next section discusses the simulations on the FPGA device level as well as the RTL level. Conclusions are drawn at the end.

2. Gain Control for the OFDM Signal Frame

The convergence rate of the AGC depends on the various parameters associated with the related blocks which include the response rate of the variable gain amplifier and the loop gain. The excessive amounts of saturation at the ADC output could occur due to the non optimum gain of the amplifier possibly due to the signals from the transmitter located at a close distance. In this case the signal power estimation accuracy is degraded and the completion time of the AGC operation is deferred. If the gain control does not reach an optimum gain level and the following signal in the same frame is still in the saturation state, the receiver front-end block might not provide enough accuracy for the remaining data recovery operation. On the other hand if the gain is too low in reference to the dynamic range of the ADC, relatively large quantization noise errors are added to the received signal samples. These phenomena indicate that the estimation of the optimum gain for the input signals are essential part of the receiver front-end which motivates the fast convergent gain loops and the detection mechanism for the degree of saturations.

One of the solutions to handle the wide range of the signal power is to adopt the multiple gain loops. In this type of gain control scheme the loop gain is chosen adaptively depending on the incoming signal power level. With this method the convergence speed could be accelerated with the proper gain selection. In this paper the hardware design method is discussed for the AGC with four different update gain loops which has been proposed to obtain faster convergence time. In our design the ADC resolution is assumed to be 10-bit which does not cause any significant amount of quantization noise in the corresponding operation range assuming the IEEE 802.11a/g signal frame. The parameters for the hardware design are determined based on the thorough performance simulation. To determine the optimum operating power level, the bit-error-rate (BER) performances as well as SQNR are considered. Once the analysis of simulation results for the BER and SQNR performance is carried out, the midpoint of the signal level range is selected which provides the best BER performance.

Another important procedure is the selection of the loop gain based on the degree of the saturation. The more samples are observed, the more accurate gain can be estimated in general. However, more observation sample could cause the processing delay. In other words there are trade-offs between number of samples and the delay. In this scheme 16 samples are used which is equivalent to the one period of the short training sequence in the WiFi system. Also, without loss of generality the detailed design procedure and the simulation results are discussed based on the IEEE 802.11a/g packet. In our design the loop gain is about -38dB for the saturation count of 1 to 13 while -63dB loop gain for the count of 16. As it can be expected, higher loop gain is assigned to the higher degree of saturation. The remaining parameters are obtained based on the analysis of the associated simulation results.

3. Implementation of AGC with Multiple Gain Loops

In this section hardware implementation of the AGC (Automatic Gain Control) block is discussed based on the FPGA hardware device platform. Although the proposed design method could be applied to any wireless data transmission system utilizing the packet based method, the well known 802.11a/g wireless local area network system is assumed for the

detailed discussion of the hardware design procedure [1]. In this implementation a 10-bit signed integer output of the ADC is assumed. The Spartan series FPGA device from Xilinx is used to implement the hardware of the AGC block. The overall system block diagram is shown in Figure 1. The control signal inputs to the AGC include clock, reset for clearing the internal memory of the block and CS (Carrier Sensing) for the information on the existence of the received signal packet. The signal path at the input of the AGC includes the in-phase and the quadrature phase component of the received signal which is real and imaginary parts, respectively. The signal I and Q represent the in-phase and the quadrature phase component, respectively. The variable gain amplifier takes the I or the Q component as an input and generates the signal whose power level is adjusted by the gain determined by the AGC block. Although the amplifier operates in the analog domain in many cases, our block diagram represents the digital equivalent circuit. Based on this equivalent circuit, the entire simulation can be done with the versatile digital hardware description language. Once the packet is detected through the carrier sensing block, the AGC starts its operation. The gain control consists of two parts. First part is the estimation of the input signal level and the second is to control the gain of the amplifier. This procedure is repeated until the incoming signal level is settled down within the acceptable range of the reference signal power level. The reset signal is activated when the gain control operation is finished for the corresponding packet to get ready for the next signal packet.

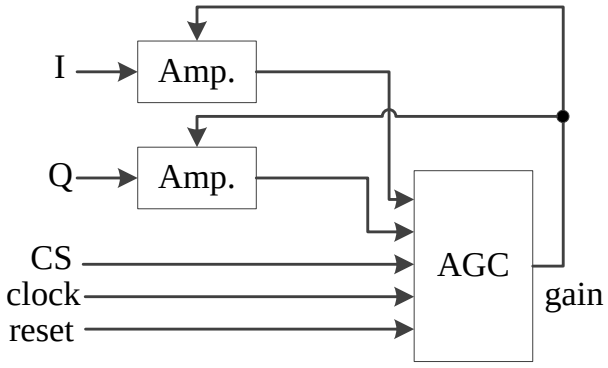

Figure 1. Block diagram of digital equivalent system for gain control

The major part of the hardware implementation of the AGC corresponds to the design of the finite state machine. This state machine is meant to describe the logical operation of the entire gain control loop. The overall state diagram is shown in Figure 2. This figure describes the detailed state transition of the block depending on the incoming signal level. For each state a number from 0 to 10 is assigned. The state transition occurs at the positive edge of the clock signal. In this system, state machine changes its state based on the values of 'state_cnt' and 'sat_cnt'. These two variables correspond to the number of processed samples and the number of saturated samples, respectively. The state change occurs when the specific condition is satisfied for the corresponding transition. For example the state machine changes its state from state 1 (MSR&EST) to 2 (LOG) when sample count variable 'state_cnt' equals to fifteen. Another example is for the saturation count variable 'sat_cnt'. This variable is used as a condition for the transition from the state 3 (COMPARE) to 4~8 (STx). The overall operation is described as follows. The receiver waits for the incoming signal at the state 0 (IDLE) when it is ready for the next signal packet. If the reset signal is equal to zero which is equivalent to the active reset, all the states and variables are initialized. If the reset signal is

equal to one, the AGC block continues to wait for the incoming signal. The clock signal is used after negative edge of the reset signal. In this hardware implementation it is assumed that the system operates in synchronization with the clock signal.

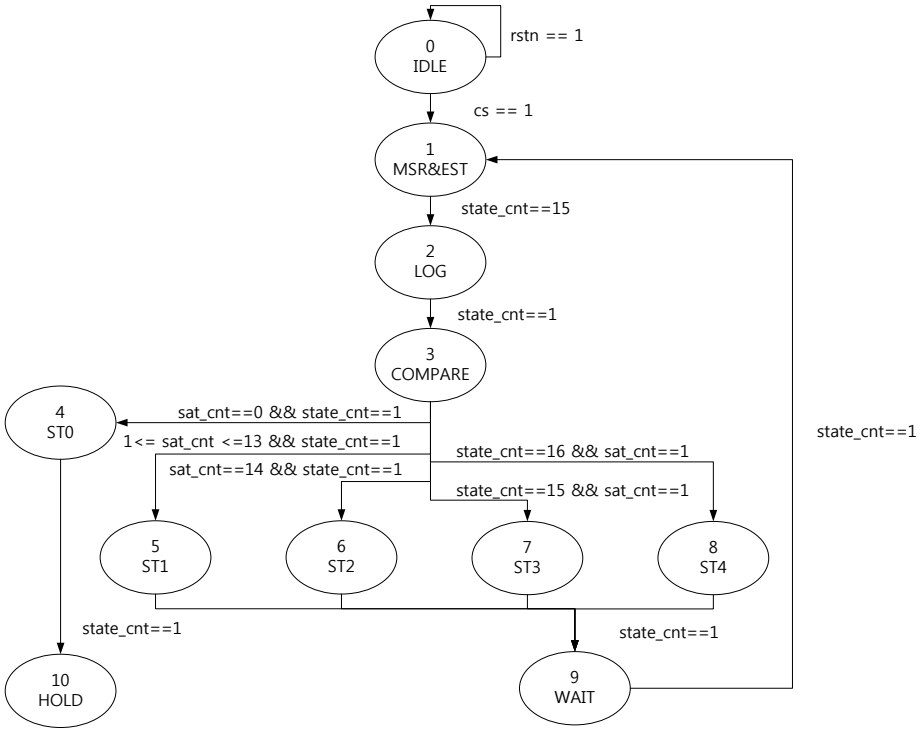

Figure 2. State diagram for the AGC with multiple gain loops

The carrier sensing block determines whether there exists a transmitted signal at the input of the receiver. Once the carrier sensing is completed and the signal is detected, the state machine changes its state from 0 (IDLE) to 1 (MSRnEST) where the operation for the signal power estimation is performed based on the direct measurement of the signal amplitude and based on the saturation number count. As an indirect estimation of the signal power, 16 samples are being monitored for the saturation statistics which corresponds to one period of short preamble. The state 1 (MSRnEST) is followed by the state 2 (LOG). In this state, the measured and estimated power level in linear scale is converted into a logarithmic dB scale.

The state 3 (COMPARE) determines the next transition state according to the number of saturation counts obtained from the previous state. The state 4 (ST0) is the target state when no saturation sample is observed. Depending on the non-zero number of saturation samples within the observation period (16 samples in our implementation), one of the states from state 5 to 8 is selected for the next target state. The criteria for selecting the state are determined by the analysis of the relationship between the saturation counts and the possible ranges of the signal power. In this design the states with higher number assumes higher signal power than the lower numbered state. For example the state 8 is for the case all the samples in the observation period are saturated while the state 4 for fewer samples are saturated. In cases one or more saturation samples are observed the actual power is likely to be bigger than the optimum reference power level. In this case the gain control operation is required to reduce the power level. According to the number counts of saturation samples, the received power level can be adjusted using the corresponding loop gain. In case of the state 4 (ST0) state, no

saturation sample is counted and power level could be higher or lower than reference power level. Therefore the input power level can be adjusted by using the difference between the measured and the reference power level.

After the control gain is delivered to the amplifier at the state 5 to 8 (ST1 to ST4), the transition occurs into the state 9 (WAIT). At this state the control block waits for the amplifier to settle on the new updated gain. The next step is to go back to the state 1 (MSRnEST) and to repeat the same procedure until the saturation count becomes zero. The state 4 (ST0) is the last stage where the final gain adjustment is carried out. Once the final gain control is done the state moves to the final stage 10 (HOLD). From that time instance the AGC block waits for the receiver to complete the data detection processing for the corresponding packet.

For the implementation of the signal power measurement sub-block which is the essential operation required at the state 1 (MSRnEST), the absolute values of the in-phase and quadrature component samples are used to approximate the actual signal power. In our case the 2'complement operation is used to obtain the absolute value of the signed integer samples. In the state 1 (MSRnEST) the state can be changed into the state 2 (LOG) if the sample number counts reaches 15. In the state 2 the signal power is transformed into the log scale. At the state 3 (COMPARE) the power of the incoming signal is compared with the reference power level. The control gain is determined by the power difference between the incoming signal and the reference in logarithmic scale. This difference is the final gain adjustment when there is no saturation samples monitored. As mentioned above the multiple iterations with possibly different loop gain are required to handle the non-zero saturation counts.

4. Simulation

In this section the simulation results and the hardware level experiments are discussed. To verify the proper functional operation of the implemented AGC with four different gain loops, the RTL level simulation is performed first. The design is carried out using the Verilog HDL (Hardware Description Language). The resulting hardware design is compiled to fit into the FPGA hardware device. In our design Spartan 3E series FPGA device from Xilinx is used to test the functional operation at the physical hardware circuit level. With the chip design analysis tool the actual operation of the digital logic circuit can be also monitored and confirmed.

The results for the RTL level simulation and the FPGA level experiment are shown in Figure 3 and Figure 4, respectively. This test assumes a relatively lower signal power level (70dB). In this experiment one step unit is assumed to be 1ns which is equivalent to the propagation delay of the device. The elementary step for the simulation is set to 1ps. As shown in the resulting waveform the state 1 (MSRnEST) is shown twice which means that two times of gain adjustment is performed to obtain the optimum signal power level. It is also confirmed from Figure 3 and Figure 4 that the RTL simulation results and the FPGA level test result coincide with each other.

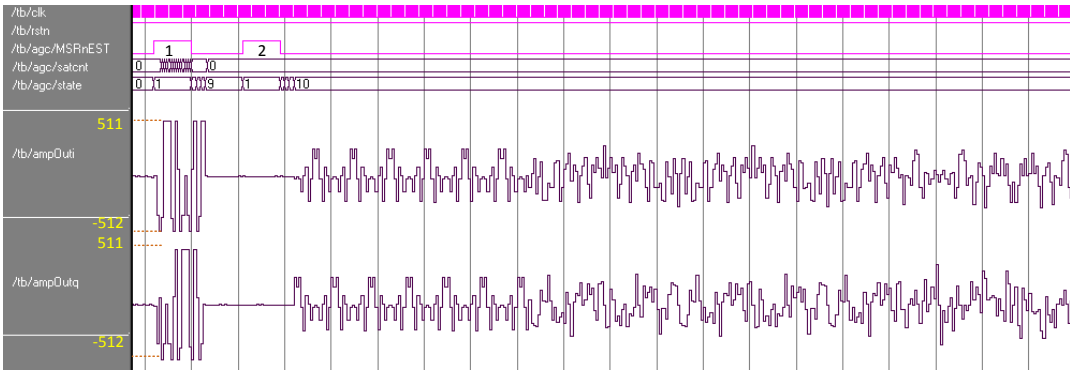

Figure 3. Controlled waveforms obtained with RTL simulation (70dB input signal)

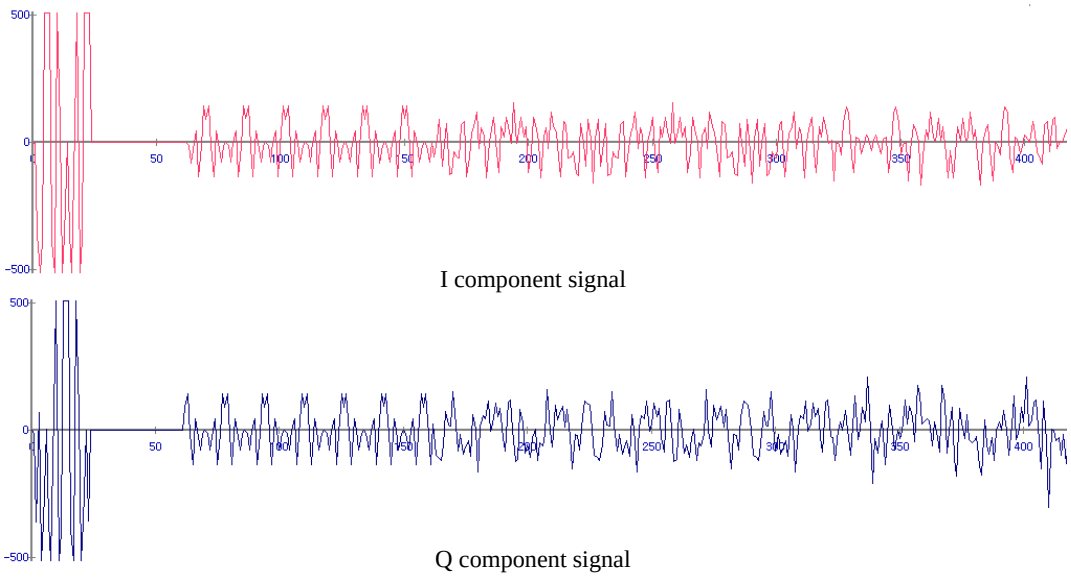

Figure 4. Controlled waveforms obtained with FPGA level experiment (70dB input)

Results for the input power level of 140dB are summarized in Figure 5 and Figure 6. It can be observed that the state 1 (MSRnEST) occurs three times which is equivalent to the three times of gain adjustment before the AGC completes its mission. It is also confirmed that the simulation and the hardware level results have coincided with each other.

To assess the hardware complexity as a function of the number of loops in the AGC, the hardware resources of the FPGA occupied by the designed circuit are compared. As shown in Table 1, the effect of the number of loops on the required resource is negligible. In the same table the major hardware resources in the FPGA are listed with the quantitative number required for the implementation of the AGCs with multiple gain loops. This confirms that the number of gain loop is not a major factor of the hardware complexity increase while they could provide the performance improvements in terms of the convergence speed.

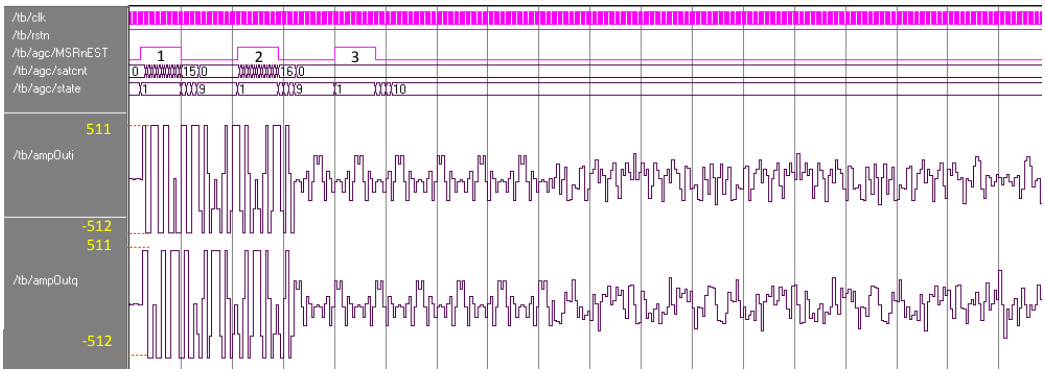

Figure 5. Controlled waveforms obtained with RTL simulation (140dB input signal)

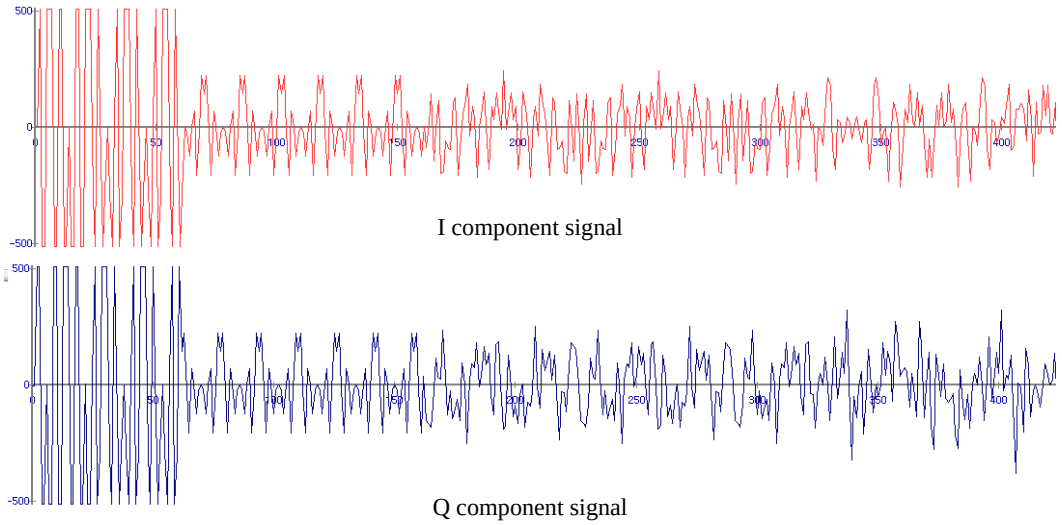

Figure 6. Controlled waveforms obtained with FPGA level experiment (140dB input)

Table 1. Comparison of hardware complexity

	2 –loops AGC	3-loops AGC	4-loops AGC
Flip Flops	87	88	89
LUTs	749	753	768
Logics	749	753	789

5. Conclusion

The amplitude of the transmitted signals through the wireless channel shows the time varying characteristics and the rate of change depends on the geographical features of the operating area of interest. At the receiver the power level control of the received signal should be completed in order not to affect the performance of the remaining blocks. This is a mandatory requirement for the packet based transmission system. In this paper hardware implementation of the gain control block is discussed which has the multiple gain loops. This AGC block includes a set of varying gains to adapt itself to the different signal power ranges.

It also includes the power estimation blocks based on the number of saturation samples within an observation period. The advantage of the multiple gain loops includes the faster convergence especially for the relatively high power received signals. Also achieved is the negligible hardware complexity increase with the improved performance. The design results are verified on the commercially available FPGA device after the RTL level simulation is completed. The functionality of the designed AGC is checked on the physical hardware device using the real time chip design analysis tool. The quantitative hardware complexity in terms of the FPGA resource usage is also discussed. Results show that the effect of the multiple loops on the complexity is negligible.

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