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Design of Power Dividers using Defected Microstrip Structure and an Analytically Calculated Characteristic Line Impedance

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Abstract

In this work, a defected microstrip structure (DMS), methods to calculate the new characteristic impedance of DMS line, and, as an application example, a design of microwave wilkinson power dividers using DMS pattern are described. DMS patterns are inserted for the desirable effects of periodic structure such as size-reduction and increased line width for high characteristic impedance. In order to calculate the proper characteristic impedance of DMS microstrip line, the quarter-wavelength transformer model method and an analytic calculation method are adopted. As an example, the DMS microstrip line with 70.7Ω characteristic impedance is designed, calculated and inserted into the wilkinson power divider. The size of designed power divider with DMS patterns is only 82% of a reference power divider composed of normal microstrip lines, while the circuit performances are very well preserved even after the size-reduction.

Keywords: *defected microstrip structure, DMS, power dividers*

1. Introduction

Recently, perturbation structures such as photonic band gap (PBG) and defected ground structure (DGS) for microstrip lines have been widely studied as planar periodic structures, which modify the characteristic impedance and dimensions of microstrip lines. Due to the perturbation structures, equivalent circuit elements per unit length, *i.e.*, inductance and capacitance, of microstrip line increase, and related physical phenomenon occurs. So the characteristic impedance of microstrip line increases for a given line width and slow-wave effect is observed. Those properties might be applied to high frequency circuits for size-reduction or performances improvement [1-6].

However, in the case of PBG, it is not easy to define a unit section and to extract the equivalent circuit elements of PBG patterns because a lot of periodic patterns are required on the ground plane. This drawback has prevented ones from applying PBG patterns to microwave and radio frequency (RF) circuits. To the contrary, there are some superior advantages in DGS compared to PBG such as; 1) less DGS elements are required for the similar effects, 2) it is easy to define a unit element and to model the equivalent circuit, and 3) DGS patterns have a great potential of applicability. However, DGS patterns should be etched off from the ground plane of microstrip lines, and this has been known as a critical disadvantage of DGS so far [4-7].

Defected microstrip structure (DMS) has been proposed recently in order to solve the drawback of DGS while making use of the advantages of DGS [8,9]. In other words, the microstrip lines with DMS patterns have the same pros of previous PBG and DGS, and do not

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have the cons mentioned above because perturbation patterns are realized not on the bottom side ground plane, but in the mid of signal line on the upper side of microstrip lines.

So it is necessary to study the applications of DMS to microwave and RF circuits because of the representative drawback of DGS can be eliminated by replacing it with DMS. In this study, a high frequency wilkinson power divider is designed, fabricated and measured to present an example of application of DMS. The designed power divider has a smaller size compared to the normal one due to the equivalent additional inductance and capacitance of the inserted DMS pattern, although the performances of the size-reduced power divider are quite comparable to the original ones.

In order to design the power divider with DMS pattern, the appropriate characteristic impedance of DMS microstrip line should be provided, because it is required to complete the design. In this work, an analytic calculation method is discussed and the obtained line impedance is applied to design the power divider.

2. DMS Microstrip Line and the Quarter-wave Transformer Method

Fig.1 shows the pattern of defected microstrip structure (DMS) adopted in this work. This DMS pattern is realized on the signal plane of mcirostrip line on the upper plane, so the ground plane is not touched. Considering the previous structures of PBG and DGS for microstrip lines, the DMS pattern is very comparative because it is a critical drawback of PBG and DGS to pattern them on the bottom ground plane.

This bottom patterning leads to two representative negative effects. The first one is the signal leakage problem. Because the PBG and DGS patterns are realized in the mid of bottom ground plane by etching them off, it is easily predicted for the signal to leak through the etched patterns on the ground plane. The second problem occurs when the circuits with PBG and DGS patterns are inserted into metallic housing. If they are placed on the package, the bottom ground plane with PBG and DGS patterns must contact the metallic surface. In most cases, the metallic housing acts as the bulky ground. So the advantages of PBG and DGS disappear in conductive housing. However in Figure 1, the DMS pattern is inserted on the upper microstrip line.

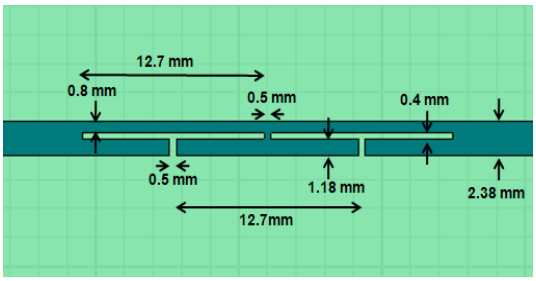


Figure 1. Microstrip line with defected microstrip structure pattern in this work

The slot-like DMS pattern in Figure 1 has additional equivalent inductive and capacitive elements. The coupling in slots results in the capacitance, and the outer length of slots inductance. It is noted that the adding of inductance is dominant over the increase of capacitance because the length of outer slot-boundary is much longer than that of coupling section.

The added equivalent inductance and capacitance caused by the DMS pattern make the electrical length of DMS microstrip line longer than that of normal microstrip line without DMS for a given physical length. This means it is possible to reduce the

physical length of microstrip line for the same electrical length by inserting DMS pattern. This is the principle in reducing the size of circuit by inserting any periodic or perturbation structure into normal transmission lines [10].

It is well known that the characteristic impedance (Z_c) of transmission lines is determined by (1)

$$Z_c = \left(\frac{L}{C}\right) \tag{1}$$

where L and C are the equivalent inductance and capacitance per unit length of transmission lines [11-13]. Then the characteristic impedance of DMS line can be expressed by (2).

$$Z_{c,DMS} = \left(\frac{L+\Delta L}{C+\Delta C}\right) \tag{2}$$

Because the added inductance (ΔL) is larger than added capacitance (ΔC), it is true that $Z_{c.DMS} > Z_{c,normal}$, where $Z_{c.DMS}$ and $Z_{c,normal}$ are the characteristic impedances of DMS and normal microstrip lines, respectively. So, if the line impedance is required to be preserved even after DMS patterns have been inserted, the line width should be increased. This is one of very important advantages in practical applications.

One simple example may be presented here with a dielectric substrate of which dielectric constant (ε_r) and thickness (H) are 2.2 and 31mils, respectively. This substrate has been selected to design the DMS microstrip line shown in Figure 1. Figure 2 represents the predicted S-parameters which have been simulated on Ansys HFSS (high frequency structure simulator). The line width 2.38mm corresponds to the width of the normal 50Ω microstrip line. However the characteristic impedance of the DMS microstrip line in Fig. 1 is no more 50Ω because the S11 in Figure 2 is not perfect within the passband.

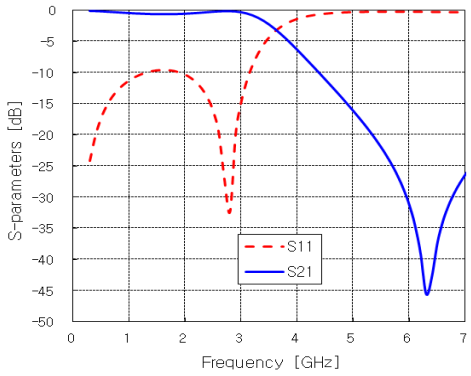


Figure 2. Simulated S-parameters of the DMS microstrip line

The characteristic impedance of DMS line ($Z_{c.DMS}$) can be found using the quarter-wave transformer method [14]. Figure 3 and Eqs. (3)-(5) are useful for calculating $Z_{c.DMS}$. Figure 3 shows the transmission line model of the DMS line with the length of quarter-wave at the center frequency (F_o). When θ is π/2 or a quarter-wave length at F_o, the magnitude of reflection coefficient (|Γ|) is maximum, so the relation between |Γ| and S_{11} in (3) is effective. Once |Γ| is known, Z_{in} is calculated by (4). Finally, $Z_{c.DMS}$ is calculated from (5). Here, Z_o is the reference impedance or termination impedance.

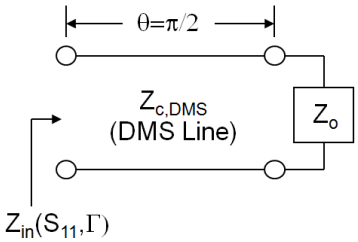


Figure 3. Equivalent circuit model to determine the characteristic impedance of the DMS line

$$S_{11}[dB] = 20\log|\Gamma| \tag{3}$$

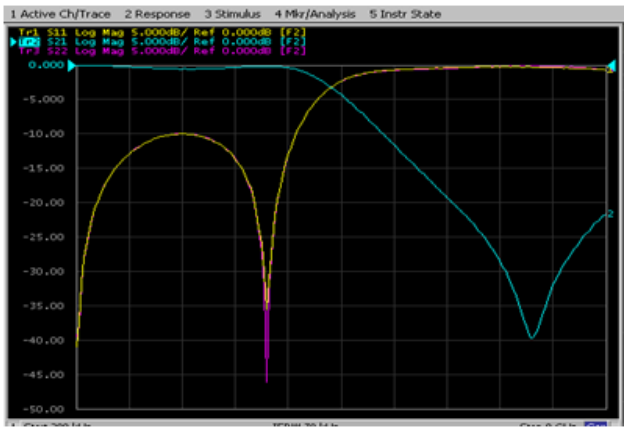
$$Z_{in} = Z_o \frac{1+|\Gamma|}{1-|\Gamma|} \tag{4}$$

$$Z_{c,DMS} = \sqrt{Z_{in} Z_o} = Z_o \sqrt{\frac{1+|\Gamma|}{1-|\Gamma|}} \tag{5}$$

Since the simulated S11 is -9.5dB in Fig. 2, the corresponding line impedance can be calculated. It turns to be around 70Ω from (1)-(3), and this is a meaningful value because wilkinson power dividers require transmission line elements with 70.7Ω of line impedance [13]. In addition, it is noted that the width of 70.7Ω normal microstrip line is only 1.37mm, while that is 2.38mm in DMS line as shown in Figure 1.

The 70.7Ω□DMS line has been fabricated, and its characteristic impedance was verified through the S-parameter measurement. Figure 4(a) and (b) show the photograph of the fabricated DMS microstrip line and measured S-parameters. The measurement has been performed using an Agilent E5071B vector network analyzer. The measured S11 is exactly the same as the predicted one in Figure 2. Therefore it can be said that the design of 70.7Ω□DMS line with 2.38mm of line width has been verified.

(a)



(b)

Figure 4. Fabricated 70□ DMS line and measured S-parameters (a)photo (b)S-parameters

3. Calculation of Characteristic Impedance of DMS Line using an Analytic Method

In order to design the power divider with DMS pattern, the appropriate characteristic impedance of DMS microstrip line should be provided, because it is required to complete the design. In this work, an analytic calculation method is discussed and the obtained characteristic impedance (Z_c) is applied to design the power divider.

Even though the above method can be used to find the new Z_c of DMS line, it is a drawback for one to apply the method only at the center frequency where the electrical length (θ) is $\lambda/4$ or $\pi/2$. So the calculated line impedance is valid only at the center frequency. However, characteristic impedance of transmission lines is a very important factor in practical applications at all required frequency band, because all of high frequency circuits should have the targeted performances within the designated band, and this is guaranteed by adopting the proper transmission line elements. Therefore when DMS patterns are combined to the normal microstrip line, it is essential to calculate the Z_c as exact as possible for successful application to high frequency circuits and systems.

Figure 5 shows the block diagram of a DMS line, of which characteristic impedance, electrical length, phase constant, and physical length are Z_c, θ, β, and l, respectively [15]. According to the basic transmission line theories, the input impedance (Z_{in}) is expressed as (6) and (7). S_{11} which corresponds to the input coefficient of the DMS line is shown in eq. (8), because Z_{in} plays a role of load when the input signal is injected from port1.

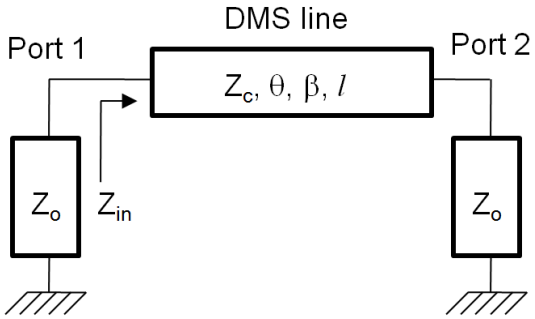


Figure 5. Block diagram for finding the characteristic impedance of DMS microstrip line

$$Z_{in} = Z_c \frac{Z_o + jZ_c \tan\theta}{Z_c + jZ_o \tan\theta} \tag{6}$$

$$z_{in} = z_c \frac{1 + jz_c \tan\theta}{z_c + j\tan\theta} \tag{7}$$

$$S_{11} = \frac{z_{in} - 1}{z_{in} + 1} = rs_{11} + jis_{11} \tag{8}$$

where $z_{in}=Z_{in}/Z_o$ and $z_c=Z_c/Z_o$, and rs_{11} and is_{11} are the real and imaginary part of the S_{11}, respectively.

If (7) is inserted into (8), then (9) is obtained. It is noted that the real and imaginary parts should be zero if (9) is valid. So (10) and (11) are produced with the quadratic equation form of "$ax^2+bx+c=0$" for z_c.

$$2z_c rs_{11} - \left(z_c^2+1\right)\tan\theta\, is_{11} + j\left[2z_c is_{11} + \left(z_c^2+1\right)\tan\theta\, rs_{11} - \left(z_c^2-1\right)\tan\theta\right] = 0 \quad (9)$$

$$z_c^2 - \frac{2rs_{11}}{\tan\theta\, is_{11}} z_c + 1 = 0 \quad (10)$$

$$z_c^2 + \frac{2is_{11}}{\tan\theta\left(rs_{11}-1\right)} z_c - \frac{1+rs_{11}}{1-rs_{11}} = 0 \quad (11)$$

Because Z_c is the characteristic impedance of the microstrip line, so it must be a real value. Then (10) can be ignored in this study because, in some cases, we may get an imaginary determinant value from (10) depending on rs_{11}, is_{11}, and tanθ.

By the way, in (11), the magnitude of rs_{11} is always less than 1 because transmission lines are passive elements. Then the third term of (11), which corresponds to "c" of the quadratic equation, is always negative. Hence, determinant "D" is always positive, and two real solutions of (11) exist. Then the optimum solution is one of them, and the other one will turn out to be improper.

The analytic method has been applied to the S-parameters shown in Figure 4 to find the more accurate Z_c of the DMS line. The calculated impedances at various frequencies are around 70.7Ω at 1GHz as depicted in Figure 6. It is noted that, in the above quarter-wave transformer method, the calculated line impedance is reliable only at around the center frequency where the electrical length is λ/4. However, in Figure 6, the calculated line impedances using the analytic method are less frequency-dependent. This means the obtained impedances are more reliable over broad band containing center frequency. In Figure 6, one can find the Z_c of the DMS line of Figure 4 (a) at other frequencies.

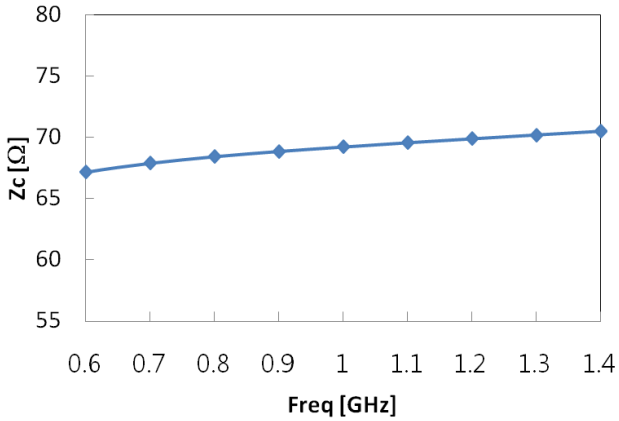
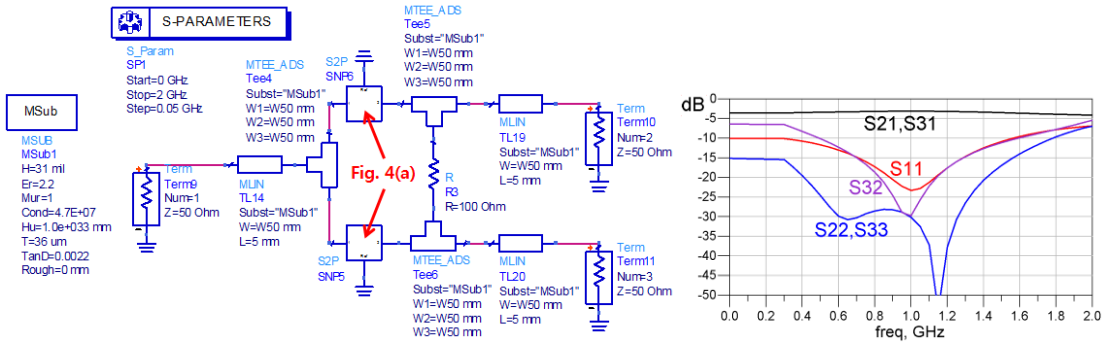


Figure 6. Calculated characteristic impedance of DMS line in Figure 4 using the analytic method

4. Design of the Size-reduced Wilkinson Power Divider using DMS Line

The DMS line designed above has been applied to design a size-reduced wilkinson power divider. Agilent Advanced Design System (ADS) has been adopted in order to simulate the circuit level design and predict the primitive performances of the divider. Figure 7(a) shows

the schematic design of the divider in which the HFSS simulation results of the DMS line are included, and the simulated S-parameters.



(a) (b)

Figure 7. Schematic design of the size-reduced power divider and simulated S-parameters (a)schematic design (b)S--parameters of the power divider using ADS

Two 70Ω DMS microstrip lines in Figure 4(a) are inserted to consist of the wilkinson divider. Figure 7(b) shows the predicted S-parameters of the designed divider. Excellent performances in power dividing, matching, and isolation are observed.

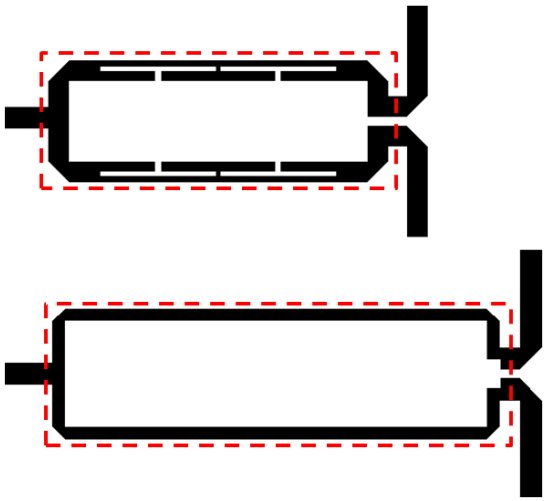
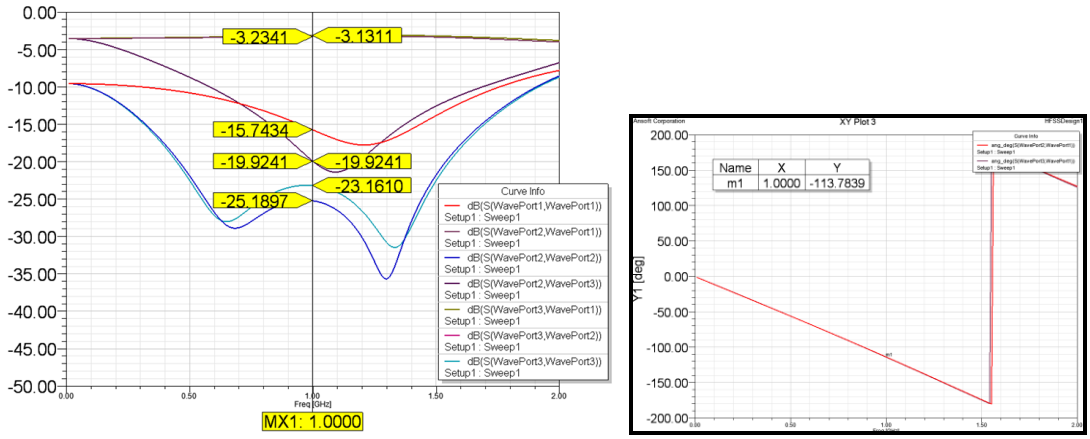


Figure 8. Layout of power dividers using DMS microstrip line(upper) and normal one(lower)

Figure 8 shows the layouts of size-reduced wilkinson power divider using DMS micorstrip line. A normal design of power divider is also presented in Figure 8 for comparison of size. In order to present the effect of DMS in size-reduction, 1GHz has been selected as the design frequency. As has been described already, the width of DMS line is fixed to 2.38mm in the DMS divider whether it is 50 Ω or 70.7 Ω line. The dimensions of DMS in the size-reduced divider are the same as those in Figure 1.

It is clear to describe the effect of DMS pattern by comparing two dividers in Figure 8. Eliminating the port feeding lines with 50 Ω, one can compare the pure divider area

designated by dotted boxes. Those are 534mm^2 and 654.7 mm^2 for the size-reduced divider and normal one. The size of DMS divider is only 82% of normal one. The size-reduction is caused by the slow-wave effect due to the added equivalent circuit element of the DMS patterns.



(a) (b)

Figure 9. Electromagnetically simulated S-parameters of the DMS power divider using HFSS (a)S-parameters (b)phase difference

Figure 9(a) shows the electromagnetically simulated S-parameters of the DMS power divider using HFSS. All performances required for power dividers such as power dividing ratio(S21, S31), matching at ports(S11, S22, S33), and isolation between output ports(S32) are excellent. In addition, Figure 9(b) shows the phase difference between two output ports is almost zero, which is close to an ideal case.

5. Fabrication and Measurement

The DMS power divider has been fabricated practically and is illustrated in Figure 10. The 70.7 Ω DMS line in Figure 4(a) has been adopted in the final layout. The substrate with the dielectric constant of 2.2 and thickness of 31mils has been selected for the design and fabrication.

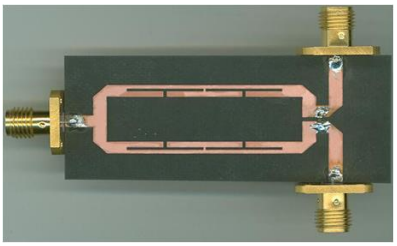


Figure 10. Fabricated power divider using DMS

Figure 11 presents the measured S-parameters of the fabricated DMS divider. The input power has been equally divided and delivered to output ports. The measured S21 and S31 are -3.07dB and -3.08dB, respectively, so the insertion loss is less than 0.1dB. The matching (S11, S22, and S33) and isolation performance (S32) are less than -20dB, which means very good performances. It is observed that the measured S-parameters

are in excellent agreement with the predicted ones. Therefore it can be said that the design of size-reduced wilkinson power divider using DMS has been completed successfully.

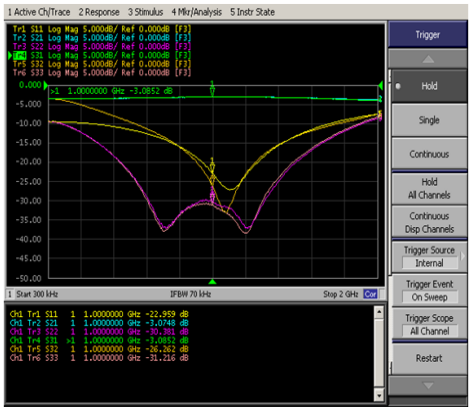


Figure 11. Measured S-parameters of the fabricated DMS power divider

6. Conclusion

A defected microstrip structure and two methods to find the characteristic impedance of microstrip line with DMS have been discussed. Due to the additional equivalent inductance of DMS, a slow-wave effect arises and the characteristic impedance of DMS line increases. So the line width of DMS line should be broader than before DMS-insertion for the characteristic impedance to be the same.

The first calculation method to find the characteristic impedance of DMS line adopts $\lambda/4$ transformer theories, and reliable at the center frequency. The other method uses an analytic approach utilizing the S-parameters of DMS line, reflection coefficient, and input impedance of DMS line. Unlikely to the first way, frequency-insensitive characteristic impedance values are obtained over broad frequency band rather than only at the center frequency.

Finally, a size-reduced wilkinson power divider has been designed and fabricated successfully using the DMS line. The characteristic impedance of DMS line has been calculated by two methods, and turned out to be around 70.7Ω, which is essential value for wilkinson dividers. The measured performances of the divider are exactly the same as the simulated S-parameters. The size of the fabricated DMS divider is only 82% of the normal one while the performances have been well preserved. There was no leakage or ground contact problem in the designed DMS divider, and also no performances degradation, either. The insertion loss at two output ports was order of 0.1dB, which is so small value, and all matching and isolation performances were excellent. It is expected that DMS pattern has a great potential for further application to microwave circuits without the well-known drawbacks of PBG and DGS.

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