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Simulink Model Based Design and FPGA Implementation of Multi-Channel DTV Transmitter

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Abstract

This paper presents DTV transmitter design based on the SW/HW hybrid architecture. Parts of the DTV transmission algorithm with less computational complexity are processed by the SW module in PC whereas computationally intensive parts are processed by the HW module in FPGA. The two parts are interconnected by the high speed serial link. To provide the multi-channel DTV signal, we design an architecture where several DTV waveforms are generated simultaneously and combined in the digital domain. We propose a simulink based communication system design and verification methodology. This method reduces the design and verification time of the prototype system significantly and reduces the RTL coding and verification burden.

Keywords*: DTV transmitter, DVB-T, Simulink, FPGA, Multi-channel*

1. Introduction

Recently new DTV technologies have been developed to improve the mobile reception performance and also to provide high data throughput, including standards such as an ATSC 8VSB/MH [1, 2] or DVB-T/T2 [3]. Furthermore, sophisticated transmission technology is being developed to make it feasible to enjoy the ultra high definition (UHDTV) theater-class picture quality at home. To consider these various DTV transmission technologies, we need a flexible architecture for the DTV transmitter/receiver design.

Most of the high-end DTV receivers recently developed have channel browsing capability where several channel signals are displayed on a single screen to aid the user's channel choice. To test such DTV receivers, we can stack up several single channel DTV transmitters to generate multi-channel signal and combine them in the analog domain. However, it is not only bulky but also an expensive solution. To design a compact transmitter with flexible system architecture, we propose a SW/HW hybrid multi-channel DTV transmitter or signal generator. To reduce the system complexity, logic intensive signal processing blocks such as the channel encoder and interleaver are implemented in PC or DSP by the SW module. And computationally intensive parts such as the waveform shaping, modulation and multi-channel combining blocks are implemented in FPGA by the HW module. These two modules are interconnected by the high speed serial link.

To generate multi-channel DTV signal in the digital domain, we increase the sampling clock frequency to reserve enough space in the frequency domain for the multi-channel combining. Several interpolation filter architectures such as the multi-stage low-pass filter [4], Farrow structure filter [5, 6] or cascaded integrator and comb (CIC) filter

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[7] can be applied for this purpose. To reduce the hardware complexity we adopt the multiplier-less CIC filter structure in this paper. After the interpolation filtering, the system up-converts each baseband signal to the consecutive frequency. We use the simple waveguide quadrature digital oscillator [8] instead of the bulky NCO or CORDIC processor to minimize the system complexity. Finally the proposed system combines each channel signal altogether to compose the multi-channel DTV signal. The resulting output signal is D/A converted and then up-converted to the RF signal using the analog subsystem.

In this paper, we propose the Matlab simulink model based system design methodology to ease the RTL coding and reduce the system development/verification time. We first design a floating point Matlab simulator for the performance verification and system parameter optimization. Next we replace the floating point simulink block with fixed point Xilinx system generation block and generate the net list automatically without RTL coding. Finally we synthesize the circuit in FPGA with Xilinx ISE design suite. This methodology reduces the development and verification time of the proposed system significantly.

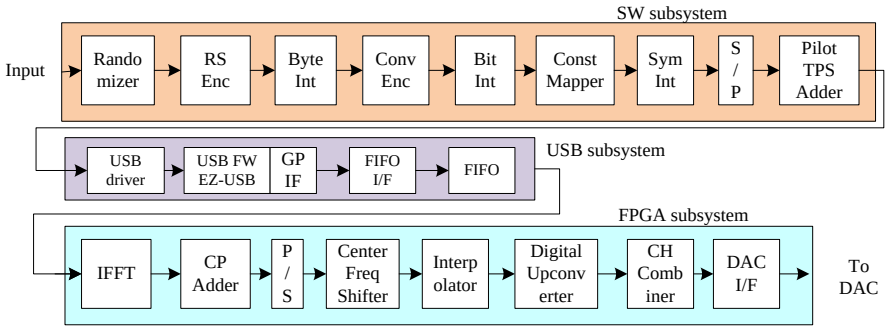

Figure 1. DVB-T transmission system block diagram

2. System Description

Figure 1 shows the system block diagram of the DVB-T transmission system. After the channel encoding which is composed of Reed-Solomon (RS) and convolutional code, the system interleaves the coded bit stream then maps those interleaved bits to the constellation points. Constellation points are interleaved again by the symbol interleaver then pilot and TPS signals are inserted in the pre-defined subcarrier locations. The algorithm blocks from the channel encoding to the pilot and TPS adding are processed by the SW subsystem in PC since those processing blocks require logic intensive operations whereas the computational complexity is not high. The data processed by the SW module is transferred to the FPGA HW subsystem via the high speed serial link (USB 2.0) connection.

FPGA HW subsystem applies the IFFT transform to the data stream transferred by the high speed serial link to convert the frequency domain signals to the time domain ones. After that the system inserts cyclic prefix (CP) then serializes the signal to generate the OFDM signal. Center frequency of the IFFT output signals are shifted to DC to aid the subsequent interpolation filter processing. Then, CIC or Farrow structure based interpolation filter is applied to increase the sampling frequency. The purpose of this interpolation is two-fold: to aid the design of the LPF after the DAC due to increased cut-off frequency and also to reserve the spaces in the frequency domain for the multi-channel combining in the digital domain.

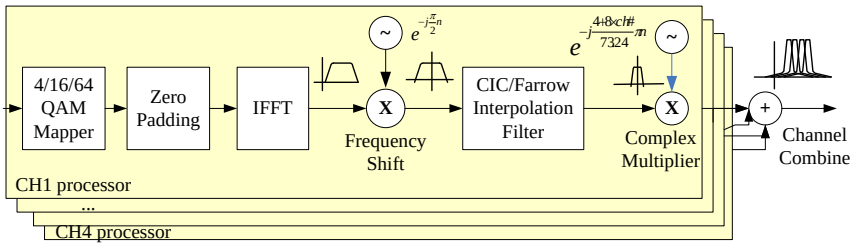

Figure 2. FPGA HW subsystem block diagram

More detailed block diagram of the FPGA HW subsystem is shown in Figure 2. First, the data processed by the DVB-T SW module are mapped to the QPSK or 16/64 QAM constellation points with pilot/TPS signal boosting considered. Then, we pad zeros after the IFFT input data block to increase the sampling rate by two. After that we shift the frequency of the IFFT output signal to move the center frequency to DC for the purpose of helping the interpolation process. Then the system increases the sampling rate by four to reserve space in the frequency domain for the multi-channel combining of each single-channel signal in the digital domain. Finally the processor up-converts each single-channel signal to the low IF (intermediate frequency) band by multiplying it with the digital quadrature oscillator output signal, then combines those signals in the digital domain.

Figure 3 shows the operations of the FPGA HW processor in the frequency domain assuming that four channel signals are combined in the digital domain. The frequency spectrum after the zero-padding and IFFT processing is shown in (a). The system moves the center frequency of the output signal as shown in (b) and then apply the CIC or Farrow interpolation filtering to increase the sampling rate and remove the image signals (marked in dotted line in (c)). Then the system up-converts the base-band signals to the low IF signal by multiplying it with the carrier signal generated by the waveguide quadrature digital oscillator. Finally those signals are added together in the digital domain to form the multi-channel low IF (intermediate frequency) signal. Since each signal occupies 8 MHz TV channel, the total bandwidth of the combined signal in the figure is 32 MHz, with the sampling frequency of eight times the DVB-T symbol rate (73.14 MHz).

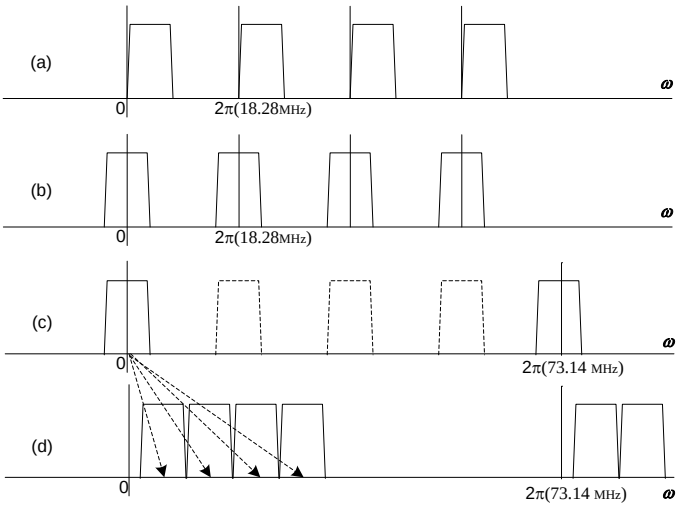

Figure 3. Operation of the HW susbsystem in the frequency domain

The combined signal is then D/A converted in analog subsystem. Then the signal passes through an analog LC band-pass filter and is up-converted to the target RF frequency. A frequency synthesizer with embedded VCO and PLL circuit is used for this operation. Finally the signal is amplified by variable gain high power amplifier.

3. Matlab Simulink Based System Design Methodology

To implement the multi-channel DTV transmitter, we propose a system level design methodology where we use the Matlab simulink with Xilinx block set tool box. The design process is described in Figure 4. First we model the total transmitter system with Matlab script file and verify the system. Then we convert the double precision simulator to a fixed point simulator and trade-off between the performance loss due to the quantization effect and the hardware complexity. Next, we replace the fixed point simulink model block with Xilinx block to generate the net-list to be implemented in FPGA. By the design flow, we reduce the RTL coding and verification burden significantly since the EDIF net-list and the wrapper codes are generated automatically by the Matlab simulink without any RTL coding. We only need to implement the top level interface to integrate the wrapper code and some small logic blocks for the USB 2.0 and NAND flash memory interface. For the verification of the DVB-T transmitter, we also implemented the double precision DVB-T receiver with a sharp band-pass filter to select one of the 4 transmitted channel signal in Figure 3. To avoid the performance loss due to the receiver processing, we use the same timing and carrier frequency information that is used in the transmitter. The BER (bit error rate) of the DVB-T receiver output is measured to confirm the transmitter performance.

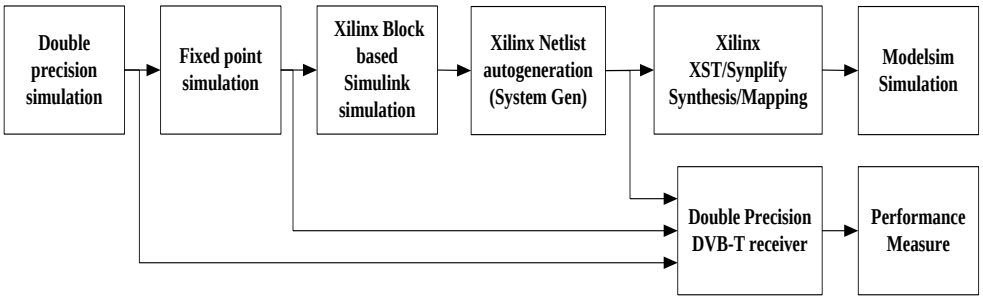

Figure 4. Design flow of the DTV transmitter system using Matlab simulink and Xilinx block set

We show an example simulink model of single channel DVB-T symbol generation block in Figure 5. Input signal which is processed by the SW processor in PC is first mapped to the complex constellation points and then FFT transformed. Then we increase the sampling rate of the input by the CIC filter. As is shown in the figure, we model every block with Xilinx block set so that the model can be implemented directly without RTL coding.

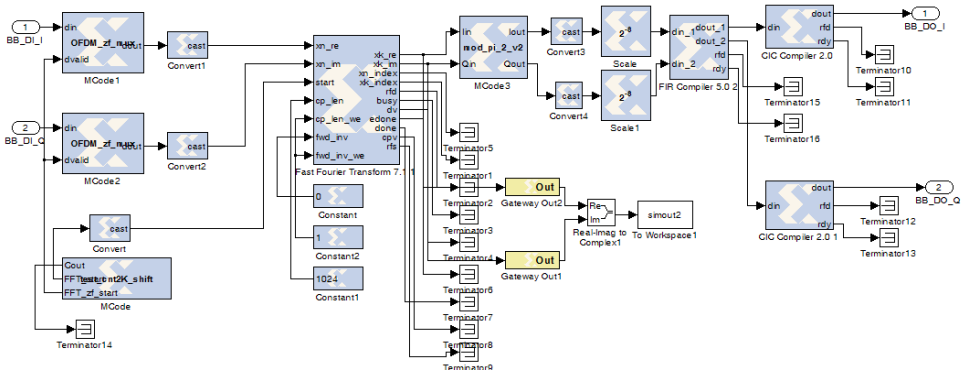

Figure 5. Simulink model of single channel DVB-T waveform generator

4. Implementation Results

We show the block diagram of the multi-channel DTV transmitter system in Figure 6. The system is composed of one main FPGA board and four small daughter boards. The main FPGA board includes the USB 2.0 interface, Xilinx Virtex4-LX200 FPGA, high density (128 GB) NAND flash memory and DDR2 SDRAM slot. To ease the system verification and for the module reusability, we implement the power module and CFC (compact flash card) or JTAG configuration module in separate daughter boards. For the USB 2.0 interface, we use the cypress CY7C68013 chip and optimize the Window device driver and 8051 firmware to satisfy the required high speed data transfer rate. We included the NAND flash memory such that the data processed by the PC SW can be stored in NAND flash memory to use the system as a DTV signal generator. The stored data is repeatedly read into the FPGA and played back continuously so that the system can be used as a signal source in a show room for a demonstration or compact manufacturing equipment in the factory. The storage capacity is high enough so that we can store approximately 2 minute's MPEG compressed video data. The picture of the implemented system is shown in Figure 7.

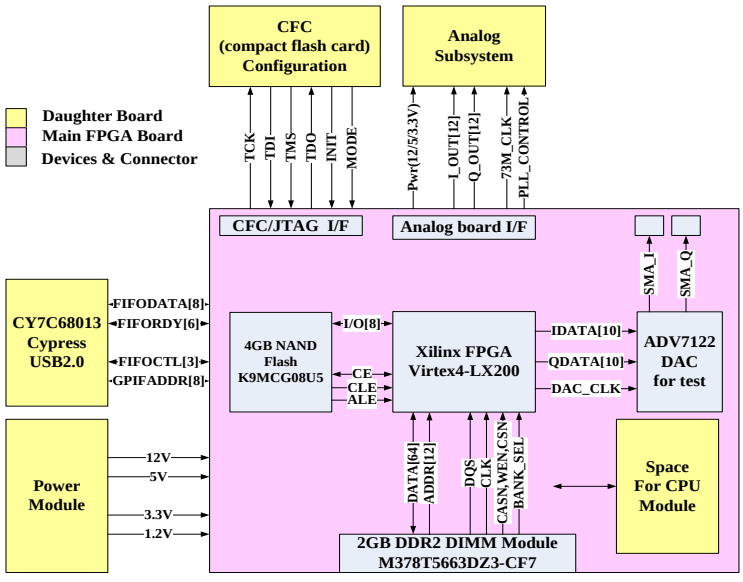

Figure 6. Block Diagram of the designed HW system

The system we implemented is DVB-T system with 8K FFT mode and 8 MHz channel bandwidth. We implemented four DVB-T channel signals considering the system complexity. Five stage CIC filter and 10 tap CIC compensation filter were used for the sampling rate up-conversion for multi-channel combining. Farrow type filter proposed in [8] can also be used to reduce the system complexity. Quadrature digital wave guide filter was used to generate a carrier signal for modulating the baseband OFDM signal to the low IF signal. To verify the system operation, we captured the output signal of the FPGA board and measured the PSD (power spectral density) of the output signal. The PSD of the four-channel combined signals is shown in Figure 8. The result shows that our proposed system generates multi-channel DVB-T signal more than 50dB sideband suppression capability, which satisfy the spectral mask specification of DVB-T system.

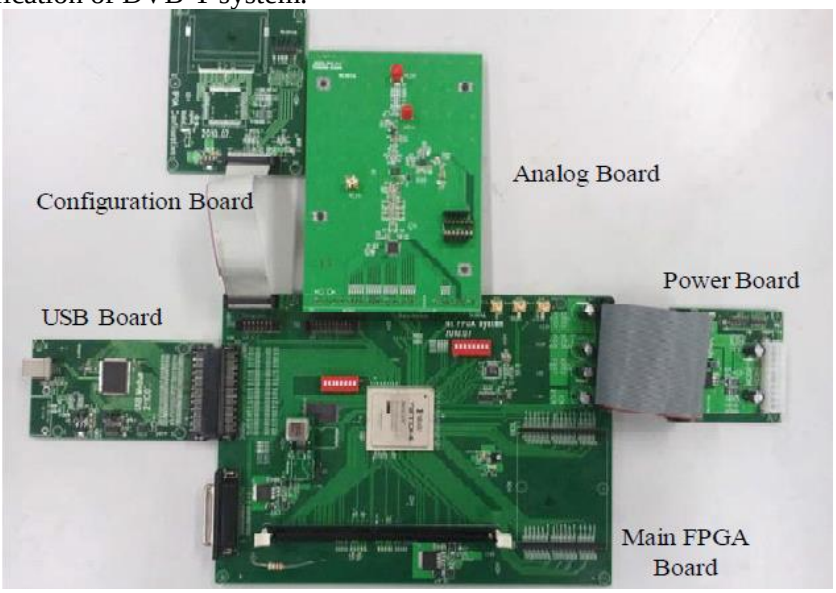

Figure 7. Picture of the implemented DTV transmitter HW system

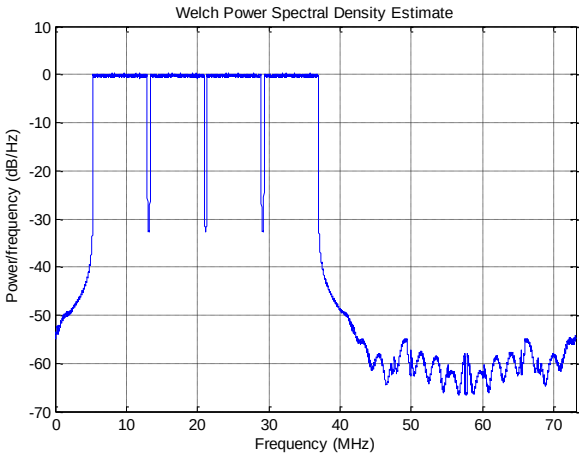

Figure 8. Power spectral density of multi-channel DTV transmitter system

5. Conclusions

In this paper multi-channel DVB-T transmitter is proposed. The system is composed of several subsystems operating partly by SW and partly by a HW module. The multi-channel DVB-T streams processed by the PC SW subsystem are transferred to the FPGA HW system via high speed serial link. The transferred data stream is processed by the FPGA HW module to generate the DVB-T OFDM signal. Several channel signals are generated simultaneously. We propose a simulink based system level design methodology where we model the DVB-T transmitter system in Matlab simulink and generate the net-list automatically with little RTL coding work. This methodology can significantly reduce the system design and verification time. Finally, the power spectral density of the simulation result is presented to show the combined multi-channel signal with good sideband suppression capability. The proposed system can be deployed in wide areas of applications where compact multi-channel DTV signal generators are required, for example when we test DTV sets with the multi-channel browsing capabilities in the LAB, show rooms with limited access to the signal sources or in the production lines where cost-effective test equipment setup is required.

Acknowledgments

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