Performance Analysis of CMOS Single Ended Low Power Low Noise Amplifier

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Abstract

This Paper presents an analysis of single ended low Noise Amplifier in a transceiver for wireless sensor network. The Low Noise Amplifier consumes a Power of 65.9μ W. The Noise analysis for the LNA is achieved for a frequency range of 1GHZ-3GHz.

Keywords*: Low Noise Amplifier, Low power, Noise analysis*

1. Introduction

In recent years, the semiconductor industry has produced consistently improving wireless chipsets in terms of functionality, cost, and form factor and power consumption. These advances have enabled the emergence of wireless micro sensor networks, which consist of a group of sensor nodes that are deployed remotely and used to relay sensing data to the end-user. Applications for sensor networks range from military, such as target tracking, to consumer and industrial, such as hospital monitoring or distributed sensing of factory equipment. As sensor networks mature, it is expected that nodes will further reduce in size and cost, allowing for the emergence of large scale sensor networks consisting of thousands of nodes. Sensor nodes are typically deployed in remote or inaccessible locations and must be powered either by batteries or through energy harvesting. Regardless of the energy source, energy efficiency is of paramount importance to enable node lifetimes on the order of months to years. The wireless transceiver is a critical block in sensor nodes as it often consumes the majority of available energy. Typical tracking and monitoring applications require transceivers to support average data rates up to tens of kilobits per second. A key metric for measuring the energy efficiency of wireless transceivers is *energy per bit*, representing the average amount of energy required by a transceiver to transmit or receive a single bit of data. Early transceivers designed for sensor networks achieved an energy per bit as low as 10 nJ/bit, and recent transceivers have achieved approximately 1 nJ/bit]. Although the energy per bit metric is valuable for comparing transceivers, there are numerous other specifications that must be considered including receiver sensitivity, transmitter output power and data rate. For example, a passive RFID system has an energy per bit of 0 but at the cost of extremely low receiver sensitivity. The design of wireless sensor networks however represents a difficult challenge. Smart environments represent the next evolutionary development step in building, utilities, industrial, home, shipboard, and transportation systems automation. Like any sentient organism, the smart environment relies first and foremost on sensory data from the real world. Sensory data comes from multiple sensors of different modalities in distributed locations. The smart environment needs information about its surroundings as well as about its internal workings; this is captured in biological systems by the distinction between exteroceptors and proprioceptors. Since many applications require fault-tolerant, long-term sensing, one important challenge is to design sensor networks that have long system life times.

Achieving long system lifetime is difficult because sensor networks range from military such as target tracking, to consumer electronics and industrial equipment, such as home lighting or distributed sensing of factory equipment. As sensor networks mature, it is expected that nodes will reduce in size and cost, allowing for emergence of large scale sensor networks consisting of thousands of millions of nodes. Low power consumption helps to increase the battery lifetime and to reduce the operating temperature. This means more stable performance due to less electrical parameter shift. Heat sinks can be shrunk or even removed, which results in smaller dimension and lower cost. However, challenges lie in compensating the degradation in the performance in order to meet the system specifications.

2. Low Noise Amplifiers

Ostensibly, one key component of any receiver chain is the low noise amplifier coming off the antennas. Since the signal at that point is comparatively weak, good gain and noise performance are necessary. The overall noise factor of the receiver front end is dominated by the first few stages and can approximated according the Frii's formula as

$$\mathbf{NF_{rec\text{-}front} = (1/G_{LNA})\ (NF_{subsequent} - 1) + NF_{LNA}}$$

Where $NF_{subsequent}$ is the total input-referred noise factor of the components following the LNA, and G_{LNA} and NF_{LNA} are the gain and noise factor, respectively, of the LNA itself. The noise of the LNA is injected directly into the received signal. Thus the LNA needs both high gain and low noise. There are well known trade-offs in amplifiers between noise and gain. Often, one is achieved at the expense of other. Through out the analysis, both the active devices and the input/output terminations are considered together in determining the impact on circuit stability, gain and noise performances. Here, power becomes the primary variable of interest. The inherent issues of the various parameters are discussed. In the absence of dedicated usable RF frequencies for wireless sensor networks, the intended RF link can only be established within officially allocated industrial, scientific, and medical (ISM) bands, which limits the choice to a few frequency ranges such as 1GHZ-2.5GHZ. The recently reported 0.9GHz CMOS receiver consumes only 2.2mW. In the proposed LNA design, the supply voltage is targeted as 1.0V and low power consumption is achieved. A drain voltage of 2.5 voltages is given. This LNA consumes a power of 38.3μ watts[1]. With the small power consumption, the LNA should

(i) amplify the received weak signals to the level suitable for processing,

(ii) provide gain to overcome the noise of subsequent stages while adding as little noise as possible and

(iii) handle large (unwanted) signal along with some very weak signal.

The receiver total noise figure is mainly determined by the LNA noise figure, for the gain of LNA is large enough. But, at the same time the noise should be as less as possible. However, the gain of the LNA should not be too high, otherwise the following stage, namely the mixer, gets saturated. Out of the several known topologies for narrow band LNA design, an appropriate topology is required for power optimized LNA design. For shunt series feedback common source topology, it is difficult to trade off among the gain, small noise figure and input/output matching. Resistor termination common source topology adds noise to the LNA. Inductive degeneration common source topology can satisfy the specification, but the isolation is not good enough compared to the cascode inductor source degeneration

topology. Above all, the cascode inductor source degeneration topology is selected for this design.

3. Circuit description

The proposed CMOS LNA circuit is shown in Fig. 1 which uses an inductor degeneration topology. A cascode transistor is used to isolate the local oscillator reverse leaking to the antenna from the LNA. Transistor M3 is the DC biasing transistor. By selecting the values for inductances Lg, and Ls, capacitance C1 and transistor size M1 as necessary, the value of the real part of the impedance can meet the matching requirements. The input impedance of the circuit at the resonance frequency $\omega 0$ is,

$$Zin = (gm\ Ls/\ Cgs) + j\omega_0(Ls + Lg) + 1\ j\omega_0\ Cgs,$$

where gm is the transconductance of the transistor M1, Cgs is the gate source capacitance. The value of Ls is optimized as 0.45 nH in this design according to the input matching requirement.

The inductor L1, capacitors C2 and C3 are for the output matching.

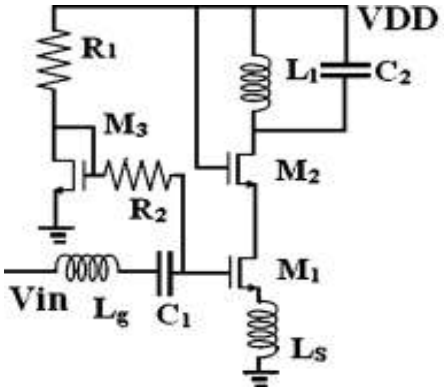

Fig. 1 Proposed CMOS LNA schematic diagram

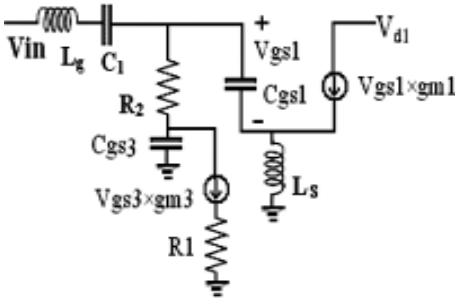

Fig.2 Small signal equivalent circuit of the input

Table.1 The details of devices in the LNA design

Components	Parameters	Functionality
M1, M2	60×(5 μm/0.18 μm)	Amplify the RF signal
M3	8×(5μ m/0.18 μm)	DC bias current mirror
L_g	35nH	Input Matching
L_s	0.45nH	Input Matching
L_1	14.7nH	Output Matching
C_1	8pF	Input Matching
C_2	0.5pF	Output Matching
Vdd	2.5v	Drain Voltage
R_1	4.8KΩ	DC Bias
R_2	50KΩ	Reduce the input from DC bias circuit

Yet, as lowVgs-VT value needs wider transistor, the optimum width of the device M1 is required to be as large as 300 μm, resulting in larger Cgs. This value expresses noise optimization in a way that takes power consumption explicitly into account. It may, however, be noted that the larger gate to source capacitor helps reducing current consumption [3]. In addition, the width of transistor M3 and the value R1 are optimized in order to control the gate voltage of the transistor M1. The LNA noise is primarily due to the transistor M1. The value of R2 is selected large enough, such as 50 kΩ, to give as less noise as possible to the whole circuit noise figure. The small signal equivalent circuit of the LNA input is shown in the Fig. 2. The RF input signal has two paths to the ground. The first is through Lg, C1, Cgs1 and Ls. This is what we want. The other one is through Lg, C1, R2 and Cgs3. The resistance R2 is high, about 50 kΩ. The impedance looking into this path is quite high. So, the RF leakage from R2 and transistorM3 gate to the ground is very small. In fact, R2 is introduced to help omit Cgs3 (i.e. capacitance from M3 gate to the ground). The DC bias ofM2 is optimized in terms of its gate width, while keeping the DC bias voltage of M1 as low as possible to reduce the power consumption of the circuit. The width of transistor M2 is optimally sized to be 300 μm in this design. The various component parameter of the Low Noise Amplifier design is tabulated in table [1]. The dc voltage gain produced by the circuit is shown in fig.3. The voltage gain reaches its maximum value of about 25 initially and it starts to degrade as the voltage starts increasing during the analysis part.

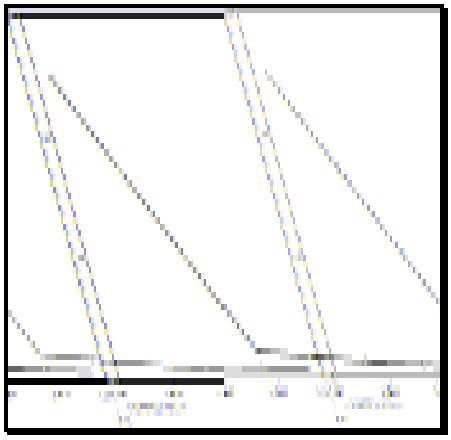

Fig.3 The DC Voltage gain produced by the circuit

4. Noise Analysis

Although many parameters specify an amplifier's noise performance, the two most important factors are voltage noise and current noise. Voltage noise is the voltage fluctuations at the input of an otherwise noise-free amplifier with shorted inputs. Current noise is the current fluctuations at the input of an otherwise noise-free amplifier with open inputs. The typical figure of merit for amplifier noise is noise density, also called spot noise. Voltage-noise density is specified in nV/√Hz, while current-noise density is usually shown in units of pA/√ Hz. These values are provided in all low-noise amplifier data sheets, and are usually specified at two frequencies: at less than 200Hz for the flicker-noise component, and at 1kHz for the flat-band component. For simplicity, these measurements are referred to the amplifier inputs to remove the need to account for the amplifier's gain. Newer low-noise amplifier designs with a CMOS input stage offer voltage-noise performance that is comparable to bipolar designs. CMOS-input amplifiers also meet or exceed the current-noise performance of the best JFETinput designs. These features make CMOS- input amplifiers an excellent choice for applications that require low distortion and low noise, such as audio preamplifiers. Additionally, the CMOS input stage allows for very low input-bias currents, low offset voltages, and very high input impedances, making these devices well suited for signal conditioning high-impedance sources. The gain of the described LNA is estimated by plotting the Bode plot on db.The input noise produced by the Low Noise Amplifier is plotted as in figure [4].

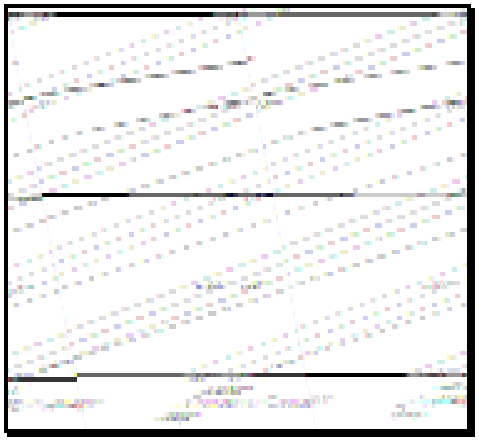

Fig.4 Input Noise produced by the LNA

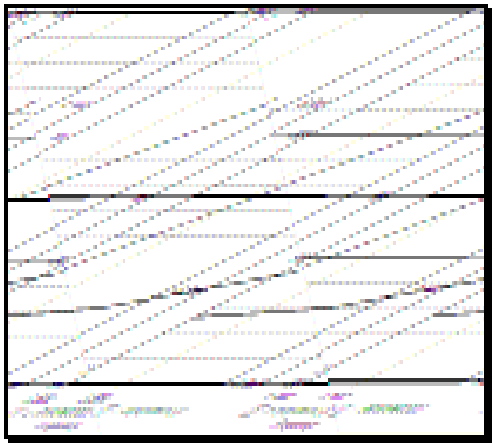

Fig.5 Output Noise Produced by the LNA

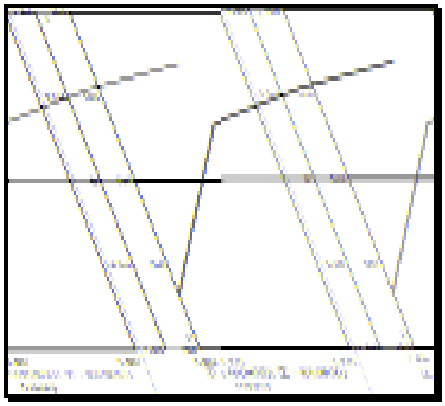

Fig.6 Input Noise in Volts

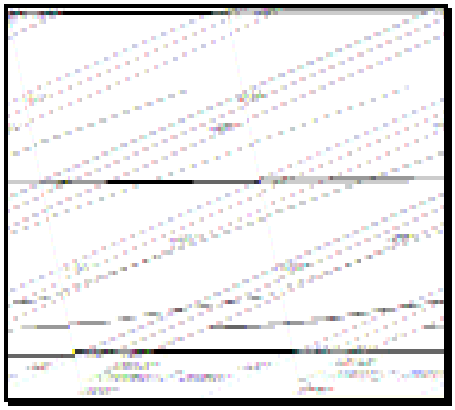

Fig.7 Output Noise in volts produced by the LNA

The output noise produced by the LNA is plotted in fig [5]. The noise plot crosses the 0db line at around 3GHz. The noise plots in voltage are shown in figures [6], [7]. In fig.6 the 0db line crosses the noise of 14 nV at a frequency of approximately1.8GHz and the plot tends the deviate at a frequency of about 2GHz. In out put noise plot fig.7 the 0db line cuts the 500pV line at frequency of about 3.3GHz. This infers that the circuit produces low noise at the output after amplification. The noise produced by various components are tabulated in table.2

Table.2 Noise Produced in the various components

Frequency (GHz)	M1 Sq v/Hz (10^{-20})	M2 Sq v/Hz (10^{-20})	M3 Sq v/Hz (10^{-28})	Input noise v/Rt Hz (10^{-8})	Output Noise v/Rt Hz (10^{-10})	Transfer Function (10^{-2})
1	3.020	2.821	3.568	1.131	2.415	2.135
1.58	3.502	2.906	6.025	1.533	2.532	1.652
2.512	5.429	3.513	19.83	1.617	2.991	1.847
3.981	26.86	17.15	23.18	1.678	6.636	3.955

5. Measurements and Results

The LNA is designed in SPICE environment. In-house available inductors, capacitors and packing models were included. The CMOS used is designed according the requirement. In this design antenna impedance and the filter impedances interfacing with LNA in the whole system were not considered as the primary focus was to match with test equipments having 50 ohm impedances for test purpose. Noise analysis is made for a frequency range of about 1GHz-3GHz and the plots are plotted as in figures [4]-[7].

6. Conclusion

A Low Power consumption of about 65.9μ watts is achieved for the LNA by an appropriate design. The presented results indicate that above LNA can be implemented in designing low power transceivers. The LNA operation is demonstrated by taking low power as the main factor.

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