International Journal of Control and Automation
Vol. 11, No. 7 (2018), pp.119-128
http//dx.doi.org/10.14257/ijca.2018.11.7.10

Signal/Power Integrity Analysis of High-Speed Memory Module with Meshed Reference Plane

Moonjung Kim

Institute of IT Convergence Technology,
Dept. of Electrical Electronic Control Engineering,
Kongju National University, Republic of Korea
mjkim@kongju.ac.kr

Abstract

In this paper, the signal integrity and power integrity of mesh patterns are investigated in the Double Data Rate 4 Small Outline Dual In-line Memory Module (DDR4 SODIMM). The mesh patterns are designed to be a square in the power plane and are repeated periodically with a spacing of 1 mm. The sizes of the mesh patterns are considered in terms of the operating speed of the DDR4 SODIMM and its wavelength. The effect of signal integrity on the address line is analyzed as the mesh size increases. The eye-diagram analysis of the address line is also carried out by comparing the aperture factor. As the mesh size increases, the eye-diagram aperture decreases. It is verified that the mesh size of 1 mm^2 or less has little effect on the signal transmission of the address line. The power integrity of the power planes with different mesh patterns is analyzed. The effect of resonance and impedance on the power-ground plane is investigated. In this work, it is demonstrated that the mesh size smaller than 1 mm^2 has the same impedance results as the solid plane. However, as the mesh size exceeds 1 mm^2, the impedance increases in all frequency ranges.

Keywords: *DDR4 SODIMM, Meshed Reference Plane, Signal Integrity, Power Integrity*

1. Introduction

Recently, miniaturization and high-integration in the electronic systems have caused various problems in signal integrity and power integrity [1-3]. As the signal is transmitted at high-speed, problems such as crosstalk and reflection may occur in the electronic system and then these can degrade its signal quality. [4-5]. Therefore, the design modifications to electronic systems often have occurred in high-speed applications [6-7].

Impedance mismatch is one of the significant factors that can degrade the signal transmission characteristics. But impedance matching can be achieved by adjusting the signal structure in a printed circuit board (PCB). Therefore, the width and spacing of the signal line should be designed to achieve impedance matching in applications of high-speed operating. Impedance matching can be also implemented by modifying the reference plane. Numerical studies have been reported on the electromagnetic characteristics that occur when a mesh is applied on a reference plane [8-10]. Recently, research was presented to adjust the radiation characteristics of electromagnetic interference by introducing mesh patterns in a reference plane [8]. But, in this paper, the influence of mesh pattern on the signal line and the reference plane is analyzed in high-speed memory module.

Received (March 23, 2018), Review Result (June 1, 2018), Accepted (June 5, 2018)

ISSN: 2005-4297 IJCA

2. Mesh Design

Dual Data Rate 4 Small Outline Dual In-line Memory Module (DDR4 SODIMM) has a size of 67.6 × 30 mm^2 and consists of a 6-layer PCB. Figure 1 shows the board routing of the DDR4 SODIMM. The layer structure of the board is summarized in Table 1. SDRAM (Synchronous Dynamic RAM) devices are mounted only on the top layer of the PCB.

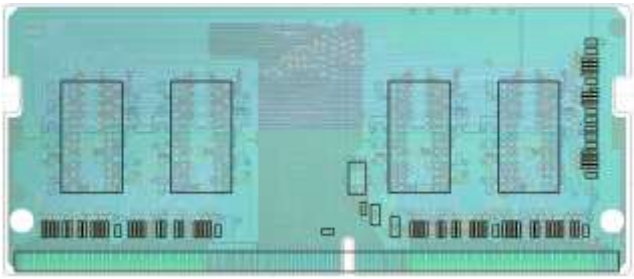
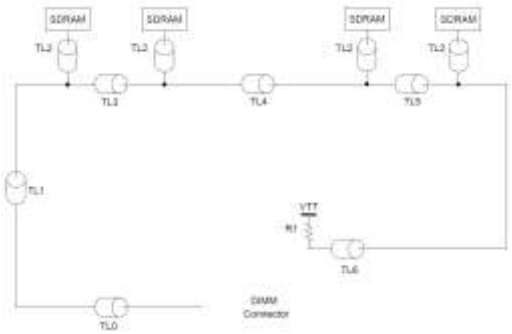


Figure 1. Board Routing of DDR4 SODIMM

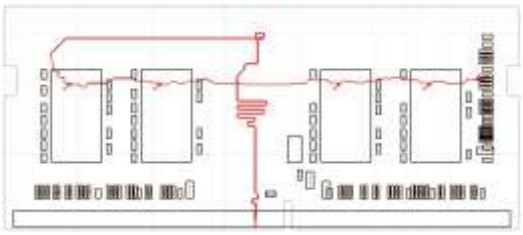
Table 1. Layer Structure of Printed Circuit Board

Layer	Thickness (mm)	Material
Top layer	0.04	Copper
Dielectric	0.06	FR4 epoxy
Second layer	0.03	Copper
Dielectric	0.08	FR4 epoxy
Third layer	0.03	Copper
Dielectric	0.71	FR4 epoxy
Fourth layer	0.03	Copper
Dielectric	0.08	FR4 epoxy
Fifth layer	0.03	Copper
Dielectric	0.06	FR4 epoxy
Bottom layer	0.04	Copper

As shown in Figure 1, four SDRAMs are arranged and various signal lines are routed in the board. Figure 2 shows the topology and routing of the address line. The address line is routed from the DIMM connector to the final transmission line (TL) and is terminated through a resistor and a VTT power supply in Figure 2 (a). Each SDRAM is connected to a branch point between TLs. Figure 2 (b) shows the routing path of the address line in the board. Fly-by topology is applied in the routing design of all address lines. The address line has a length of about 133 mm and a width of 0.15 mm. Analysis of the signal integrity is performed on the address line.



(a) Topology of Address Line



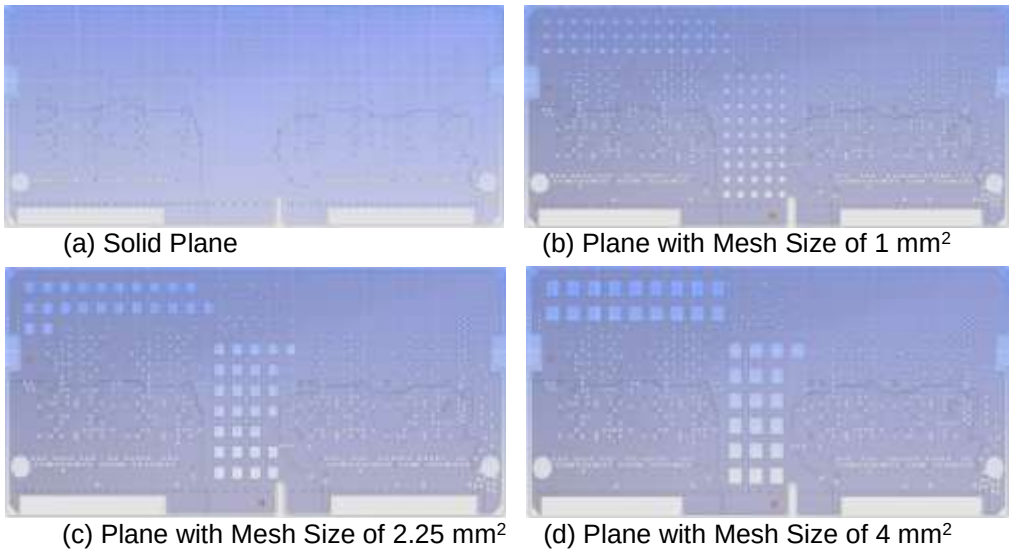
(b) Routing of Address Line

Figure 2. Structure and Routing of Address Line in DDR4 SODIMM

Effect of the mesh pattern on reference plane in the DDR4 SODIMM is investigated in this study. The reference plane of the address line is VDD and the mesh structure applied in VDD plane. Therefore, its signal integrity of the address line on a meshed VDD is analyzed. The size of mesh pattern is designed based on the operation speed of DDR4 SODIMM. SDRAM in this work has an operating speed of 2400 Mbps, which corresponds to a frequency of 1.2 GHz. Its wavelength can be calculated from Equation 1.

$$\lambda = \frac{c}{n \times f} = \frac{c}{\sqrt{\varepsilon_r} \times f} \tag{1}$$

where f is the operating frequency, c is the speed of light in a vacuum, n is the refractive index in the dielectric layer and ε_r is the dielectric constant. The dielectric material of the PCB has a dielectric constant of 4.4. The wavelength can be calculated by reflecting the effective bandwidth of the digital signal, which is the fifth harmonic of the frequency, in other words, 3.6 GHz. Considering the design limitation that the mesh size should be small enough, $\lambda/10$ criterion is applied in the calculation of the mesh size. Therefore, the mesh size is determined to be less than 4.0 mm and then square mesh is designed on the VDD plane of the PCB. For analyzing the effect of the signal quality on the mesh size, meshes with different lengths on one side of 1.0 mm, 1.5 mm and 2.0 mm are designed in this work. On the other hand, the mesh spacing is kept constant at 1 mm. Figure 3 shows the solid VDD plane and different meshed VDD planes. The plane area to which the mesh patterns can be applied is limited because there are a large number of vias in the VDD plane. As shown in Figure 3, the mesh patterns are applied to only a part of the VDD plane and are placed at the center and top left corner of the VDD plane.



(a) Solid Plane (b) Plane with Mesh Size of 1 mm^2

(c) Plane with Mesh Size of 2.25 mm^2 (d) Plane with Mesh Size of 4 mm^2

Figure 3. VDD Planes with Different Mesh Sizes

A periodic mesh pattern is designed on the VDD plane as shown in Figure 3. The effect of signal quality on meshed planes is analyzed by comparing their eye-diagrams. The analysis of the frequency-domain and time-domain is calculated using ANSYS SIwave and Designer. Figure 4 shows the port location of the address on the board and 6 points are designated as a port. The ports are located on the DIMM connector, entrance of loaded section and 4 SDRAM branches.

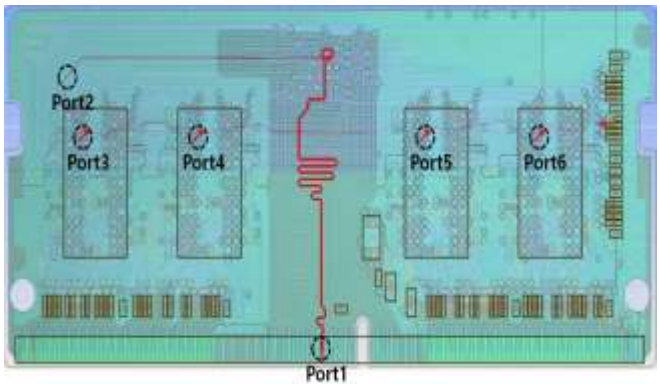


Figure 4. Port Location of Address Line

Figure 5 shows the equivalent circuit model of the address line for eye-diagram analysis. It includes an S-parameter model corresponding to each TL of the address line as shown in Figure 2 (a). The address line has 4 branches from Trace1 to Trace6 and is connected to the termination resistance and termination voltage at its end. Lead_in in Figure 5 is an S-parameter model corresponding to TL between port 1 and port 2 in Figure 4. Trace1 to Trace6 are the S-parameter models of each TL in the address line as shown in Figure 2 (a).

All branches are modeled identically using Trace2, resistance, inductance and capacitance. Trace2 is a stub where the branch from the address line is connected to SDRAM at its end. In this work, Trace2 is followed by RLC package model and the input capacitance of SDRAM. As shown in Figure 5, a probe is placed to check eye-diagram for each SDRAM. Table 2 summarizes the equivalent circuit elements and values of the address line.

The eye-diagram of the address line is analyzed using ANSYS Designer. The operating speed of the DDR4 SODIMM is 2400 Mbps and the Unit Interval (UI) is set to 0.416 ns. The rising time and falling time are assigned as 0.138 ns.

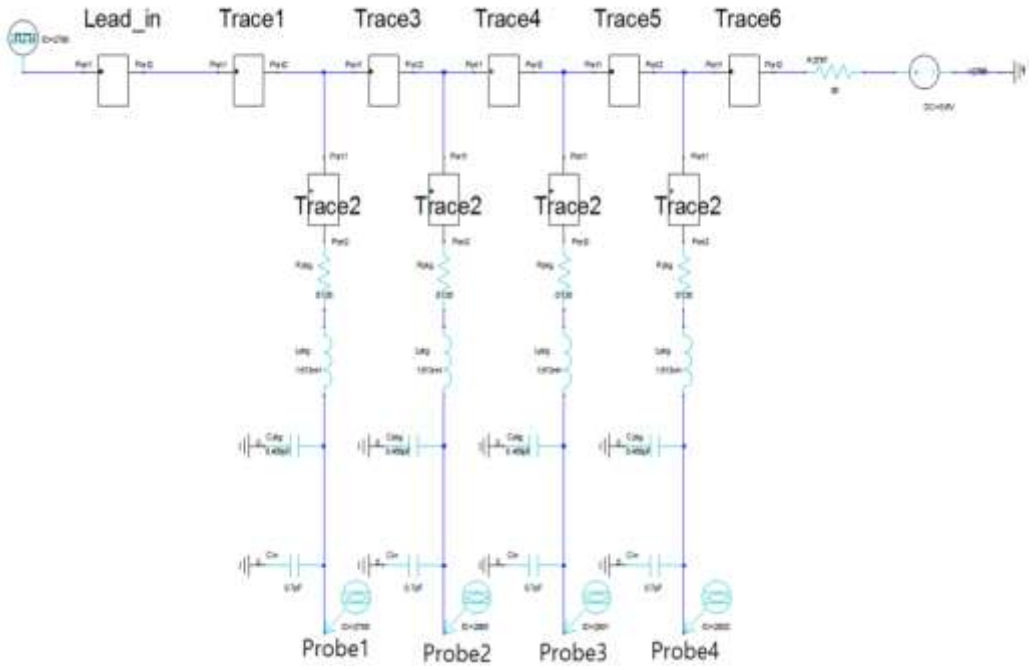


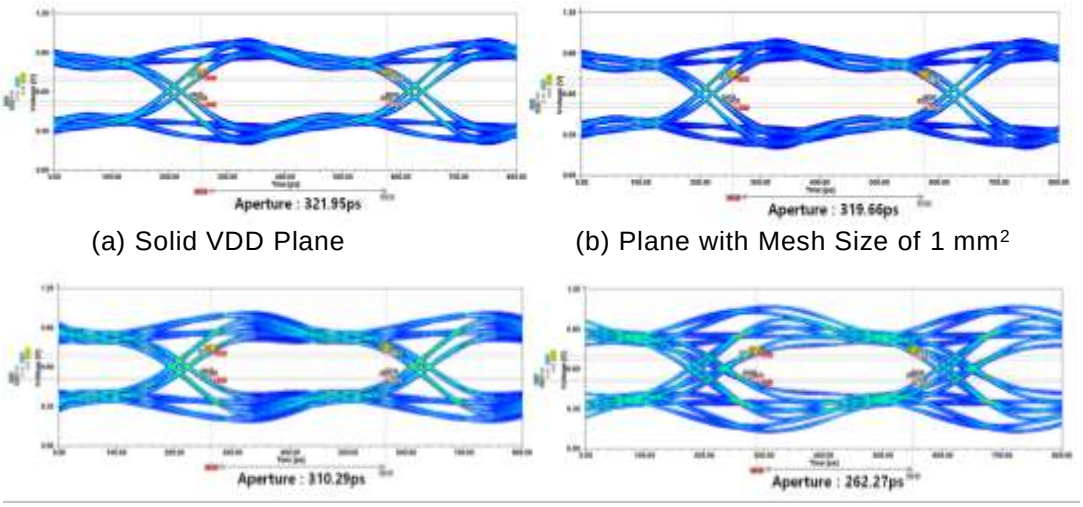
Figure 5. Equivalent Circuit Model of the Address Line

Table 2. Equivalent Circuit Element and its Value in the Address Line

Parameter	Value
Package resistance (R_{pkg})	0.135 Ω
Package inductance (L_{pkg})	1.613 nH
Package capacitance (C_{pkg})	0.468 pF
Chip input capacitance (C_{in})	0.7 pF
Termination resistance (R_T)	36 Ω
Termination voltage (V_{TT})	0.6 V

3. Analysis and Result

The eye-diagram, resonance and power-ground impedance calculations are performed for the address line and meshed VDD plane as shown in Figure 3 and Figure 4. ANSYS SIwave and Designer are used for the calculations of signal integrity and power integrity. The signal transmission characteristics of the address line on the meshed VDD plane are investigated through the eye-diagram calculation at the probe position of each SDRAM as shown in Figure 5. Figure 6 shows the eye-diagram results at Probe1 position.

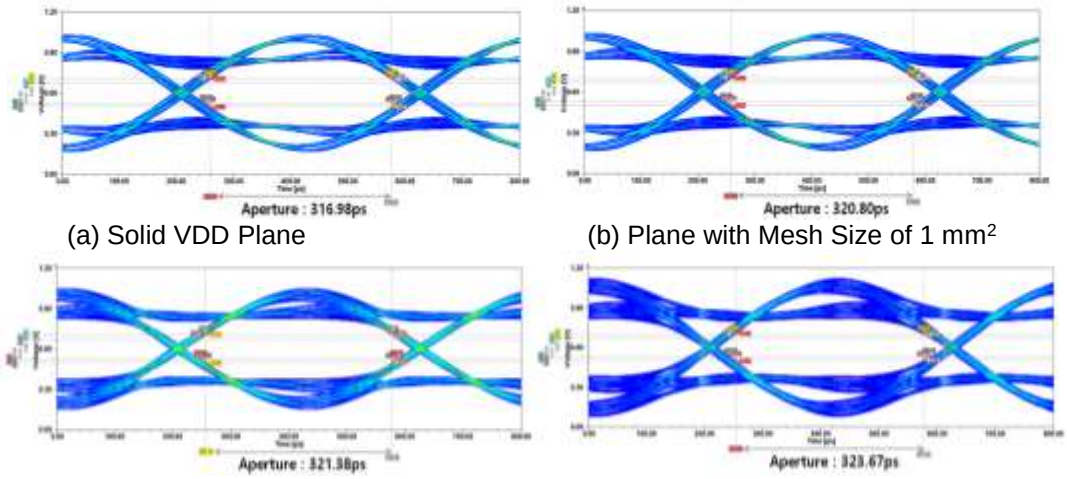


(a) Solid VDD Plane (b) Plane with Mesh Size of 1 mm^2

(c) Plane with Mesh Size of 2.25 mm^2 (d) Plane with Mesh Size of 4 mm^2

Figure 6. Eye-diagram at the Location of Probe1

In this work, aperture is used to compare the difference in the signal quality for the meshed VDD planes and is calculated from the voltage at the logic input level for DC and AC of the DDR4 SODIMM [11]. As shown in Figure 6, the jitter of the signal increases with the mesh size at Probe1 and the aperture decreases. However, the solid VDD plane and the plane with mesh size of 1 mm^2 are almost the same. Therefore, the mesh size of 1 mm^2 or less doesn't affect substantially the aperture. The aperture difference between the plane with mesh size of 2.25 mm^2 and the solid plane is less than 4%. But, the plane with mesh size of 4 mm^2 has relatively large differences. The mesh size at Probe1 position increases the jitter and the voltage fluctuation and then decreases its aperture. Adding mesh patterns may result in a change in the characteristic impedance of the address line, which can cause its impedance discontinuity. As the mesh size increases, signal reflection and voltage fluctuation at Probe 1 can increase due to impedance discontinuity.

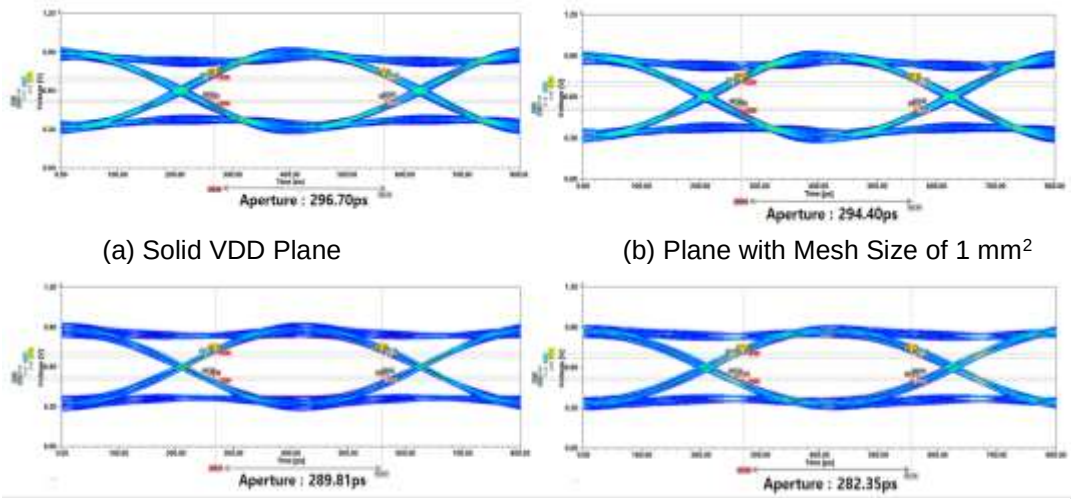


(a) Solid VDD Plane (b) Plane with Mesh Size of 1 mm^2

(c) Plane with Mesh Size of 2.25 mm^2 (d) Plane with Mesh Size of 4 mm^2

Figure 7. Eye-diagram at the Location of Probe2

Figure 7 shows the eye-diagram of the address line with the different meshed VDD planes at Probe2 position. As the mesh size increases in the VDD plane, the voltage fluctuation and the aperture also increases. However, there is no big difference in aperture. The solid VDD plane and the plane with mesh size of 1 mm^2 have almost similar voltage fluctuations.

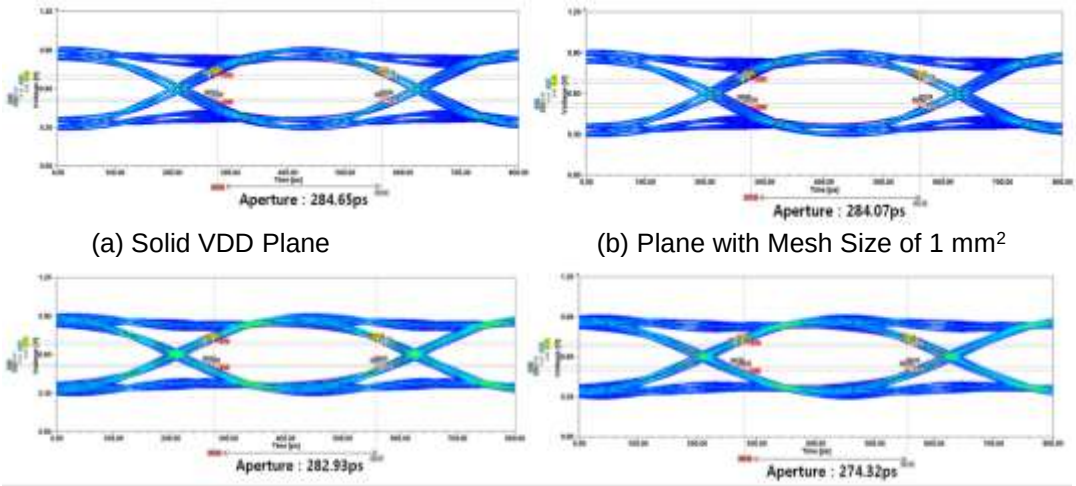


(a) Solid VDD Plane (b) Plane with Mesh Size of 1 mm^2

(c) Plane with Mesh Size of 2.25 mm^2 (d) Plane with Mesh Size of 4 mm^2

Figure 8. Eye-diagram at the Location of Probe3

Figure 8 shows the eye-diagram at Probe3 position. All VDD planes have similar eye-diagram characteristics. But the aperture decreases with the mesh size. Compared with results at Probe1 and Probe2, it can be seen that the voltage fluctuation at Probe3 is greatly reduced. Probe3 position is closer to the termination resistor in the address line than Probe1 and Probe2 positions. This leads to a reduction in signal reflection and voltage fluctuation.



(a) Solid VDD Plane (b) Plane with Mesh Size of 1 mm^2

(c) Plane with Mesh Size of 2.25 mm^2 (d) Plane with Mesh Size of 4 mm^2

Figure 9. Eye-diagram at the Location of Probe4

Figure 9 shows the eye-diagram of the address line with the meshed VDD planes at Probe4 position. The aperture decreases with the mesh size but has a similar value except for the plane with mesh size of 4 mm^2. The solid VDD plane and planes with mesh size of 1 mm^2 and 2.25 mm^2 exhibit substantially the same aperture results.

Mesh size doesn't have a significant effect on the voltage fluctuation at Probe4 and all planes shows almost the same results.

Table 3 summarizes the effect of the mesh size on the apertures of the eye-diagram. As the mesh size increases, the aperture decreases. The periodic mesh pattern is applied to the VDD plane in this paper. This may cause impedance discontinuity in the address line. As a result, signal reflection and voltage fluctuation can be increased. Figure 10 shows the aperture at each probe position in the address line. The solid VDD plane and the plane with mesh size of 1 mm^2 have the same tendency for the probe position and also show almost similar results. Therefore, it is verified that the mesh size smaller than 1 mm^2 has no significant effect on the signal transmission characteristics of the eye-diagram in this work. However, when the mesh size exceeds 1 mm^2, the aperture decreases greatly.

Table 3. Effect of Mesh Size on Apertures of Eye-diagram

Location of probe	Aperture (ps)			
	Solid VDD plane	Plane with mesh size of 1 mm^2	Plane with mesh size of 2.25 mm^2	Plane with mesh size of 4 mm^2
Probe1	321.95	319.66	310.29	262.27
Probe2	316.98	320.80	321.38	323.67
Probe3	296.70	294.40	289.81	282.35
Probe4	284.65	284.07	282.93	274.32

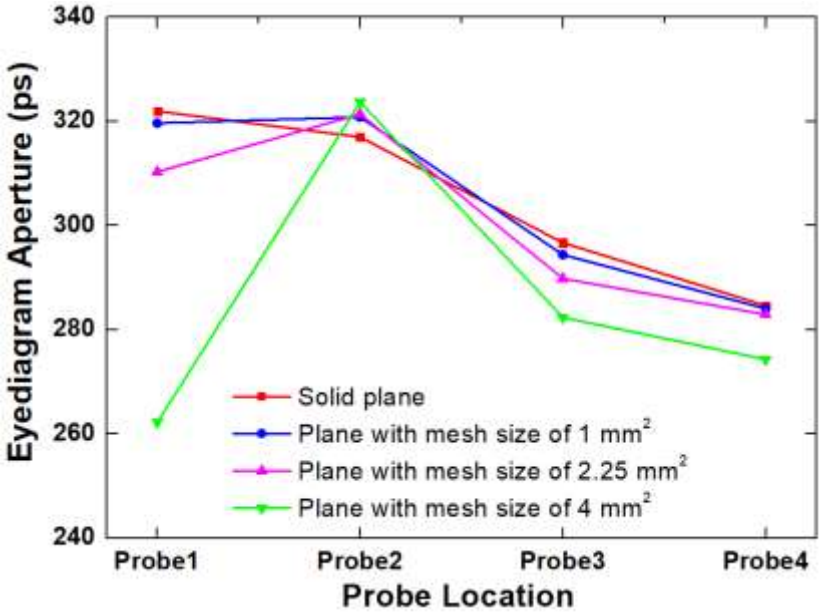


Figure 10. Aperture at Probe Position

The power-ground impedance can be changed because the mesh patterns are applied to the design of the VDD plane. Therefore, the power integrity simulation is performed to analyze this effect. The resonance between the VDD and VSS planes is calculated using ANSYS SIwave. The power-ground impedance of DDR4 SODIMM board where the resonance occurs is also calculated. Figure 11 shows the distribution of the electromagnetic field between the VDD and VSS Planes. A resonance occurs in the circle shown in Figure 11. This resonance area may degrade

the signal transmission characteristics of the address line routed on the meshed VDD plane. Figure 12 shows the impedance of the VDD plane and the VSS plane for each mesh size. The significant resonance occurs at 1.8 GHz in all mesh sizes, which leads to an increase in the impedance around this frequency range. However, the impedance at 1.8 GHz doesn't significantly affect the operating of the DDR4 SODIMM because its clock frequency is set to 1.2 GHz and its impedance is relatively low. The solid VDD plane and plane with mesh size of 1 mm^2 show almost the same impedance characteristics. It is verified that the mesh size smaller than 1 mm^2 has little effect on the impedance. However, as the mesh size exceeds 1 mm^2, the impedance increases in all frequency ranges.

Figure 11. Electromagnetic Field Distribution in the VDD-VSS Plane

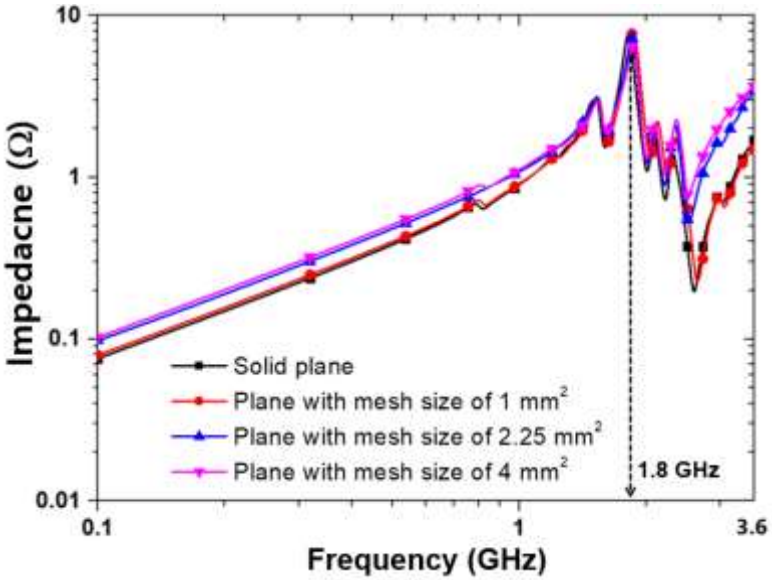


Figure 12. Impedance of VDD Plane and VSS Plane

4. Conclusion

In this paper, analysis of the signal integrity and the power integrity is performed as the mesh is applied to the VDD plane in the DDR4 SODIMM. Its eye-diagram calculation is investigated to analyze the signal transmission characteristics of the address line routed on the VDD plane. As the mesh size increases in the plane, the eye-diagram aperture decreases. However, the solid VDD plane and the plan with mesh size of 1 mm^2 have almost the same results for aperture and power-ground impedance. Therefore, it is verified that the mesh size of 1 mm^2 or less has little effect on the signal transmission of the address line. In addition, even though the periodic mesh area is removed from the

VDD plane, the plane with mesh size of 1 mm^2 has the same impedance results as the solid plane.

Acknowledgment

This work was supported by the research grant of the Kongju National University in 2016. This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(2017R1D1A3B03033760). The author is grateful to Yoon-Chan Nam for his technical support.

References

[1] M. Sindhadevi, M. Kanagasabai, H. Arun and K. Shrivastav, "Signal Integrity Analysis of High Speed Interconnects in PCB Embedded with EBG Structures", Journal of Electrical Engineering & Technology, vol. 11, **(2016)**, pp. 175-183.
[2] S. Kwak, Y. Jo, J. Jo and S. Kim, "Power Integrity and Shielding Effectiveness Modeling of Grid Structured Interconnects on PCBs", Journal of Semiconductor Technology and Science, vol. 12, **(2012)**, pp. 320-330.
[3] K. H. Chung, Y. J. Jang, C. W. Jung and S. K. Kim, "A Study on Source Stability Design Method by Power Integrity Analysis", The Korea institute of Electronic Communication Sciences, vol. 9, **(2014)**, pp. 753-759.
[4] S. Y. Kim, S. G. Jang, S. S. Nam, H. G. Bang and Y. K. Chin, "Crosstalk in High Speed Digital Signal Transmission Line", The institute of Electronics Engineers of Korea, vol. 31, **(1994)**, pp. 989-998.
[5] J. K. Yang and M. Kim, "Improvement of Connector Performance Using Analysis of Characteristic Impedance", The Institute of Electronics Engineers of Korea, vol. 48, **(2011)**, pp. 47-53.
[6] J. W. Choi, K. S. Park, M. J. Chai, J. W. Kim and K. Kwack, "Design DDR3 ZQ Calibration Having Improved Impedance Matching", Conference on the Institute of Electronics Engineers of Korea, **(2008)**, pp. 579-580.
[7] J. Lee, "Matrix Type CRC and XOR/XNOR for High-Speed Operation in DDR4 and GDDR5", Journal of the Institute of Electronics and Information Engineers, vol. 50, **(2013)**, pp. 136-142.
[8] E. Marzolf and M. Drissi, "Analysis of Transmission Lines over Slotted Ground Plane and Method of Compensating Resonance Effect", Electronics System Integration Technology Conference, **(2006)**, pp. 62-66.
[9] U. Choi, Y. J. Kim and Y. S. Kim, "Crosstalk Reduction in Printed Circuit Board Using Irregularly-Spaced Vias in a Guard Trace over a Slotted Ground Plane", Circuit Theory and Design Conference, **(2009)**, pp. 794-797.
[10] Y. Nam and M. Kim, "Analysis of Signal Transmission Characteristics on Meshed Ground Plane", International Journal of Control and Automation, vol. 10, **(2017)**, pp. 145-154.
[11] DDR4 SDRAM SO-DIMM Standard, **(2016)** June.

Author

Moonjung Kim, he received the B.S. degrees in electronic engineering from Kyungpook National University, Daegu, Republic of Korea, in 1997 and the M.S. and Ph.D. degree in electrical and electronics engineering from Korea Advanced Institute of Science and Technology, Daejeon, in 2003. Since September 2006, he has been with the Department of Electrical Electronic and Control Engineering, Kongju National University, Chungnam, Korea, as a faculty member. His current research interests include the signal/power integrity and signal transmission analysis in the high-speed package/board/system.

