International Journal of Control and Automation
Vol. 11, No. 2 (2018), pp.103-114
http//dx.doi.org/10.14257/ijca.2018.11.2.09

PID Controller Design using Youla Parameterization in the Voltage Bus Conditioner

Houng-Kun Joung[1] and Sang-Min Lee[2*]

[1]*Dept. of Mechanical & Automotive Engineering, Hanyang Cyber University*
[2]*Chungbuk Technopark*
[1]*21c8545@hanyang.ac.kr*, [2]*leesm@cbtp.or.kr*

Abstract

The DC distributed power system requires a filter due to the characteristics of constant power load (CPL) and switching noise and has unstable characteristics owing to negative impedance. This study aimed to control the voltage bus conditioner (VBC) in order to resolve the instability of DC distributed power system with CPL characteristics. The PID controller design method proposed in this study designed a PID controller by using Youla parameterization for ensuring robustness, stability, and internal stability. The simulation results showed that the proposed method offered better performance.

Keywords*: DC Distributed Power System, Voltage Bus Conditioner, PID Controller, Youla Parameterization*

1. Introduction

As power demand increases and supply voltage decreases, power systems have new challenges. DC distributed power systems are currently used in various fields including communication systems, military facilities, aerospace, electric vehicles, and new renewable energy systems [1][2][3][4][5]. A typical DC distributed power system is as shown in Figure 1.

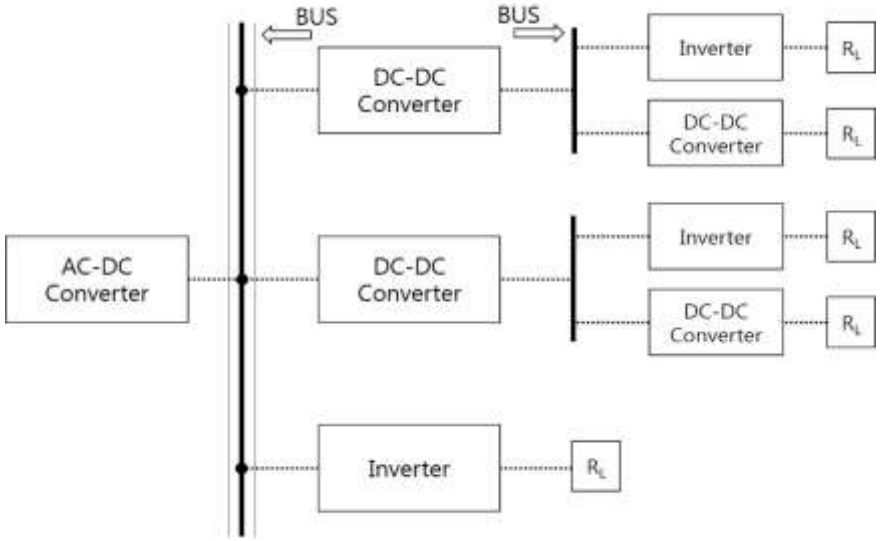

Figure 1. A Schematic Diagram of General High Voltage DC Distributed Power System

Received (October 19, 2017), Review Result (December 19, 2017), Accepted (January 28, 2018)
* Corresponding Author

ISSN: 2005-4297 IJCA

The converter generally has the characteristics of constant power load (CPL) and requires an appropriate filter due to switching noise (Figure 1). These characteristics result in negative impedance [6]. A typical DC distributed system consists of a source converter and a load converter (Figure 2).

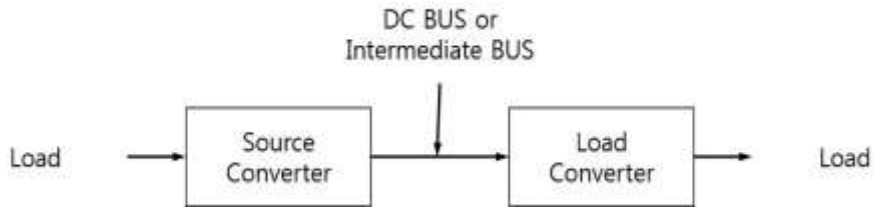

Figure 2. Structure of Partial DC Distributed Power System

A load converter with CPL characteristics has the characteristics of negative impedance and these characteristics can make the whole DC distributed power system unstable due to the interaction with the input filter. The voltage bus conditioner (VBC) is a power converter with having an energy storage device to resolve the instability issue of the bus voltage. The VBC generally has a bi-directional structure [7]. Moreover, it can be divided into the current type VBC and the voltage type VBC depending on the energy storage type. The current-type VBC can efficiently utilize the energy stored in the storage inductor, but it has a shortfall of losing power a lot during a steady state condition. Furthermore, it is also difficult to control it efficiently when the load current is larger than the current flowing through the inductor [7]. However, these shortfalls can be overcome by using cryogenic power electronics and superconducting coils. Additionally, the shortfalls of the above-mentioned current-type VBC can be supplemented by the voltage type VBC. The voltage-type VBC always require a large-capacity storage capacitor because the size of the voltage stored in the storage capacitor must be always larger that of the bus voltage [8]. This study used a voltage-type VBC with having a small capacity capacitor, which could overcome the disadvantage of a voltage-type VBC with a large-capacity capacitor [8]. There are many methods to control a voltage-type VBC with having a small capacity capacitor and these methods include the optimal linear quadratic regulator (LQR), [9][10], LQG-LTR[11], and H^{∞} [11][12], based on the mathematical theories. Since these mathematical methods are designed to satisfy the required performance even in the worst case, the controllers have higher orders than the controlled system. It is not difficult to realize the design of the controller because of the improvement of the processor performance and the computing power. However, the PID controller is more preferred because the PID controller is flexible and simple in the aspect of effects by investment and it is easier to design than the optimal control theory [13].

This study designed a PID controller by using Youla parameterization in order to control VBC and secure the internal stability. The PID controller tuning method proposed in this paper determines the control gain of the PID controller by using Youla parameterization and considering the inputs and outputs between each system in addition to the input and output of the entire system. Therefore, it is more stable and robust than the existing PID controller design.

2. Voltage Bus Conditioner

The topology of the current-type converted proposed in this study is shown in Figure 3, where V_C means the bus voltage. C_F has a small capacity in order to mitigate the switching frequency. C_{ST} is a storage capacitor and LF regulates the current between Bus Voltage V_c and V_{ST} (storage voltage) during on or off while two switches (Q_1 , Q_2) have a short dead time symmetrically. The characteristics of a power converter, which switches,

are complex. These complex characteristics can be expressed by using a state-space model [14]. When I_C is assumed to be 0 in Figure 3, $I_S \cong I_L$ can be considered true and it can be expressed as a state space averaging equation (Equation (1)).

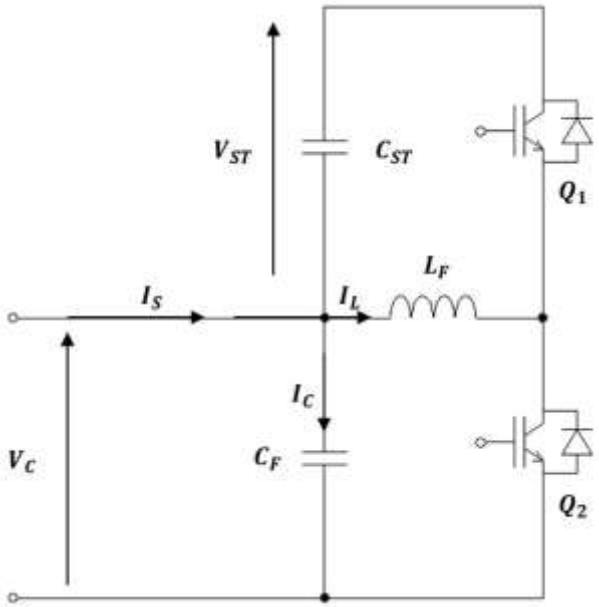

Figure 3. The Topology of the Voltage Bus Conditioner

$$\begin{bmatrix} \dot{\overline{V_{ST}}} \\ \dot{\overline{I_L}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1-D}{C_{ST}} \\ -\frac{1-D}{L_F} & 0 \end{bmatrix} \begin{bmatrix} \overline{V_{ST}} \\ \overline{I_L} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{D}{L_F} \end{bmatrix} \overline{V_C} \tag{1}$$

In Equation (1), D means the duty ratio and it is the standard when Q_2 is on. The duty ratio of the steady-state is equal to Equation (2).

$$\mathrm{D} = \frac{\mathrm{V_{ST}}}{V_C + V_{ST}} \tag{2}$$

When a linearized small signal model is expressed by Equation (1), it can be expressed as Equation (3).

$$\begin{bmatrix} \overline{V_{ST}} \\ \overline{I_L} \end{bmatrix} = \frac{\begin{bmatrix} \frac{(1-D)D}{L_F C_{ST}} \\ \frac{D}{L_F} s \end{bmatrix} \begin{bmatrix} V_{ST} \\ I_L \end{bmatrix} + \begin{bmatrix} -\frac{I_L}{C_{ST}} s - \frac{(1-D)V_T}{L_F C_{ST}} \\ \frac{V_C + V_{ST}}{L_F} s + \frac{(1-D)I_L}{L_F C_{ST}} \end{bmatrix} D}{s^2 + \frac{(1-D)^2}{L_F C_F}} \tag{3}$$

When the transfer function of I_L against the changes of duty is expressed by Equation (3), it can be expressed as Equation (4).

$$\mathrm{G(s)} = \frac{\overline{I_L}}{D} = \frac{\frac{\mathrm{V_T}}{L_F} s + \frac{(1-D)I_L}{L_F C_{ST}}}{s^2 + \frac{(1-D)^2}{L_F C_{ST}}} \tag{4}$$

The location of zero in Equation (4) changes because the current I_L in the numerator of Equation (4) has a positive or a negative value owing to the switching action of two switches (Q_1 and Q_2). It greatly affects the response speed and the characteristics of the system.

3. Controller Design

3.1. PID Controller Structure

Two representative PID controller structures are the parallel type structure and the serial type structure. It is easy to develop a parallel structure formula and the control input u(t) is expressed as Equation (5). The block diagram of it can be described as Figure 4 [13].

$$\mathrm{u(t)} = \mathrm{K_{pp}}(e(t) + \frac{1}{K_{ip}}\int_0^t e(\tau)d\tau + K_{dp}\frac{de(t)}{dt}) \tag{5}$$

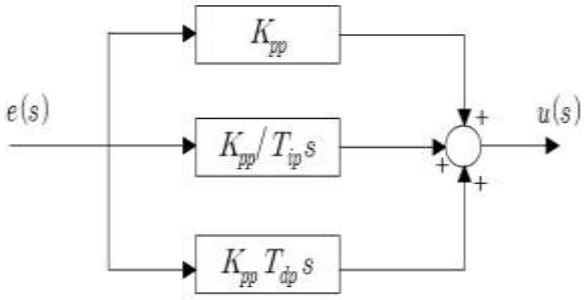

Figure 4. Block Diagram of the PID Controller's Parallel Structure

The proportional element P, the integral time I, and the differential time D parts are separated in the parallel structure of Figure 4. It is the ideal PID controller structure. However, in practice, it has a disadvantage of requiring more analog amplifiers than a series structure PID controller to realize it. This study used a parallel structure PID controller, which is easy to formulate, because it is possible to interchange a parallel structure PID controller with a series structure PID controller at each design parameter, although the series structure PID controller is more commonly used in practice. The design parameters of the PID controller is set as proportional gain ($\mathrm{K_P}$), integral time ($\mathrm{K_i}$), and differential time ($\mathrm{K_d}$) and control input u(t) is expressed as Equation (6).

$$\mathrm{u(t)} = \mathrm{K_p}\left(e(t) + \frac{1}{K_i}\int_0^t e(\tau)d\tau + K_d\frac{de(t)}{dt}\right) \tag{6}$$

3.2. Coprime Factorization

When the transfer function P(s) of the VBS is assumed as a real-rational function, Equation (7) and (8) can be divided into two coprime functions.

$$\mathrm{P(s)} = \mathrm{N(s)M(s)^{-1}} \qquad N(s),\ M(s) \in RH^{\infty} \tag{7}$$

$$\mathrm{P(s)} = \widetilde{\mathrm{M}}\mathrm{(s)}\widetilde{\mathrm{N}}\mathrm{(s)^{-1}} \qquad \widetilde{N}(s),\ \widetilde{M}(s) \in RH^{\infty} \tag{8}$$

where Equation (7) is right coprime factorization and Equation (8) is left coprime Factorization. The transfer function P(s) of VBC (a real rational function) is expressed by real rational gain functions (Equation (7) and (8)) so it can explain internal stability and effectively control P(s), which has unstable zero and pole. Especially, when P(s) is stable,

the right coprime factorization and left coprime factorization become $(\mathrm{P(s)}, \mathrm{I})$ and $(\mathrm{I}, \mathrm{P(s)})$, respectively.

3.2. Controller Parameterization

When P(s), a transfer function of a real rational function VBS, satisfies the Bezout identity, Controller G(s) can be divided into stable rational functions.

Bezout theorem: If there are $\mathrm{X(s)}, \mathrm{Y(s)} \in \mathrm{R}H^{\infty}$ satisfying Equation (9), when $\mathrm{P(s)} \in \mathrm{R}L^{\infty}$, P(s) will be right coprime factorization since $\mathrm{N(s)}, \mathrm{M(s)} \in \mathrm{R}H^{\infty}$ is true. That is, it becomes Equation (10).

$$\mathrm{X(s)N(s)} + \mathrm{Y(s)M(s)} = 1 \tag{9}$$

$$\mathrm{P(s)} = \mathrm{N(s)M(s)}^{-1} \tag{10}$$

Left coprime factorization is also expressed in the same way and X (s) and Y (s) can be estimated by using the Euclidean algorithm generally [16]. All controllers, stabilizing P(s), can be obtained by using the coprime factorization of P(s), which is a transfer function of VBC. The group of these controllers can be expressed through parameterization. The group of all controllers, which stabilize the closed loop feedback system internally, is equal to Equation (11) [16].

$$\left(G(s) \;:\; G(s) = \frac{X(s)+M(s)Q(s)}{Y(s)-N(s)Q(s)} \;:\; Q(s) \in RH^{\infty}\right) \tag{11}$$

If $\mathrm{P(s)} \in \mathrm{R}H^{\infty}$, N(s), M(s), X(s), and Y(s) of Equation (9) can be assumed as P(s), 1, o, and 1, respectively and it becomes equal to Equation (12).

$$\mathrm{G(s)} = \frac{X(s)+M(s)Q(s)}{Y(s)-N(s)Q(s)} = \frac{Q(s)}{1-G(s)Q(s)} \tag{12}$$

In general, Q (s) is a design parameter that is designed with considering the performance and condition. When the sensitivity function S(s) and the complementary sensitivity function T(s) are expressed by the parameterized controller and P(s), a coprime factorized transfer function VPC, they become Equation (13) and (14).

$$\mathrm{S(s)} = \big(1 + \mathrm{P(s)G(s)}\big)^{-1} = M(s)\big(Y(s) - N(s)Q(s)\big) \tag{13}$$

$$\mathrm{T(s)} = \big(1 + \mathrm{P(s)G(s)}\big)^{-1} P(s)G(s) = N(s)\big(X(s) + M(s)Q(s)\big) \tag{14}$$

Therefore, the problem of minimizing the weighted sensitivity becomes equal to Equation (15).

$$\min\|W_1 S(s)\|_{\infty} = \min\big\|W_1 M(s)\big(Y(s) - N(s)Q(s)\big)\big\|_{\infty} \tag{15}$$

3.2. Selection of Parameter $\mathrm{Q(s)}$

The block diagram of the control system with a unity feedback for the VBS control can be expressed as Figure 5. In Figure 5, a transfer function for input and output can be described as Equation (16).

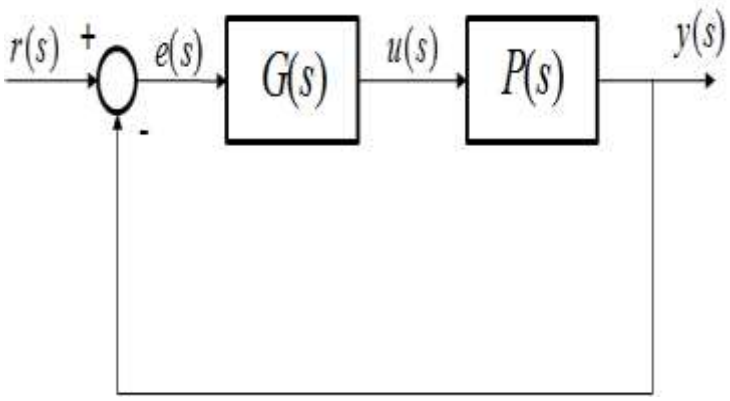

Figure 5. Block Diagram of a Control System with Unity Feedback

$$\frac{\mathrm{y(S)}}{\mathrm{r(s)}} = \frac{P(s)G(s)}{1+P(s)G(s)} \tag{16}$$

where Equation(12) is considered for the PID controller tuning, it can be expressed as Equation (17).

$$\mathrm{Q(s)} = \frac{\mathrm{G(s)}}{1+\mathrm{P(s)G(s)}} \tag{17}$$

One of the difficulties to design a controller in the closed loop feedback control system is that the transfer function of the closed loop is non-linear in the controller G(s). However, it can be expressed as a block diagram (Figure 6), derived from Figure 5 with considering the design parameter Q(s) of Equation (17).

The technique using the design parameter Q(s) is defined as Q Parameterization or Youla Parameterization [17]. Equation (12) can refer to a controller, which has an internally stable feedback system. A design parameter Q(s), which is a stable transfer function in a proper fraction form, can be determined arbitrarily. Therefore, a controller can be designed by selecting Q(s) arbitrarily but Q(s) needs to be determined carefully because the objective of this study was to estimate tuning parameters of the PID controller for controlling VBS. By carefully selecting Q(s), it is possible to reduce the high order of a controller, which is one of the disadvantages of the control method mathematically designed by a controller, to a simple PID controller form parameter. Moreover, if the plant is stable in the proper fraction form, Q(s) can be expressed as Equation (18).

$$\mathrm{Q(s)} = \mathrm{P^{-1}}(s)F(s) \tag{18}$$

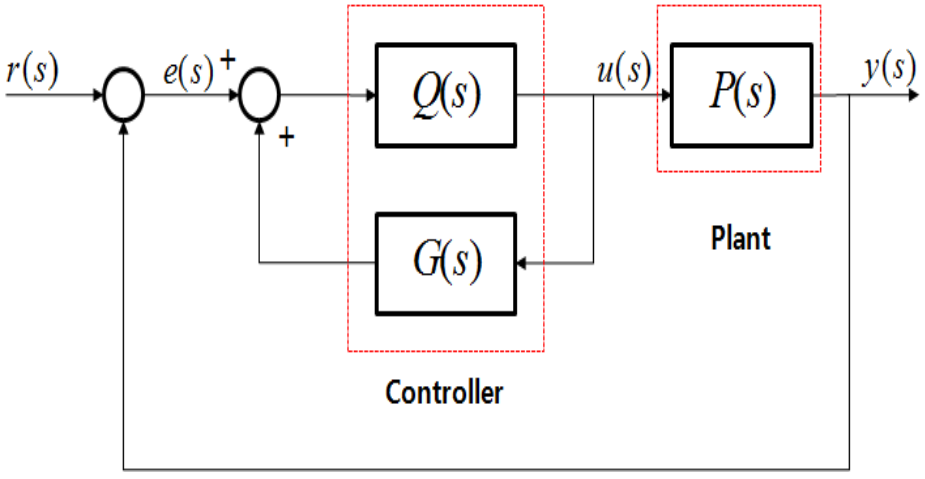

Figure 6. Block Diagram of a Control System with Unity Feedback

where *F(s)* is a desired roll-off function and it is typically chosen as the n[th] order critical damping system.

$$\mathrm{F(s)} = \frac{1}{(\tau s+1)^{\mathrm{n}}}\,, \quad \tau > 1 \tag{19}$$

where n is the relative order of the system, τ is a value minimizing Equation (19), and when $\tau \to 0$, Equation (20) is equal to 0

$$\|Q(s) - F(s)Q(s)\|_{\infty} \tag{20}$$

When the design parameter Q(s) is estimated by using Equation (4) and Equation (19), it is equal to Equation (21).

$$\mathrm{Q(s)} = \frac{\mathrm{S}^2+a}{(bs+c)(\tau s+1)^2} \tag{21}$$

$$\mathrm{a} = \frac{(1-\mathrm{D})^2}{L_F C_{ST}},\ \ \mathrm{b} = \frac{\mathrm{V_T}}{L_F},\ \ c = \frac{(1-D)I_L}{L_F C_{ST}}$$

When the shape of the PID controller for controller VBC is made by using the design parameter Q(s), Equation (17) can be expressed as Equation (22)

$$\mathrm{G(s)} = \frac{\mathrm{Q(s)}}{1-\mathrm{G(s)Q(s)}} = \frac{F(s)G^{-1}(s)}{1-F(s)G^{-1}(s)G(s)} = \frac{F(s)}{1-F(s)}G^{-1(s)} \tag{22}$$

When the gain of the PID controller is obtained from Equation (22), it becomes equal to Equation (23), (24), and (25).

$$\mathrm{K_p} = \frac{\frac{(1-D)^2}{L_F C_{ST}}\tau-\tau^2}{4\tau^2} \tag{23}$$

$$\mathrm{K_i} = \frac{\mathrm{V_T}}{2\tau L_F} \tag{24}$$

$$\mathrm{K_d} = \frac{4\tau^2-4\frac{(1-D)^2}{L_F C_{ST}}\tau^3+\tau^2\frac{(1-D)I_L}{L_F C_{ST}}}{8\tau^3} \tag{25}$$

3.2. Control of VBC

The block diagram of the VBC control system can be shown as Figure 7 and the control consists of two loops.

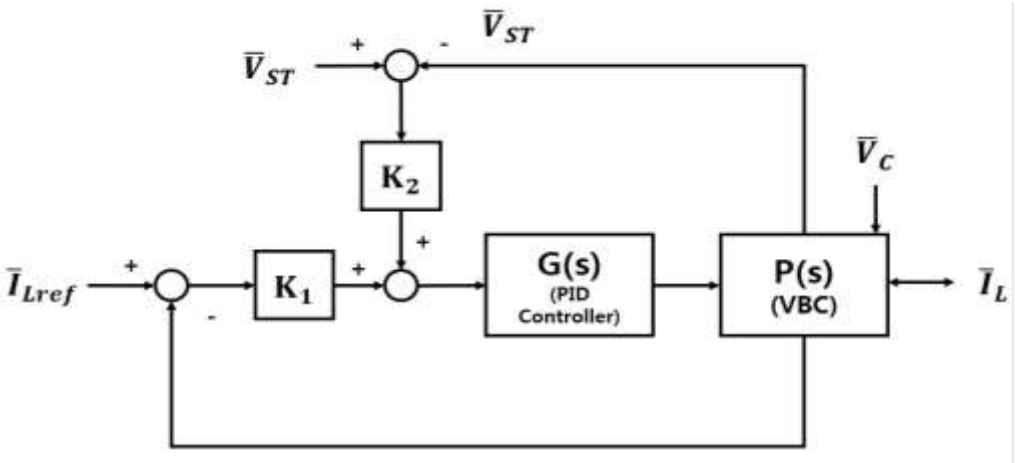

Figure 6. Block Diagram of a VBC Control System

The main loop mitigates the transient state of the DC bus and the auxiliary loop maintains the desired storage voltage. The auxiliary loop maintains can be ignored in Figure 7 because $K_1 \gg K_2$.

4. Simulation

The simulation was executed by using Matlab and parameters are shown in Table 1.

Table 1. Parameters for the Simulation

Parameter	Symbol	Value
Bus Voltage	V_i	270[V]
Inductance of LC Filter	L_S	400[μH]
Capacitance of LC Filter	C_S	50[μF]
Storage Capacitor of the VBC	C_{ST}	100[μF]
Inductance of the VBC	L_F	900[μH]
Capacitance of the VBC	C_F	1.2[μF]
Rated Pulsed Load		3[kW]
Switching Frequency		20[kHz]

$B_r(\omega)$, a barrier for command following and disturbance rejection for the internal stability, and $B_n(\omega)$, a barrier for reducing sensor noise and modeling error, are defined as Table 2.

Table 2. Frequency Domain Specification Design

Barrier		Boundary Frequency
$B_r(\omega)$	$m_r = 40dB$	$\omega \leq 1$
	0	$\omega > 1$
$B_n(\omega)$	0	$\omega \leq 400$
	$e_{max}^{-1} = 10/\omega$	$\omega > 400$

Figure 7 shows the changes of loop shapes according to parameter τ of the roll-off function F(s) in the design parameter Q (s) of the PID controller.

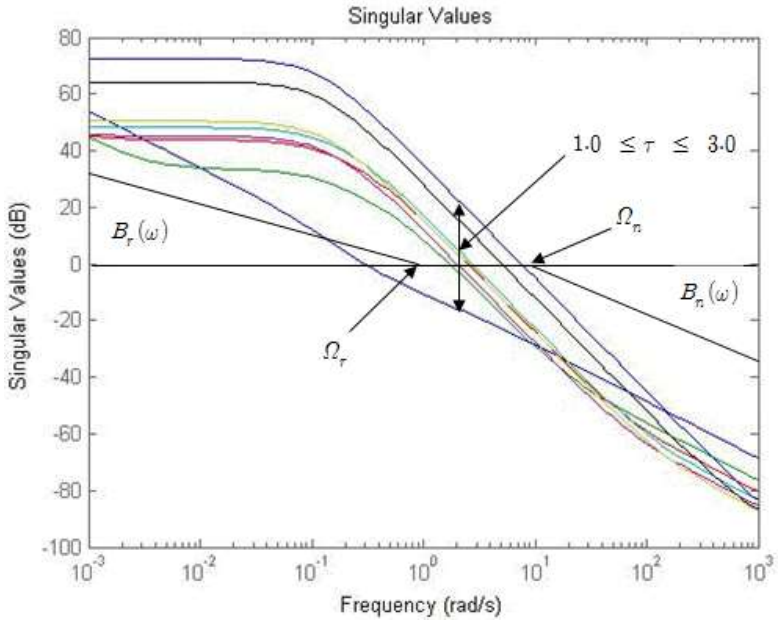

Figure 7. Changes of Loop Shapes According to the Parameter τ Setting

Figure 7 reveals that $B_n(\omega)$, a barrier for reducing sensor noise and modeling error, $B_r(\omega)$, a barrier for command following and disturbance rejection for the internal stability, were not invaded when violated when the parameter τ of the PID controller was 3.0≥ and ≥1.5. As the value closer to the intermediate boundary was chosen, the loop shape of the VBC control system was farther away from the barrier $B_r(\omega)$ in the high-frequency range and the barrier $B_n(\omega)$ in the low-frequency range to improve the performance of response. Therefore, when the parameter τ is set to 1.8, the PID control parameters can be estimated (Table 3). In Figure 6, gain K_1 of the main loop was set as 1 and K_2 of the auxiliary control loop was set as 0.06. The results of step response are shown in Table 4.

Table 3. PID Controller Design Parameters

Control Parameter	K_p	K_i	K_d
	41.30	40.56	0.08

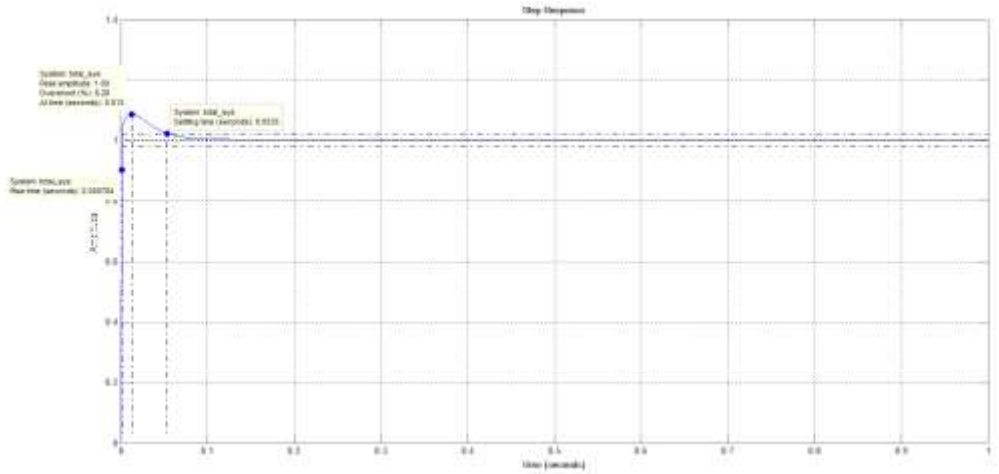

Figure 8. Step Response of the VBC Control System

Table 4. Performance of the VBC Control System against Step Response

Overshoot	Setting Time	Rising Time
0.0535	8.28%	0.000784

The setting time, overshoot, and rising time (Figure 8 and Table 4) indicated that the method proposed by this study was excellent.

5. Conclusion

This study designed a voltage-type PID controller in order to stabilize the instability of DC distributed power system. The study obtained satisfying results (rising time, overshoot, and setting time) by designing a PID controller assuring robustness, stability, and internal stability and designing an analytical and sophisticated PID controller.

Acknowledgments

This study was funded by MOTIE, Korea, under the "Regional Specialized Industry Development Program (R0006062)" supervised by KIAT.

References

[1] C. C. Heath, "The Market for Distributed Power System", Applied Power Electronics Conference and Exposition 1991, APEC'91, Conference Proceedings 1991, 6th Annual IEEE, **(1991)**, pp. 225-229.
[2] W. A. Tabisz, M. M. Jovanovic and F. C. Lee, "Present and Future of Distributed Power Systems", Applied Power Electronics Conference and Exposition 1992, APEC'92 Conference Proceedings **(1992)**, 7th Annual IEEE, **(1992)**, pp. 11-18.
[3] J.-S. Lai and D.J. Nelson, "Energy Management Power Converter in Hybrid Electric and Fuel Cell Vehicles", Proceedings of the IEEE, vol. 95, no. 4, **(2007)**.
[4] S, Luo, "A Review of Distributed Power Systems, part I:DC Distributed Power System", aerospace and Electronic Systems Magazine, IEEE, pp. 5-16.
[5] B. Mammano, "Distributed Power Systems", in Proceedings of Unitrode Power Supply Design Seminar (SEM-900), **(1993)**, pp. 1-11.
[6] A. Emadi, A. Khakigh, C. H. Rivetta and G. A. Williamson, "Constant Power Loads and Negative Impedance Instability in Automotive Systems: Definition, Modeling, Stability, and Control of Power Electronic Converters and Motor Drives", IEEE Transactions on Vehicular Technology, vol. 55, no. 4, **(2006)**.
[7] S. V. Mollov, and J.D. LA, "Study of control algorithms for a voltage bus conditioner", Vehicle Power and Propulsion 2005 IEEE Conference, **(2005)**, pp. 372-378.
[8] C. D. Scott and R. E. Smalley, "Diagnostic Ultrasound: Principles and Instruments", Journal of Nanosci. Nanotechnology, vol. 3, no. 2, **(2003)**, pp. 75-80.
[9] R. E. Kalman, "A New Approach to Linear Filtering and Pridiction Problems", Trans. of the ASME, Journal of Basic Eng, vol. 82, **(1960)**, pp.35-45.
[10] R. E. Kalman, "Contributions to the Theory of Optimal Control", Bol. Soc. Mat. Mex., vol. 5, **(1960)**, pp.102-119.
[11] G. Stein and J. Doyle, "Robustness with Observers", IEEE Trans. On Auto. Control, AC-24, **(1979)**, pp. 607-611.
[12] J. Doyle, K. Glover and P.P. Khargonekar and B.A. Francis, "State space solutions to standard H^2 and H^∞ control problems", IEEE Trans. Auto. Control, AC-34, **(1989)**, pp. 831-847.
[13] K. J. Astrom and K. J. Hagglund, "PID Controllers: Theory, Design, and Tuning, 2nd ed. Research Triangle Park, NC: ISA, **(1995)**.
[14] A.J. Forsyth and S.V. Mollov, "Modeling and control of DC-DC converters", IEEE Power Engineering Journal, **(1998)**, pp. 229-236.
[15] J.M. Maciejowski, "Multivariable Feedback Design", Addison-Wesley, 1989
[16] Doyle, J. C., B. A. Francis, A. R. Rannenbaum, Feedback Control Theory, Maxwell MacMillan International Editions, **(1992)**.
[17] M. Morari, and E. Zarifiou, "Robust Process Control", Prentice-Hall, Englewood Cliffs, N.J., **(1989)**.

Authors

Houngkun Joung, he received the BS degrees in the electrical engineering from Semyung University, Seoul, Korea, in 2002. and the MS and PhD degrees in the electrical engineering from Hanyang university, Seoul, Korea, in 2004, 2017 respectively. He is a adjunct professor in the mechanical & automotive engineering, Hanyang Cyber University from 2017.

Sangmin Lee, he received the BS and MS and PhD degrees in the electronics engineering from Chungbuk National University, Changju, Korea, in 2002 and 2010 and 2018 respectively. He is a engineer EMC(electromagnetic compatibility) and reliability evaluation at ChungbukTechnopark from 2005. His scientific interests are focused on the electromagnetic compatibility and reliability evaluation technology the guideline standard.