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A Two-Stage Cascaded Multi-Level Inverter

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Abstract

The cascaded H-bridge multi-level inverter has been extensively applied to middle-high voltage and high power fields, but it has disadvantages of numerous DC voltage sources and switch tubes. Based on this reason, this paper presents a two stage cascaded multilevel inverter. The preceding stage is composed of several basic modules through cascading, and the backward stage is H-bridge inverter. The direct voltage use ratio of every basic module in this inverter is increased by 2 times, and the number of DC voltage sources and switch tubes is reduced effectively. In addition, H-bridge at the backward stage operates under power frequency conditions only, which can further reduce the switching loss. According to the new type of inverter, this paper proposes carrier cascading modulation and hysteresis control method combining. The cascaded multilevel inverter can output a variety of level. Finally, simulation model of the inverter is built up, the input and load jump of the two working modes are simulated and analyzed. The performance of the proposed inverter are verified by simulation.

Keywords*: Multi-Level inverter; Cascade; Carrier Disposition; Voltage utilization*

1. Introduction

At the high power application site, such as combination of photovoltaic power generation, wind power generation, and new energy power generation, the multi-level inverter is becoming a mainstream choice by providing good big voltage and large current[1, 2]. Compared with two-level inverters, the devices of multi-level inverter possess small stress, which has effectively increased the power level. Under the same switching frequency, the harmonic distortion rate is reduced, and the quality of output waveform is increased. Besides the above advantages, the cascaded multi-level inverter is characterized by modularization and easy extension, but the high number of DC voltage sources and switch tubes has restricted its application in industry[3-5].

The traditional cascaded H-bridge multilevel inverter outputs 2N+1 levels, requiring N DC input sources and 4N switch tubes[6-7]. By directing at the high number of switch tubes in cascaded H-bridge topology, related experts have proposed a new topological structure literature, which has reduced the number of switch tubes by half[8]. Besides, the cascaded H-bridge multilevel topology is improved in many aspects. The number of switch tubes is reduced to a certain extent, but the number of conductive switch tubes is not decreased. And researchers have turned the switch number almost reduced to 1/4, and only three switch tubes are conductive at any time, but the number of DC voltage sources remains unchanged[9]. The diode-clamped, flying capacitor and hybrid cascaded multi-level inverter has reduced the number of DC voltage sources to a certain extent, but will increase the number of switch tubes.

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In order to overcome the above problems, this paper puts forward a cascaded multi-level inverter by setting three-level module as the basic unit, which has reduced the number of DC voltage sources by half and almost decreased the number of switch tubes by half.

2. Topology of Multilevel Inverter

2.1. Multi-level DC/DC Convertor

The basic modules of cascaded multi-level DC/DC convertor are presented in Figure 1(a), and it is composed of 1 input voltage source V_{in} ($V_{in}=V_{dc}$), 2 DC-link capacitors (C_1 and C_2), 2 diodes (D_1 and D_2), 2 capacitance charge-discharge control switches Q_1 and Q_2 (unidirectional switches), and 3 level selection switches S_0, S_1 and S_2 (bidirectional switches). According to Figure 1(a), Q_1 and Q_2 cannot be conductive at the same time, otherwise, short-circuit fault will happen to the input voltage source. In addition, only one switch in S_0, S_1 and S_2 can be conductive at the same time, otherwise, short-circuit fault will happen to capacitors C_1 and C_2.

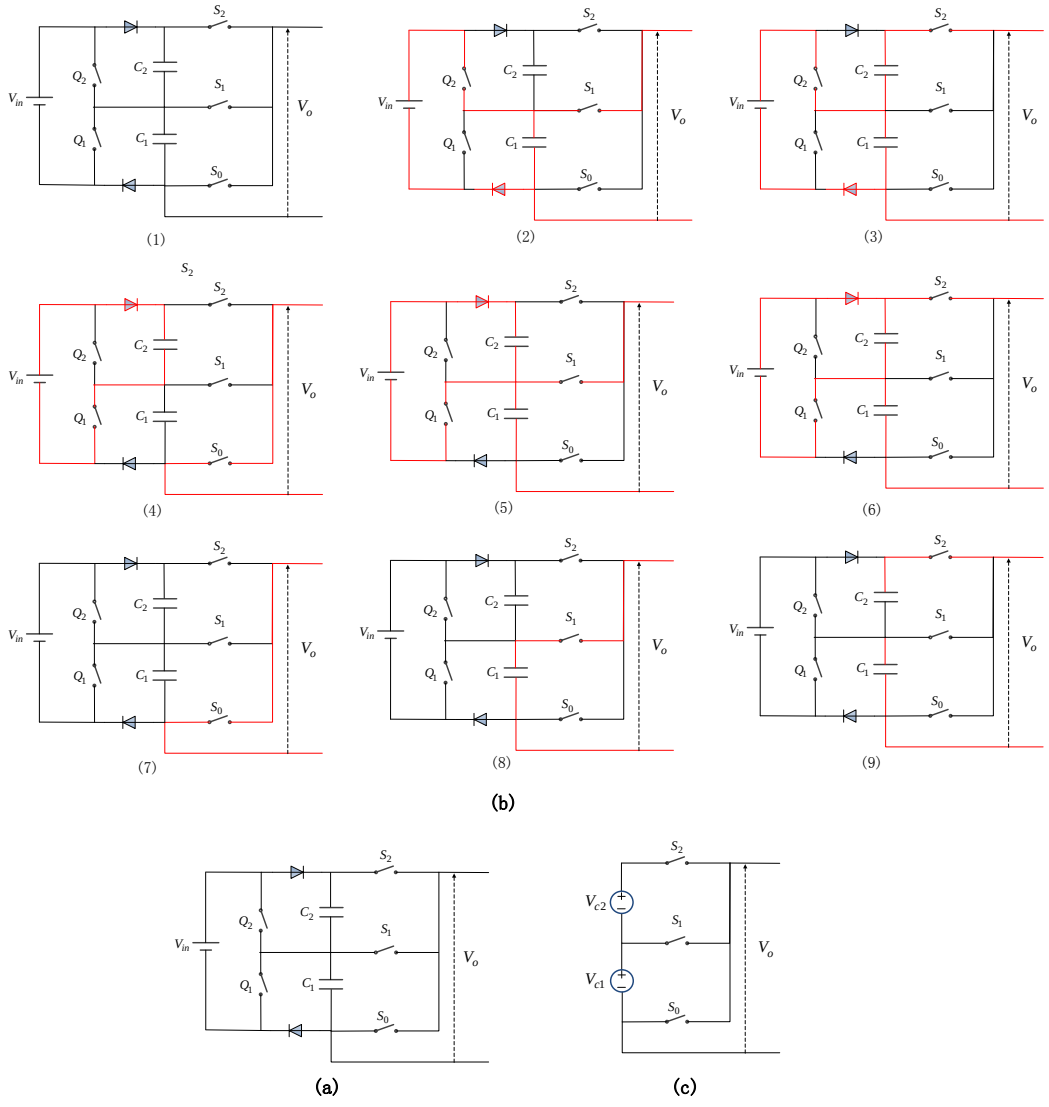


Figure 1. Basic Module Working State

Figure 1(b) gives 9 operating states of basic modules, and the 9 operating states of basic modules are elaborated in the following:

Mode 1: Q_1, D_2 and S_0 are conductive, and other switches are cut off. At this time, capacitor C_2 is in a charging state. $V_{c2}=V_{in}=V_{dc}$; $V_o=0$.

Mode 2: Q_1, D_2 and S_1 are conductive, and other switches are cut off. At this time, capacitor C_2 is in a charging state. $V_{c2}=V_{in}=V_{dc}$; $V_o=V_{c1}=V_{dc}$.

Mode 3: Q_1, D_2 and S_2 are conductive, and other switches are cut off. At this time, capacitor C_2 is in a charging state. $V_{c2}=V_{in}=V_{dc}$; $V_o=V_{c1}+V_{c2}=2V_{dc}$.

Mode 4: Q_2, D_1 and S_0 are conductive, and other switches are cut off. At this time, capacitor C_1 is in a charging state. $V_{c1}=V_{in}=V_{dc}$; $V_o=0$.

Mode 5: Q_2, D_1 and S_1 are conductive, and other switches are cut off. At this time, capacitor C_1 is in a charging state. $V_{c1}=V_{in}=V_{dc}$; $V_o= V_{c1}=V_{dc}$.

Mode 6: Q_2, D_1 and S_2 are conductive, and other switches are cut off. At this time, capacitor C_1 is in a charging state. $V_{c1}=V_{in}=V_{dc}$; $V_o= V_{c1}+V_{c2}=2V_{dc}$.

Mode 7: S_0 is conductive, and other switches are cut off. At this time, capacitors C_1 and C_2 are in a discharging state. $V_{c1}=V_{in}=V_{dc}$; $V_o=0$.

Mode 8: S_1 is conductive, and other switches are cut off. At this time, capacitors C_1 and C_2 are in a discharging state. $V_o= V_{c1}=V_{dc}$.

Mode 9: S_2 is conductive, and other switches are cut off. At this time, capacitors C_1 and C_2 are in a discharging state. $V_o= V_{c1}+V_{c2}=2V_{dc}$.

According to Figure 1(b), when the switching period T of Q_1 and Q_2 is small, $V_{c1}=V_{c2}=V_{in}=V_{dc}$, and the equivalent circuit of basic modules is shown in Figure 1(c). Table 1 shows the relation between the output voltage V_o of basic modules and switching state of S_0, S_1 and S_2 under different operating states. According to Table 1, basic modules have three level outputs: 0, V_{dc} and $2V_{dc}$.

Table 1. Switching state

S_0	S_1	S_2	V_o
1	0	0	0
0	1	0	V_{dc}
0	0	1	$2V_{dc}$

For every basic module, the switch function S_i is defined, as shown in formula (1):

$$S_i = \begin{cases} 1, & switch\ on \\ 0, & switch\ off \end{cases} \quad (i = 0,1,2) \tag{1}$$

The output levels of basic modules can be unified into:

$$V_o = i \cdot V_{dc} \ if\ S_i = 1 \quad for\ i = 0,1,2 \tag{2}$$

The typical output waveform of basic modules in one period can be worked out according to formulas (1) and (2), as shown in Figure 2.

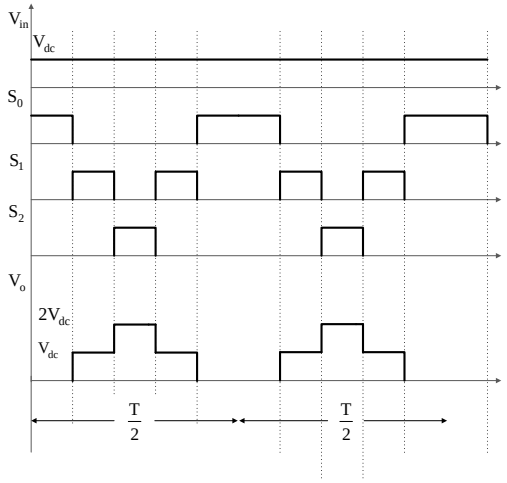


Figure 2. Output Waveform of Basic Modules in One Period

The topological structure of cascaded multi-level DC/DC convertor can be gained through cascading of several modules, as shown in Figure 3. It's worth noting that the total output voltage of multi-level DC/DC convertor is the sum of the output voltages of all basic modules.

$$V_o(t)=V_{o,1}(t)+ V_{o,2}(t) +V_{o,3}(t)+\cdots\cdots+ V_{o,n}(t) \tag{3}$$

If $V_{in,j}=V_{dc}$(j=1,2,……， n), the following formula can be gained according to formula (2)

$$V_o(t) = (i_1 + i_2 + i_3 + \cdots + i_n) \cdot V_{dc} = V_{dc} \cdot \sum_{j=1}^{n} i_j \tag{4}$$

i_j represents the quantity of levels output by basic module j, and it meets the following formula:

$$i_j = \begin{cases} 2, & if\ S_{2,j} = 1 \\ 1, & if\ S_{1,j} = 1 \\ 0, & if\ S_{0,j} = 1 \end{cases} \quad for\ j = 0,1,2\cdots n \tag{5}$$

Therefore, the maximum output voltage of multi-level DC/DC convertor is $V_{omax}=2n\cdot V_{dc}$. The maximum quantity of levels output is 2n, and levels of any quantity in 0-2n can be output.

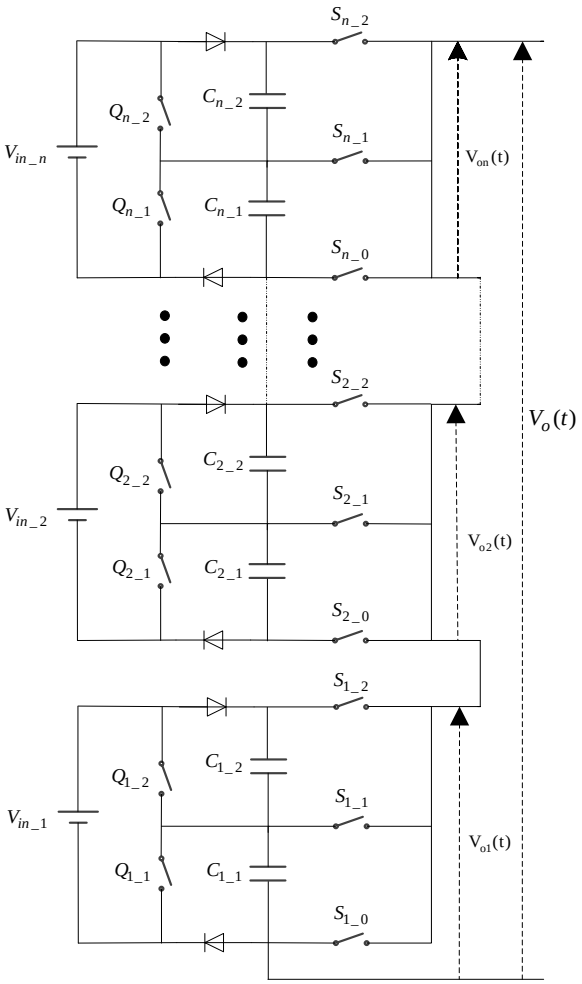


Figure 3. Cascaded Multi-Level DC/DC Convertor

2.2. Cascaded Multi-level Inverter

Through the series connection of an *H*-bridge to the output end of multi-level DC/DC convertor presented in Figure 3, we can form a cascaded multi-level inverter, as shown in Figure 4. The switching states of 4 switch tubes at *H*-bridge decide the direction of load voltage V_l. Table 2 displays the relation between V_o and V_l under 4 switching states of *H*-bridge. The following conclusions can be gained easily according to Table 2. When H_1 and H_3 are conductive, and H_2 and H_4 are cut off, V_l has the same direction with V_o. When H2 and H4 are conductive, and H1 and H3 are cut off, V_l and V_o present a reverse direction. Figure 5 shows the common waveform of 7-level inverter composed of 3 modules. Within the period 0-0.5T, V_l=Vo; within the period 0.5T-T, V_l=-Vo.

$$|V_l| = V_o \tag{6}$$

$$V_l = \begin{cases} +V_o, & if\ H_{1,3}\ on, H_{2,4}\ off \\ -V_o, & if\ H_{2,4}\ on, H_{1,3}\ off \end{cases} \tag{7}$$

Table 2. Switching States of the Cascaded Multi-Level Converter

H_1	H_2	H_3	H_4	V_l
1	0	0	1	$+V_o$
0	1	1	0	$-V_o$
1	0	1	0	0
0	1	0	1	0

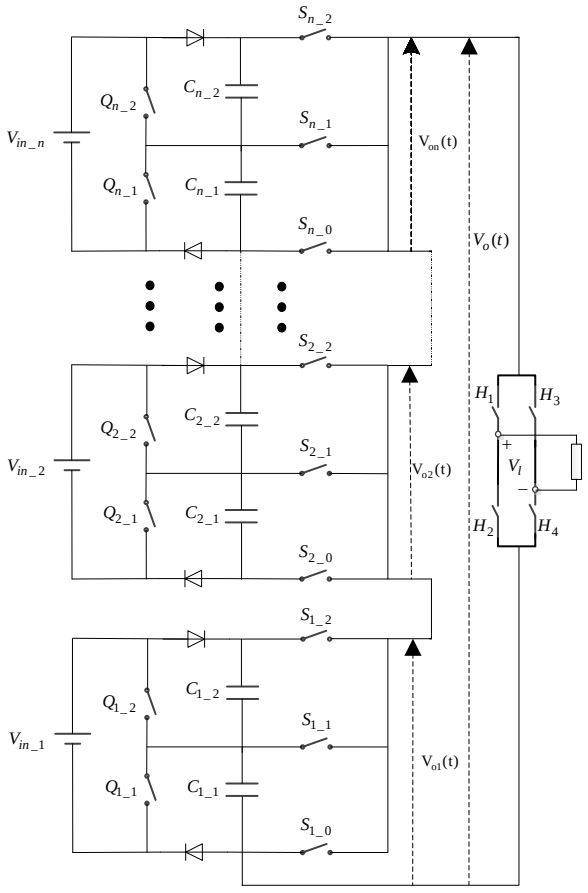


Figure 4. Two-Stage Cascaded Multi-Level Inverter

3. Modulation Strategy

The two-level *H*-bridge carrier phase-shift modulation technique has already been quite mature, but it cannot be directly applied to the inverter proposed in this paper. The quantity of output levels of basic modules is 3, so the modulation method of combining laminated carrier modulation with carrier phase-shift modulation is adopted in this paper.

1) Laminated carrier modulation is adopted in the single module;

2) The carrier phase-shift modulation is adopted between the modules.

3.1. Laminated Carrier Modulation

The control signal of a single basic module is shown in Figure 5. A comparison is made between the values of carrier signal and reference signal Vref via the comparator. Moreover, the comparison results are recorded as C_a and C_b. The waveform of output voltage V_0 can be drawn according to C_a and C_b. And then the drive signals of switching

devices S_0, S_1 and S_2 are determined via switch function (8). It's worth noting that basic modules only output zero or positive levels, so if the reference signal shows negative half-cycle, the absolute value should be taken before it is compared with the carrier wave. In this way, the quantity of carrier waves can be reduced by half.

$$\begin{aligned} S_0 &= \overline{C_b} \\ S_1 &= \overline{C_a} \cdot C_b \\ S_2 &= C_a \end{aligned} \tag{8}$$

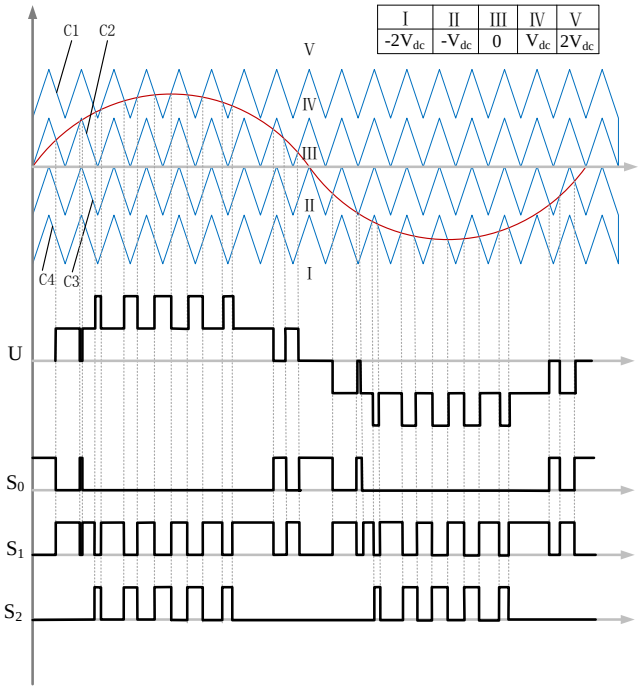


Figure 5. Laminated Carrier Modulation Strategy

3.2. Carrier Phase-Shift Modulation

Suppose that the number of modules is n. Then the carrier phase angle difference of every module is 360°/n. The carrier wave of module j is defined as $C_{a,j}$ and $C_{b,j}$. Then the initial phase angles of $C_{a,1}$, $C_{a,2}$, $C_{a,3}$……$C_{a,n}$ are 0, 360°/n, 720°/n……360° respectively; $C_{b,j}$ has the same initial phase angle as $C_{a,j}$. Therefore, the drive signal of basic module j is as follows:

$$\begin{aligned} S_{0,j} &= \overline{C_{b,j}} \\ S_{1,j} &= \overline{C_{a,j}} \cdot C_{b,j} \\ S_{2,j} &= C_{a,j} \end{aligned} \tag{9}$$

3.3. Q1 and Q2 Control Strategy

Under the influences of circuit parameter and load jump, voltage unbalance will happen to the tandem split capacitors in DC-link during the operation process. As a result, the harmonic distortion rate will increase, and the output waveform quality will deteriorate. By adding *PI* control into the preceding-stage circuit, we can realize capacitor voltage balance. By taking C_1 and C_2 in Figure 1 as an example, when the voltage of capacitor C_1 is higher than that of C_2, Q_2 is cut off, Q_1 is conductive, C_1 discharges to reduce the voltage, and meanwhile C_2 charges to increase the voltage. When the voltage of capacitor C_1 is lower than that of C_2, Q_1 is cut off, Q_2 is conductive, C_1 charges to increase the

voltage, and meanwhile C_2 discharges to reduce the voltage. The above process is repeated continuously, to guarantee the dynamic equilibrium of voltage between C_1 and C_2. The block diagram for capacitor voltage balance control is shown in Figure 6.

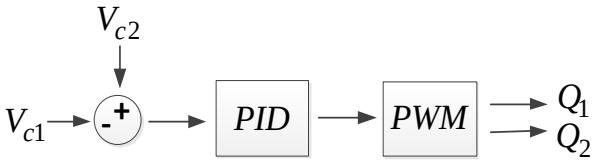


Figure 6. Capacitor Voltage Balance Control Block

4. Performance Analysis

4.1. Voltage Stress

According to Figure 1, $V_{Q1stress}= V_{Q2stress} =V_{dc}$. The voltage stress of S_0, S_1 and S_2 is related to the operating modes. When S_0 is conductive, and S_1 and S_2 are cut off, $V_{s1stress}=V_{dc}$ and $V_{s2stress}=2V_{dc}$. When S_1 is conductive, and S_0 and S_2 are cut off, $V_{s0stress}=V_{dc}$ and $V_{s2stress}=V_{dc}$. When S_2 is conductive, and S_0 and S_1 are cut off, $V_{s0stress}=2V_{dc}$ and $V_{s1stress}=V_{dc}$. Therefore, $V_{s0stress}=V_{s1stress}=V_{s2stress}=2V_{dc}$.

4.2. Direct Voltage Use Ratio

The five-level inverter of a single module is carefully compared with diode-clamped five-level inverter. Under every operating mode, short circuit is used to replace switch conduction, and open circuit is used to replace cutoff state. It is discovered that they almost have the same simplified circuit. As for the sole difference, the former realizes inversion through *H*-bridge, while the latter realizes inversion by setting a neutral point in the middle of split capacitors in DC-link. Therefore, the number of capacitors of the former is half of the number of split capacitors owned by the latter. Let the capacitor voltage of the two be equal to each other. Then the five-level inverter proposed can be equivalently replaced by a diode-clamped five-level inverter. When laminated carrier modulation is adopted, the input-output relation of diode-clamped five-level inverter is shown in formula (8):

$$V_0 = \frac{1}{2} MV'_{in} \tag{10}$$

In the formula, V_o is the peak value of output voltage after *LC* filter; *M* means the modulation ratio; V'_{in} represents the DC input voltage source of the equivalent diode-clamped multi-level inverter; the number of split capacitors in DC-link is 4; the terminal voltage is V_c, and $V'_{in} = 4V_c$.

When carrier modulation is adopted for the five-level inverter proposed, the input-output relation is shown in formula (9):

$$V_o = \frac{1}{2} MV'_{in} = \frac{1}{2} M \cdot 4V_c = 2MV_c \tag{11}$$

In the formula, V_{in} means the DC voltage source of the five-level inverter proposed, and $V_{in} = V_c$. According to formulas (10) and (11), compared with the diode-clamped five-level inverter, direct voltage use ratio of the five-level inverter proposed is improved from *0.5M* to *2M* by 3 times. When the duty ratio and output voltage peak are consistent, input voltage of the latter is only 0.25 times the voltage of the former. When the input voltage is the same, the maximum output voltage of the latter is 4 times the voltage of the former. Therefore, the five-level inverter proposed has effectively improved the direct voltage use ratio, and expanded the input and output range.

4.3. Number of Devices

A comparison is made with *H*-bridge cascaded multi-level inverter, the new-type cascaded inverters proposed in literature [8] and literature [9] in the number of DC voltage sources and switch tubes, as shown in Table 3. According to Table 3, the number of DC voltage sources owned by the cascaded topology proposed is half of that possessed by the other three topological structures, and the number of switch tubes is almost half of that possessed by *H*-bridge cascaded multi-level inverter.

Table 3. Comparison of Number of Switches and DC Voltage Sources Needed for Different Output Voltage Level

	Number of DC voltage sources				Number of switch tubes			
Quantity of output levels	Cascaded *H*-bridge	Literature 8	Literature 9	Topology proposed	Cascaded *H*-bridge	Literature 8	Literature 9	Topology proposed
5	2	2	2	1	8	8	7	9
9	4	4	4	2	16	12	9	13
13	6	6	6	3	24	16	11	17
17	8	8	8	4	32	20	13	21
21	10	10	10	5	40	24	15	25
…	…	…	…	…	…	…	…	…
4N+1	2N	2N	2N	N	8N	4N+4	2N+5	4N+5

5. Simulation Analysis

A new-type cascaded 9-level inverter simulation platform is established in MTALBA/Simulink, and it is obtained through cascading of two basic modules. Let the input voltage of all modules be equal to each other; the remaining circuit parameters are determined according to Section 3.2. Table 4 shows the open-loop simulation results under different input and modulation ratios. Table 5 gives the simulation results of PI control for voltage effective values. Figure 8 presents the waveform of closed-loop simulation when the input voltage is 90V.

According to Table 4 and Table 5, the simulation results have a certain deviation from the theoretical values. The voltage of diode and switch tube will drop under conduction, so such deviation is deemed as reasonable. Besides, *THD* is within 1%. Therefore, the laminated carrier modulation technique mentioned in 3.2 can meet modulation requirements of the new-type cascaded multi-level inverter. In Figure 7 (b), the output voltage becomes stabilized after 0.35s, and the modulation time is too long. If load disturbance or power disturbance happens at the same time, the output waveform effect will become poorer.

Table 4. Open-Loop Simulation Results of Different Input and Modulation Ratio

V_{in}	M	Theoretical V_o/V	Simulated V_o/V	THD
50	0.6	120	116.1	0.6%
75	0.65	195	189.4	0.54%
100	0.7	280	275.5	0.65%
110	0.707	311	303.1	0.54%

Table 5. Closed-Loop Simulation Results of Different Input

V_{in}	Theoretical V_o/V	Simulated V_o/V	THD
50	120	118.3	0.94%
75	195	192.1	0.84%
100	280	272.3	0.61%
110	311	304.9	0.59%

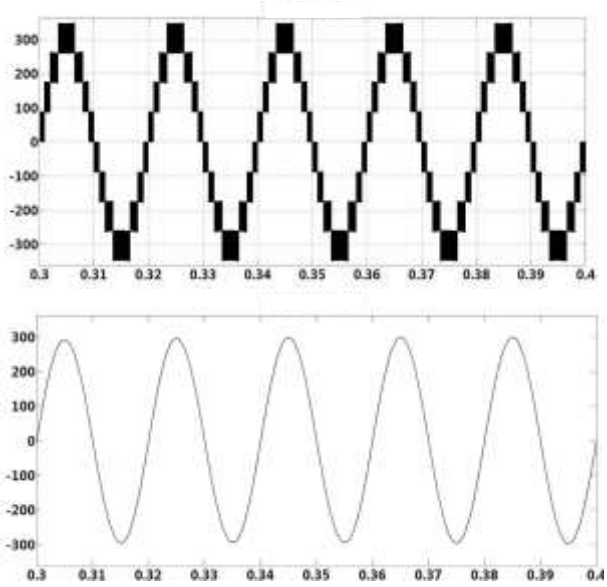
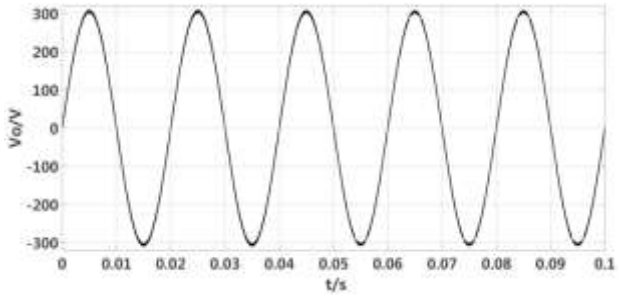


Figure 7. Closed-Loop Output Voltage Before and After LC Filter when Input 90V

In order to restrain load disturbance or power disturbance, hysteresis control and capacitor voltage PI control are used to improve the dynamic properties of cascaded 9-level inverter. Figure 8 to Figure 10 show the output voltage and inductor current waveforms when power source jumps from 120V to 100V under constant load, load jumps from 11 Ω to 20 Ω under constant power source, and power source and load jump at the same time. The jumping time is t=0.04s. According to Figure 8 – Figure 10, the new-type cascaded multi-level inverter possesses very good dynamic response after hysteresis control.



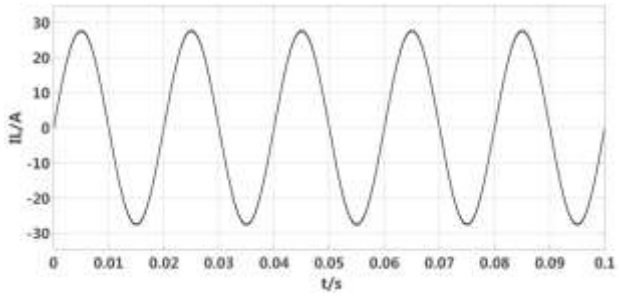


Figure 8. Output Voltage and Inductor Current when Input Jumps

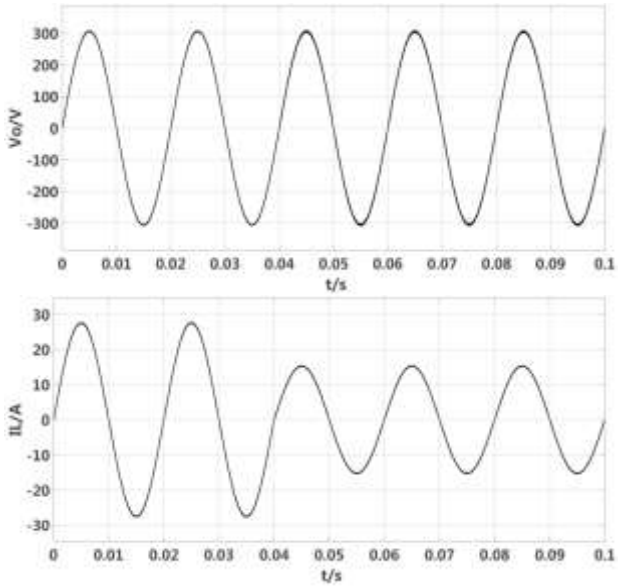


Figure 9. Output Voltage and Inductor Current when Load Jumps

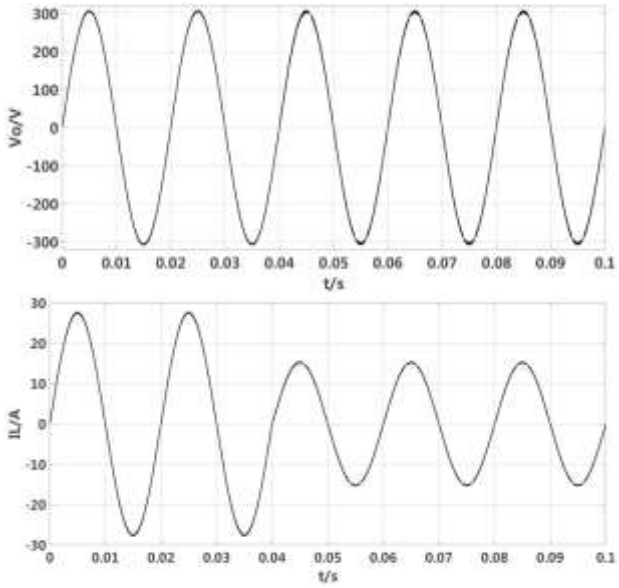


Figure10. Output Voltage and Inductor Current when Input and Load Jump at the Same Time

6. Conclusions

Compared with the diode-clamped inverter, the five-level inverter proposed increases its direct voltage use ratio by 3 times, and it is easy to realize capacitor voltage balance. As for the cascaded multi-level inverter based on the five-level inverter proposed, the number of voltage sources is reduced by half, and the number of switch tubes is also greatly decreased. Hence, the loss is reduced, and cost is saved. Laminated carrier modulation and hysteresis control can realize modulation and control for the cascaded multi-level inverter proposed well.

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