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Multi Loop Controllers for Single Inductor Multiple Output Dc-Dc Buck Converters: A Comparative Study

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Abstract

The paper compares various control algorithms used as a multi loop control structure with a view to enhance the load and line regulatory characteristics for a Single Inductor Multiple Output (SIMO) dc-dc converter. SIMO converters fulfill to offer a power supply with different voltage and current levels suitable for use in portable electronics. The theory allows the advantages of reduction in cost and size due to the presence of single inductor associated with the systems but experiences a disadvantage in terms of cross regulation between the different outputs when the load conditions change. The formulation evolves the philosophy of using the principles of Error Compensator, PID controller, Fuzzy tuned PID controller and Sliding Mode Controller (SMC) individually through a multi loop schematic to improve the time response specifications of the system and provide a regulated output over a wide range of operating loads. The test results obtained using DT9834 Data Acquisition Module (DAQ) based hardware validates the simulated response and reveals that the SMC outperforms the others controllers. The performance of the converter opens up a new dimension to the use of the utilities in the domestic world and corner greater milestones for the electronic industry.

Keywords*: Single Inductor Multiple Output (SIMO) DC-DC converter, PID, Fuzzy Tuned PID, Error Compensation, Sliding Mode Controller, Cross Regulation*

1. Introduction

The portable electronics applications continue to be the major consumer product of the present world powered by single or multiple cell Lithium based batteries. These gadgets require different voltage-current levels for operating different subsystems. Each subsystem is usually powered by individual power converter with the power device designed for high efficiency [1]. The real estate of the present Printed Circuit Boards (PCB) is a scarce resource and the inductor in each power switching device is bulky and accounts for a higher overall loss for the converter. Besides, the presence of multiple inductors reduces the reliability of the power converter system [2]. A power supply with different voltage and current levels invites attention and Single Inductor Multiple Output (SIMO) system allows the advantages of reducing the number of bulky inductors, capacitors and controllers associated with the system [3]. The advantages of SIMO are reduced cost, size and volume, small form factor and increased efficiency if Low Drop Outputs (LDOs) are replaced with switching converters [4]. However, the above merits come with an added constraint of cross regulation which is the effect of change in line and load variation of one output to the others. Therefore a SIMO converter necessitates

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addressing load and line variations with fast transient response along with less cross regulation between the outputs [5].

The converter can be operated in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) or Pseudo Continuous Conduction Mode (PCCM) of operation and each mode inherit their own advantages, disadvantages and limitation of handling load current. The PCCM mode can handle large loads with small ripple and provide independent control of the outputs [6]. The DCM mode on the other hand cannot handle loads with higher currents and further produces large ripple current. The ripple phenomenon reduces the overall efficiency of the system. In DCM mode, the inductor current reaches and stays constant at zero at the end of each switching cycle which will help to avoid the cross regulation between the outputs[7]. In this paper CCM mode is used due to high current loads seen in the target application of portable electronic gadgets but reducing the cross regulation effect is a challenging task.

2. Literature Review

Simple Control Scheme is needed but not at the expense of performance. The dc-dc SIMO converter designed and analyzed are nonlinear and used for applications with low voltage and current in milliWatts to Watts. The converter considered in this paper undergoes large perturbations. Various control algorithms are used in literature and a summary of the techniques will help in choosing the suitable controller for the proposed SIMO converter. The use of time multiplexed control can be seen as two independent DCMs in which there is a freewheeling state of inductor current when distributing energy from one channel to another thus being able to distinguish two outputs but 3% ripples are seen and losses are increased due to the presence of freewheel switch. The energy dissipation seen in time multiplexed control [8], when used for heavy loads brings in large peak inductor currents which in turn increases the ripples and leads to decrease the efficiency. The digital control algorithms based on the output voltages or inductor current as seen in [9] have been developed to make the SIMO converters work with less cross regulation and robust to load/line variations. However the digital controllers are complex and need extra sensing devices along with A/D and D/A converters. The compensators are designed with the help of the ripple based mathematical model of the system [10] to suppress the cross regulation between the outputs but 5 % ripple is seen in the outputs. Some authors [11] ,instead of using the advanced control and high switching frequency, parallel structured hybrid SIMO power converter is developed with active current compensation technique to minimize the cross regulation. Since the linear regulators equal to the number of outputs are added along with SIMO switching power converter which will increase cost and switching losses of the system. In [12] sliding mode controller have successfully designed for SIMO power converter .However these techniques are restricted to dual output and not extended to more than two. To achieve the good regulation performance over wide load and voltage ranges with fewer ripples, the Relative Skip Energy Control (RSEC) [13] is used to make the converter to work in either Continuous Conduction Mode or Green Mode. Bang-Bang Zeroth-Order Control [14], Adaptive Gate Biasing [15], Output Independent Gate Drive Control [16] and Error-Based Controller [17] are developed for the SIMO DC-DC converter to obtain the high efficiency, compact area and less ripples. However, the above methods are not using any specific linear and nonlinear controller and these algorithms are again complex and need extra circuits.

Considering the requirement and understanding the limitations of various controllers discussed above, Error compensator, PID controller, Fuzzy Logic Controller and Sliding Mode Controller are designed. Simulation studies to reduce the cross regulation effect and ripples in the output voltage using these controllers are carried out. Cross regulation means the percentage change in one output voltage due to the change in the load current in another output. Ripples mean the superimposition of AC voltage waveform on the dc

output voltage of the converter. The results obtained are validated by using Data Acquisition Module® DT 9834. From the study, it is established that sliding mode control based system performs better than other control schemes suggested in this paper.

3. Problem Definition

The main attempt owes to develop a multiple loop control methodology for improving the performance of a SIMO dc-dc converter. It orients to generate the reference for the pulse width modulated (PWM) pulses through the coordinated error manipulation of the different outputs following the principles of four different control strategies. The efforts revolve around the comparative study of the time response specifications and measurement of ripple across the operating range of the converter. The exercises evaluate the response on a MATLAB® platform and augur its validation through the results from a prototype.

3.1 Power Module

Figure1 shows the general topology of SIMO dc-dc buck converter with single inductor where switches S_P and S_N form main path and all other switches S_1, S_2…..S_n form sharing paths.

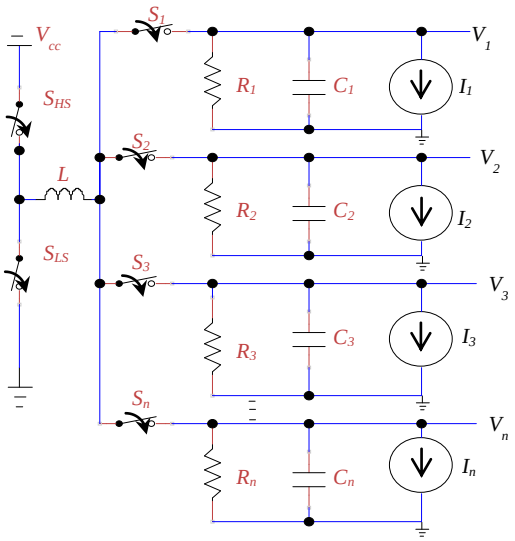
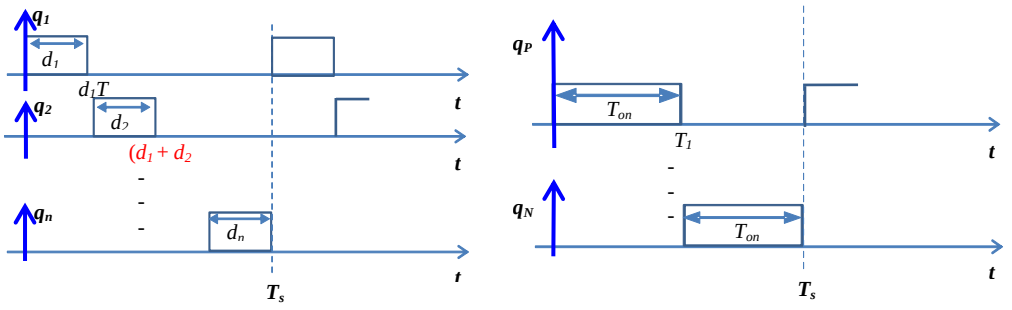


Figure 1. Circuit Diagram of SIMO Buck Converter

Designed converter can be operated in either CCM or DCM. The mode of selection is influenced by the load current rating, allowable ripples in the output voltages and cross regulation effects. Figure. 2 shows the switching scheme of the converter operating in CCM mode for one switching cycle where T_s is the period of switching.



(a) (b)

Figure 2. Switching Timing of the Converter–(a) Main Path (b) Sharing Path

The q_1, q_2, ….q_n shown in Figure.2(a) are the gating signals for the switches S_1, S_2…..S_n present in sharing paths. The gating signals for the switches in main path S_{HS} and S_{LS} are shown in Figure. 2(b) as q_P and q_N. As the converter is in Continuous Conduction Mode of operation, the designed controller has to suppress the cross regulation effects in addition to improve the transient and steady state performances.

3.2 Steady State Characterization

To determine the values of passive elements and the conducting periods of the switches in SIMO dc-dc converter operating in periodic steady state, the averages of inductor current and capacitor voltage waveforms over one switching periods are equated to zero according to inductor volt second balance and capacitor charge balance principles.

3.2.1 Average Value of Inductor Voltage and Capacitor Current

The average value of voltages across inductor for 'n' outputs are given in equation (1)

$$V_L = \sum_{i=1}^{n} V_{in} d_i - \sum_{i=1}^{n-1} V_{oi} d_i - V_{on}\left[1 - \sum_{i=1}^{n-1} d_i\right] \tag{1}$$

The capacitor current based on charge balance principle is given as $d_i I_L = \frac{V_{oi}}{R_i}$, $i = 1,2, \ldots . n$ and

$$\left(1 - \sum_{i=1}^{n} d_i\right) I_L = \frac{V_{on}}{R_n} \tag{2}$$

By using the equations (1) and (2), the average inductor current I_L and the average voltages V_{01}, V_{02} ,…V_{0n} can be determined. The inductor current I_L and the average voltages are given by the equations (3) and (4).

$$I_L = \frac{\sum_{i=1}^{n} V_{in} d_i}{\sum_{i=1}^{n-1} d_i^2 R_i + (1 - \sum_{i=1}^{n-1} d_i^2) R_n} \tag{3}$$

$$V_{oi} = d_i R_i \left[\frac{\sum_{i=1}^{n} V_{in} d_i}{\sum_{i=1}^{n-1} d_i^2 R_i + (1 - \sum_{i=1}^{n-1} d_i^2) R_n}\right]$$

where $i = 1,2,\ldots..n - 1$

$$V_{on} = \left(1 - \sum_{i-1}^{n-1} d_i\right) R_n \left[\frac{\sum_{i=1}^{n} V_{in} d_i}{\sum_{i=1}^{n-1} d_i^2 R_i + (1 - \sum_{i=1}^{n-1} d_i^2) R_n}\right] \tag{4}$$

The steady state values of the effective duty cycles are selected such that the desired operating point of average value of inductor current and average value of output voltages can be obtained.

3.2.2. Ripple Analysis

In all switching converters, dc output voltages have ripples whose peak to peak amplitude is in the order of ten to few hundred millivolts. The small ripple approximation predicts zero output voltage ripple, regardless of the value of the output filter capacitance. But the component of output capacitor current arises from the inductor current ripple. Hence the inductor current and the capacitor voltage ripples play a major role in determining the value of capacitor and inductor.

As the inductor current profile has charging and discharging periods, its ripple ($|\Delta_{iL}|$) for an ideal converter is expressed as in equation (5).

$$|\Delta_{iL}| = \frac{1}{Lfsw}\sum_{i=1}^{n}[V_{in}d_i - V_{oi}d_i] \quad (5)$$

where f_{sw} is the switching frequency

The selected value of L should satisfy the inequality in equation (6) to get the desired current ripple

$$L \geq \frac{1}{|\Delta_{iL}|_{max}fsw}\sum_{i=1}^{n} V_{in}d_i - V_{oi}d_i \quad (6)$$

The voltage across the i^{th} output capacitor during its charging subinterval can be considered to find the output voltage ripple ($|\Delta V_i|$) in equation (7) for an ideal converter

$$|\Delta V_i| = \frac{d_i(1-d_i)\sum_{i=1}^{n}V_{in}d_i}{C_i fsw \sum_{i=1}^{n-1} d_i^2 R_i + (1-\sum_{i=1}^{n-1} d_i^2)R_n} \quad (7)$$

The output capacitor C_i is selected using equation (8) such that the value of ΔV_{oi} should be less.

$$C \geq \frac{d_i(1-d_i)\sum_{i=1}^{n}V_{in}d_i}{|\Delta V_i|_{max}fsw\sum_{i=1}^{n-1} d_i^2 R_i + (1-\sum_{i=1}^{n-1} d_i^2)R_n} \quad (8)$$

4. Multi Loop Controller Structure

Figure 3 shows the block diagram of multi loop controller for SIMO dc-dc buck converter. All loops have been provided with the same controller either Error Compensator or PID controller or Fuzzy tuned PID controller or Sliding Mode Controller (SMC).

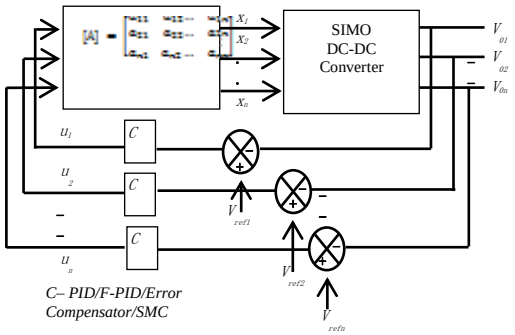


Figure 3. General Block Diagram of Multi loop Controller

The error signal obtained from each output is processed by the controller. The control signals from each loop are manipulated according to the coefficients of matrix [*A*] to generate the reference signal of PWM pulse generator. Hence "*N*" number of control equations have to be framed by considering the outputs of control loops as inputs (*U*) .The elements of matrix [*A*] is selected in such a way that the cross regulation between the outputs are minimal and hence it represents the best tradeoff between complexity and effectiveness. Figure 4 shows the variation of inductor current with respect to time during the conducting period of the switches in main and sharing paths.

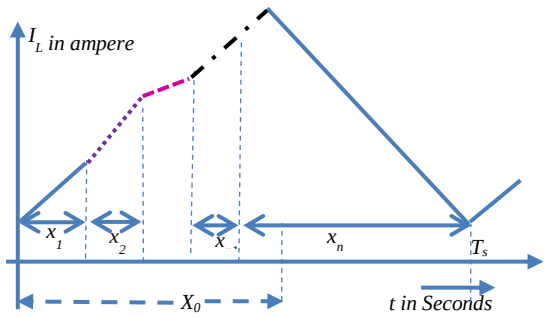


Figure 4. Charging and Discharging Intervals of Inductor Current

$$X_0 = a_{11}u_1 + a_{12}u_2 \ldots\ldots\ldots + a_{1n}u_n$$
$$X_1 = a_{21}u_1 + a_{22}u_2 \ldots\ldots\ldots + a_{2n}u_n$$
$$X_{n-1} = a_{n1}u_1 + a_{n2}u_2 \ldots\ldots\ldots + a_{nn}u_n \quad (9)$$

X_0 decides the ON time of S_{HS} in main path and X_1 , X_2 , …….. X_{n-1} decide the ON time of $n-1$ switches in sharing path. The ON time of the S_{LS} is the complement of ON time of S_{SH} and ON time of S_n is the complement of sum of ON time of switches S_1, S_2,…S_{n-1}. The use of different [A] matrices lead to different control strategies and the chosen matrix represents the best trade-off between complexity and effectiveness.

5. Controllers for SIMO Converters

Voltage mode controllers are used in this paper for SIMO converters since they will be able to achieve the desired objectives in easiest way with minimum number of components. The input is 12V battery which is equivalent to three cell lithium ion batteries found in notebook computer. Each output of SIMO dc-dc converter is considered as an asynchronous buck converter and the controllers are designed for the specifications shown in Table.1 and Table.2 of Single Inductor Dual Output (SIDO) and Single Inductor Quad Output (SIQO) dc-dc converter respectively.

Table 1. The Parameters of the SIDO Buck Converter

Parameters	Symbol	Value
Input Voltage	V_{in}	12v
Switching frequency	f_s	33 kHz
Output 1 Voltage	V_{01}	1.5v
Output 2 Voltage	V_{02}	1.2v
Output 1 Current	I_{L1}	500mA
Output 2 Current	I_{L2}	300mA
Capacitor 1	C_1	220µF
Capacitor 2	C_2	220 µF
Inductor	L	51 µH

Table 2. The Parameters of the SIQO Buck Converter

Parameters	Symbol	Value
Input Voltage	V_{in}	12 V
Switching Frequency	f_S	33 kHz
Inductance	L	51 µH
Output Voltage 1	V_{01}	1 V

Output Voltage 2	V_{02}	1.2 V
Output Voltage 3	V_{03}	1.8 V
Output Voltage 4	V_{04}	3.3 V
Output Current 1	*IL1*	1 A
Output Current 2	*IL2*	0.5 A
Output Current 3	*IL3*	1 A
Output Current 4	*IL4*	2 A
Capacitance 1	C_1	2200 μF
Capacitance 2	C_2	1000 μF
Capacitance 3	C_3	1000 μF
Capacitance 4	C_4	3300 μF

The values of load current and voltages are taken in such way that they reflect real world applications seen in a note book computer. The controllers taken for comparison and implementation are the error compensator, PID controller, Sliding Mode Controller and Fuzzy tuned PID controller.

6. Hardware Implementation

The above said controllers are developed in MATLAB/Simulink® and their performances are analyzed. To validate the performance of all the controllers, the prototype models of the SIDO and SIQO converters are developed. The interfacing between the prototype models and the controller developed in MATLAB®/Simulink® are done with the help of data acquisition module DT 9834®. Then the output voltages are compared with the reference voltages and the error signal is applied to the compensator developed in MATLAB/Simulink® and the control voltage signals are applied to the analog output of the DAQ module.

(a) SIDO (b) SIQO

Figure 6. Laboratory Setup

The pulse width modulation generator and driver circuit avails the data from DAQ module to generate the pulses for the MOSFET switches in the power module. The Figures 6 (a) and (b) show the laboratory setup of SIDO and SIQO buck converters interfaced with DT9834® DAQ module.

7. Results and Discussions

Compensators/Controllers are developed to obtain the desired performance of the system in both frequency and time domains. The performance measures considered in this paper in time domain are rise time, settling time and steady state error and the measures in frequency domain are phase margin, gain crossover frequency and bandwidth. Rise time and settling time indicate how fast the system output reaches the steady state value and

measured during transient period. Steady state error is the difference between the final value and the desired value. The speed of response of a system is indicated by the parameter bandwidth and higher bandwidth indicates faster transient response. Phase margin indicates the amount of additional phase angle that can be added to the system such that the system reaches the verge of instability and for a good stable system the value of phase margin should be around 50^o to 60^o [18].

7.1 Error Compensator

As dc-dc converters are working at high switching frequencies to produce the output voltages with fewer ripples, the multilayer ceramic capacitors having low value of Equivalent Series Inductance (ESL) and resistance are selected. However the advantage of using multilayer capacitor leads to stabilizing the dc-dc converter with sophisticated compensation network when compared to electrolytic capacitors. The compensation network is selected based on the type/size of the inductor, capacitor and their external series resistances and the design parameters such as switching frequency, bandwidth, loop gain and phase margin. To achieve the desired performance specifications, the parameters of the compensation network have to be adjusted properly. The selected compensator will place the required number of poles and zeros at proper locations into the system such that the slope of the loop gain at zero crossover frequency is -20dB/decade to get the stable system. Each output is considered as an asynchronous buck converter with two poles and one zero. The frequency of poles and a zero are given by the equations (10) and (11).

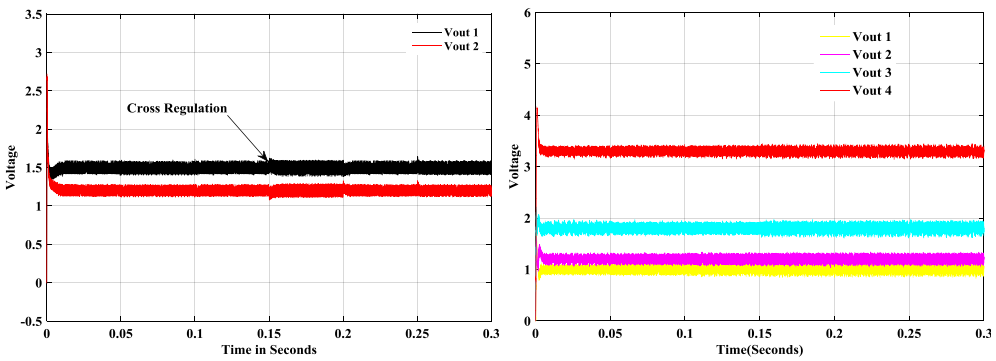
$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} \tag{10}$$

$$F_{ESR} = \frac{1}{2\pi\, ESR\, C} \tag{11}$$

where ESR is the equivalent series resistance of the output capacitor.

For SIDO and SIQO systems with the specifications shown in Tables 1 and 2, type III compensator is preferred since F_{ESR} is less than half of the selected switching frequency. The selected compensator will introduce two zeros and three poles into the system. The integrator is selected to remove the steady state error and the phase lag produced by it is compensated by the first zero. The second pole is used to compensate the zero of the system and the third is placed to attenuate the noises in the high frequency range. The second zero of the compensator is used to compensate the one of the poles of the *LC* filter in order to get the desired loop gain at the desired bandwidth. The poles and zeros are selected such that the zero crossover frequency of the system is at one tenth of the switching frequency.

The time variations of the simulated output voltages for the SIDO and SIQO converters are shown in Figures 7 (a) and (b) respectively.



(a) (b)

Figure 7. Performance of Error Compensation (a) SIDO (b) SIQO

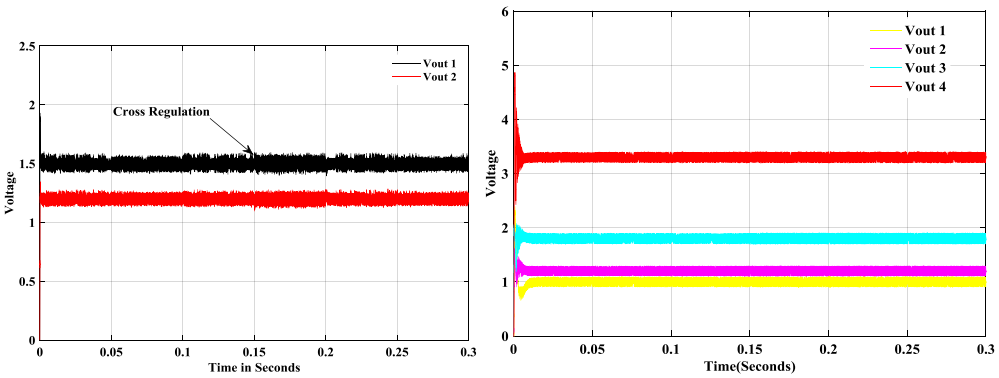
7.2. PID controller

The PID controller is preferred to make the output to settle at the steady state value with lesser rise time and smaller overshoot with zero steady state error. It does proportional, integral and derivative actions on the error signal which is the difference between the actual and desired outputs. The controller parameters can be changed dynamically and these tunable PID controllers are flexible [19].Several tuning methods are available in literature to determine the parameters of PID controller such that acceptable stability and medium fastness of response are obtained. As the type III compensator is equivalent to PID controller, the parameters of the PID controller can be obtained from the locations of poles and zeros of the error compensator. The PID controller parameters for both the systems are shown in Table 4.

Table 4. PID Controller Parameters

System	Output Voltages and Capacitor values	K_p	K_i	K_d
SIDO dc-dc converter	1.2V with 220 µF	0.3378	1367	2.045e-05
	1.5V with 220 µF	0.3378	1367	2.045e-05
SIQO dc-dc converter	1V with 2200 µF	1.2118	1550	2.320e-04
	1.2 V with 1000 µF	0.7679	1457	0.990e-04
	1.8V with 1000 µF	0.7679	1457	0.990e-04
	3.3V with 3300 µF	1.5572	1622	3.640e-04

The time variations of the output voltages for both the systems in simulation are shown in Figures 8 (a) and (b) respectively.



(a) (b)

Figure 8. Performance of PID Controller (a) SIDO (b) SIQO

7.3. FUZZY Tuned PID Controller

The DC-DC converters exhibit non linearity due to the variable structure behavior during a single switching period. Nonlinear control methods such as FLC are in vogue for controlling the dc-dc converters [20]. Fuzzy Logic Controllers are based on fuzzy set theory with linguistic variables. The fuzzy logic controller and PID controller however enjoy their own advantages while FLC perform better in terms of reduction of rise time and the PID controller produce less steady state error. But the FLC may not be able to withstand the load disturbance as PID controller. These factors give the designer to hybridize and enjoy the benefits of both the controllers [21]. '*n*' number of controllers are

designed to place in '*n*' number of loops. The block diagram of the controller is shown in Figure 9.

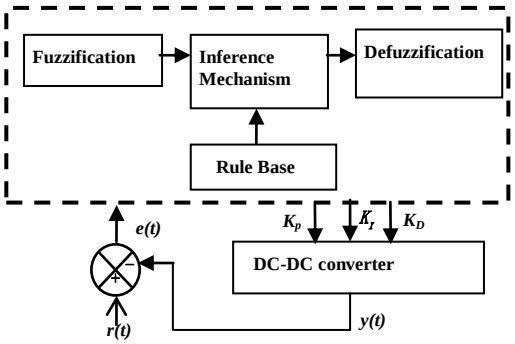
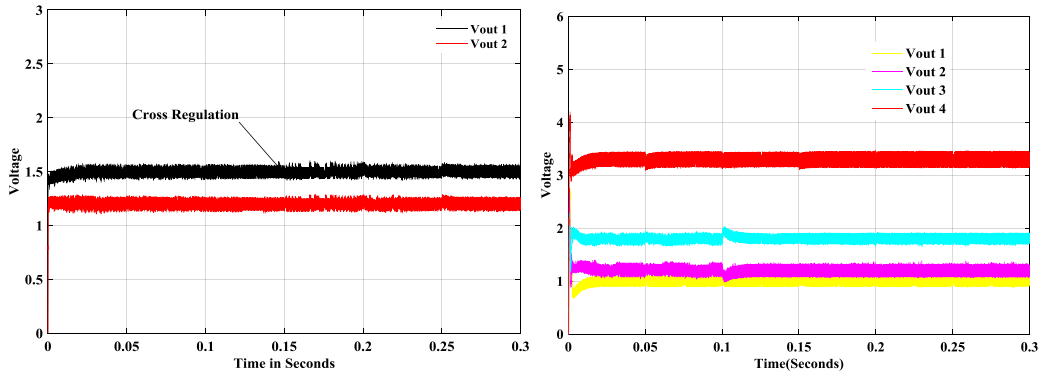


Figure 9. Fuzzy Tuned PID controller

The output *y(t)* from the dc-dc converter is compared with reference *r(t)* which gives the error signal *e(t)*. Error and change in error are the crisp set of input data to the fuzzy controller which have to be converted into fuzzy data using fuzzy linguistic terms. The triangular membership function is used to quantify the linguistic terms. To control the output variable Mamdani fuzzy rule base is constructed and inference is the process of using maximum algorithm for combining the results of individual rules. To convert the fuzzy value into a final crisp output middle of maximum defuzzification algorithm is used. The output decides the K_p, K_i and K_d values of the PID controller. Figures 10 (a) and (b) show the output of the simulated results of the SIDO and SIQO converters.



(a) (b)

Figure 10. Performance of Fuzzy Tuned PID Controller (a) SIDO (b) SIQO

7.4. Sliding Mode Controller

The Sliding mode controller is a nonlinear control method which gives guaranteed stability and robustness against parameter, line and load uncertainties. The function of the sliding mode controller is to push the system trajectories towards the sliding surface such that the system will remain in stable quiescent point. It is designed for each output considering '*n*' number of buck converter is designed for '*n*' outputs. The sliding surface for *n* controller loops for the converter is given by the equation (11)

$$S_i = \alpha_i x_{1i} + x_{2i} \tag{11}$$

where $i = 1, 2, 3 \ldots n$, α_i is the sliding coefficient, x_{1i} are the output voltage errors and x_{2i} is the differentiation of output voltage errors.

The control component to drive the state trajectories is given in equation (12)

$$U_{ni} = Sign(S_i) \tag{12}$$

In order to maintain the system on the sliding surface, the continuous component U_{eqi}, is developed as in the equation (13) in terms of the L and C_i components of the converter when $\dot{S}_i = 0$.

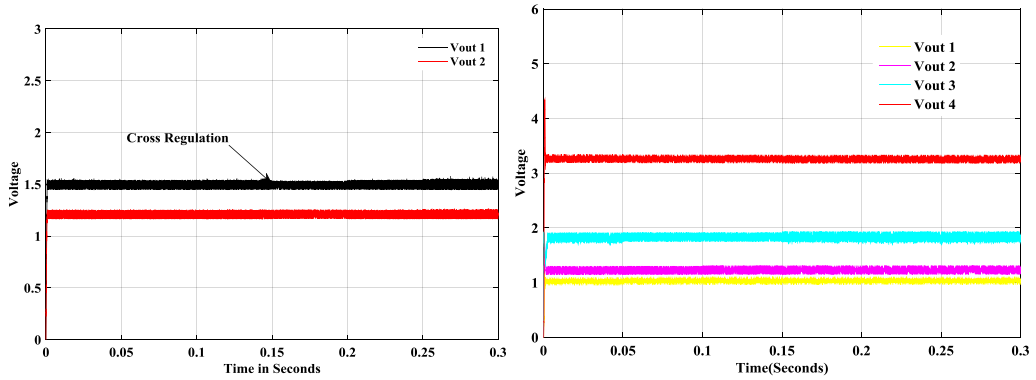
$$U_{eqi} = \left[\frac{L-\alpha_i R_i C_i L}{R_i C_i V_{in}}\right] i_L - \left[\frac{L-\alpha_i R_i C_i L - R^2 C}{R_i^2 C_i V_{in}}\right] V_{0i} \tag{13}$$

The dc control output from the controller is $U = U_n + U_{eq}$ which can be used to vary the conducting period of the devices in response to line and load disturbances.

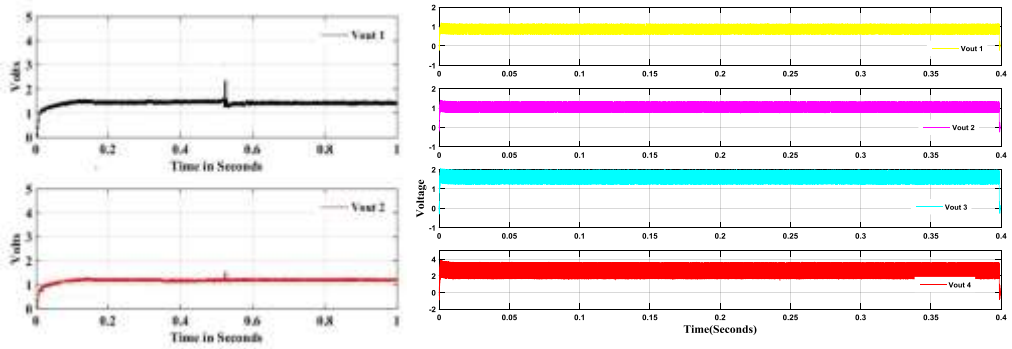
The sliding coefficient is selected such that it should satisfy the constraint in equation (14) to satisfy the time domain specifications.

$$\alpha_i \geq \frac{1}{R_i C_i} \tag{14}$$

The simulated and hardware output voltages for the SIDO and SIQO converters are shown in Figures 11(a) and (b).



(a)



(b)

Figure 11. Performance of Sliding Mode Controller (a) Simulation (b) Hardware

To analyze the performance of SIDO and SIQO converters with controllers/compensators, rise time and settling time observed during transient period and ripples and the steady state error measured during steady state period are considered. To estimate the robust stability of the converters, load disturbances are given and the cross regulation between the outputs are observed. As the settling time of the outputs are in the order of milliseconds, a time window of 0.3 seconds is sufficient to show the cross regulation.

The performances shown in the Figures 7-11 display the slight changes in all the outputs due to simultaneous sudden increase in load in one output and further establish its capability to restore back to the desired set point output. The PID controller has a larger overshoot and quicker rise time compared to the other controllers. The Fuzzy tuned PID and SMC controllers enjoy a negligible Percentage Overshoot and Peak Time value. While the cross regulation appears to be the highest in the PID controller, it follows a progressively diminishing magnitude for the Fuzzy tuned PID controller, Error compensation and SMC. The PID offers a poor transient response and a higher cross regulation besides the amount of ripple voltages being high. However the results of the sliding mode controller in Figure 11(a) and 11(b) reveal a very good transient response, less ripples and very low cross regulation. Figures 12 and 13 show the performance comparison of all four controllers for SIDO and SIQO converters in terms of rise time, settling time, ripple and mean value respectively.

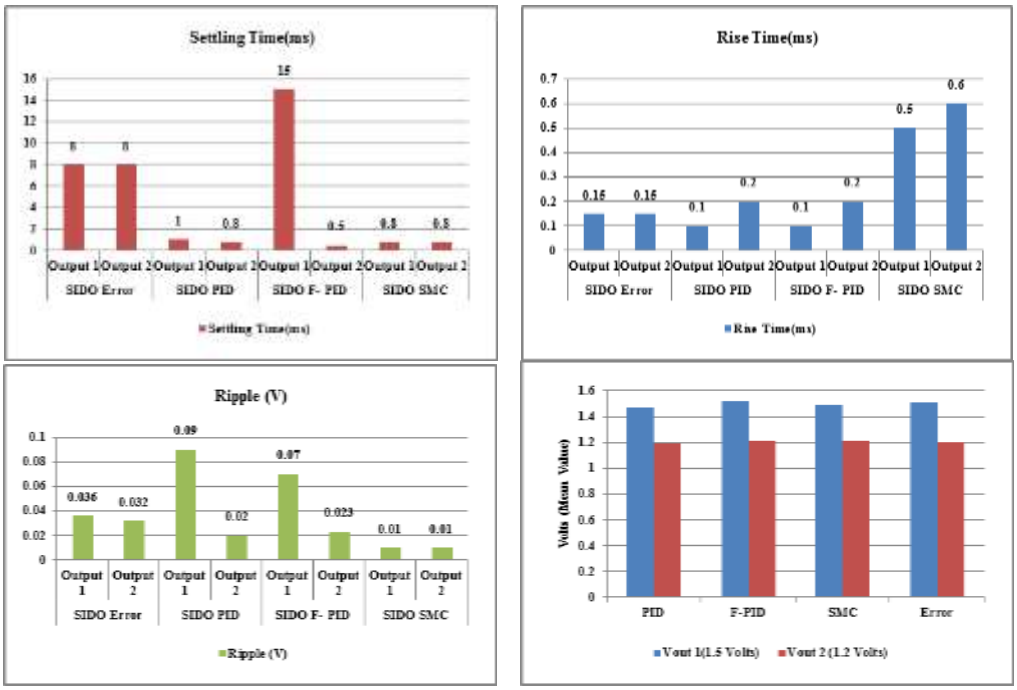
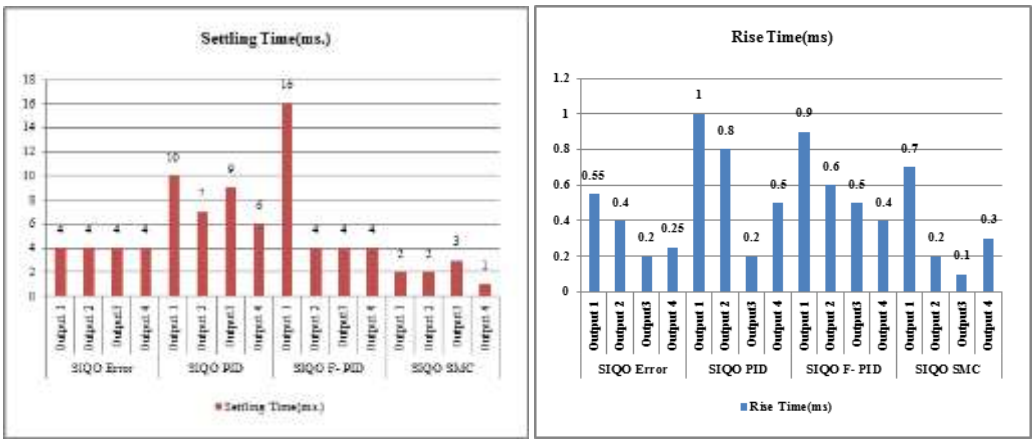


Figure 12. Performance Analysis of Multi loop Controllers for SIDO Dc-Dc Converters

The Figures 12 and 13 reveal that except for the rise time, the SMC controller outperforms the other three controllers.



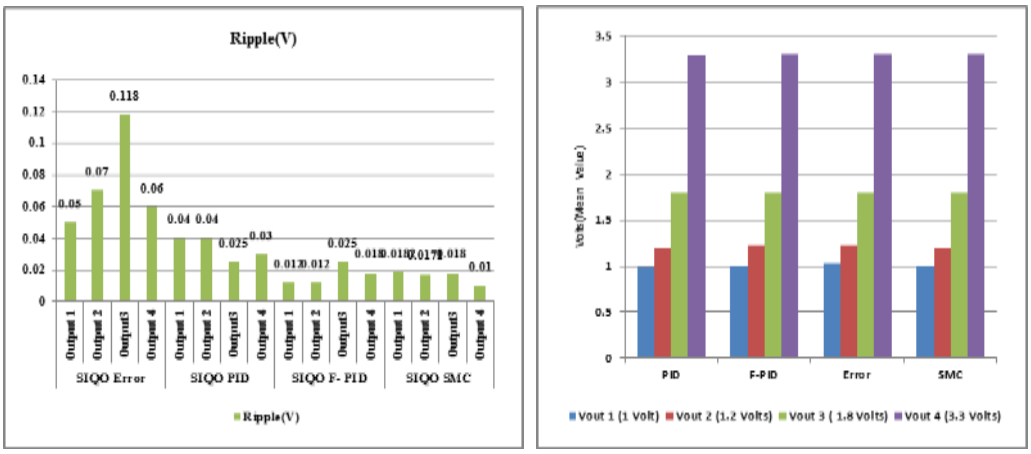


Figure 13. Performance Analysis of Multi loop Controllers for SIQO Dc-Dc Converters

The plots showing the mean value reveal that Sliding Mode Controller is able to make the steady state error of the output voltages zero.

8. Conclusion

A multi loop control mechanism has been formulated to enhance the performance of a SIMO dc-dc converter. The study has been endowed with the investigations of four different controllers to elicit the benefits of one over the other for use in the chosen multiple output converters. The performance has been measured in terms of time response characteristics and output voltages mean value and ripple. The load regulatory analysis has been included to exhibit its ability for rejecting the transient disturbances and ensuring a stable output over the range of operating loads. The SMC has been seen to deliver the best results followed by PID, Fuzzy Tuned PID and Error Compensation techniques. The results of the SIDO and SIQO converters have been cast to outweigh that of isolated closed loop responses and establish a place for the SIMO converters a role in the consumer electronics world.

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