International Journal of Control and Automation
Vol.10, No.8 (2017), pp.41-52
http://dx.doi.org/10.14257/ijca.2017.10.8.04

Design and Implementation of Scan Flip-flop for Processor Using QCA Technology

Shanthala.G.M[1], Riazini[2] and Karthik.P[3]

[1]*Dept. Of ECE, K. S. School of Engineering & Management, Bangalore*
[2]*Dept. Of ECE, the Oxford College of Engineering, Bangalore*
[3]*Dept. Of ECE, K.S.S.E.M, Bangalore*

Abstract

The present day technology is more improved. Many devices like processors, digital circuits, controllers etc. can be designed with good performance like high speed operation, less power consumption and reduction in sizes. In this paper a scan flip-flop is designed using 2:1 Mux and D flip-flop. A scan flip-flop is being used in processors for built in self-test. They can scan the internal chip and detect their fault before fabrication. So this helps to reduce time and cost. At the time of testing after fabrication if any fault is detected, it leads to waste of money and effort of our work. Quantum Cellular Automata is a encouraging nanotechnology that has accepted as one of the top six incipient technology in imminent computers. We have urbanized a new methodology in QCA design of 2:1 MUX, D flip-flop and a Scan flip-flop using efficient MUX and D flip-flop. These circuits designed by QCA, evidenced to have better area proficiency and less input to output delay compared to CMOS design. QCA Designer simulator tool is used to test the proposed design. The tools used to simulate the circuits are QCA designer tool and Cadence tool. Cell count of the proposed design is very less compared to previous design. Thus there is reduction in area usage. Also the power dissipation is $0.079X10^{-15}$ J, *which is very less. The area occupied by QCA designed scan flip-flop are in nm^2 whereas CMOS designed scan flip-flop occupied area in µm.*

Keywords*: Majority voter Circuit, majority gate, QCA Designer, QCA Cell, QCA 4:1 MUX*

1. Introduction

CMOS Technology is impending its clambering rapidly. The designing in nano-space factor is facing big problems. Quantum-dot cellular Automata is a feasible substitute to current CMOS technology. It is achieving its eminence in digital circuit design due to its great device compactness and clocking rapidity. QCA cells and a QCA majority gate have been tested successfully. The data communication and processing in QCA is purely due to columbic mechanism. The radical elements of this new nano technology are majority voter & inverter. Each digital cut is designed using majority gate & inverter gate. The majority gate is designed and implemented using Boolean expressions. The primitive gates are AND, OR and NOT. This designing is more efficient for digital circuits since it is having lesser number of gates. In this paper, proposed 2:1 MUX, designed using QCA has resulted with best performance such as less cell count and less input output delay. This high performance MUX is used in scan flip-flop which in -tern also showed good result compared to CMOS design.

1.1. QCA Concept in Details

This QCA technology has quantum cells. The quantum cells has 2 electrons present at a time, has 4 quantum wells & 2 electrons are occupies in adjacent position to each other.

ISSN: 2005-4297 IJCA

The polarization takes place here, it is done with the help of columbic repulsion. The polarization constitutes two modes of operation: logic '0'& logic "1". Advantage of QCA is there is current flow in & out of each cell.

The cells within the design are field configured, so charge from one cell is transmitted to next cell. The highlight property for this is , the essential device -device interaction's barrier state between each state is modulated by the clocking scheme. This clocking scheme does the work of lower power dissipation. When cells are arrange in series they act as wires, which will be having the same values for all cells. Usually the primitive majority gate has 3 initial inputs, one polarization state assigned by us, one output & an processing cell in between all the above four cells as shown in Figure 1a and Figure 1b. Assume three input's of majority voter like U, V, W. They can be expressed as M(U,V,W)=UV+VW+WU. IF we want to do operation like OR or AND it is dependent on the polarization that we request. Inverter circuit is shown in Figure 1c.

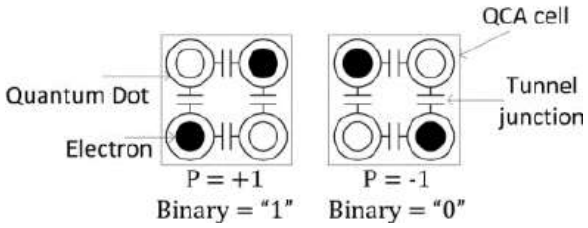


Figure 1a. Simple QCA Cell

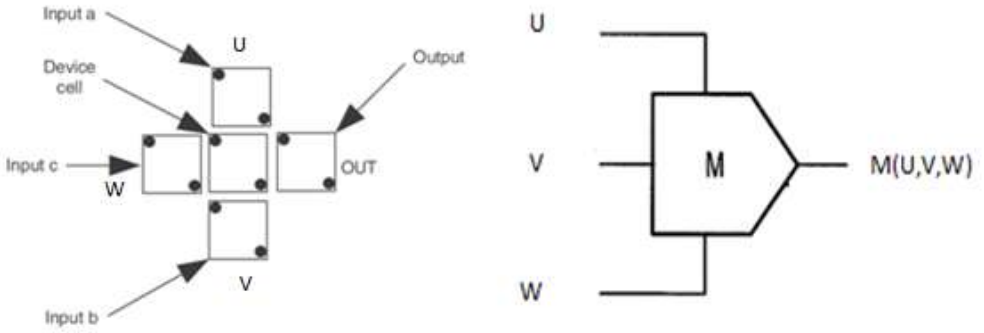


Figure 1b. Majority Gate QCA

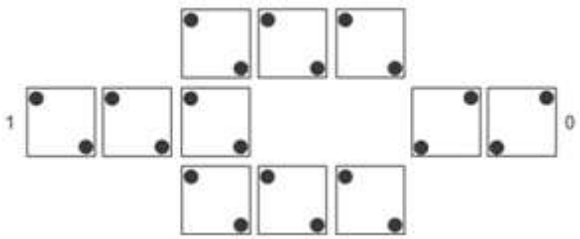


Figure 1c. QCA Inverter

1.2. QCA Clocking

The quantum dot cellular automation clocking schemes is provided with the help of potential barriers. When we have low range of potential, then the electrons are said to be at no operation. The tunneling rate is reduced when increase the potential barrier at that time the electrons initialize to localize .When the electrons gets localized they starts to do polarization. The cells get localized at highest barrier potential. The localized cell behaves

as usual input & the active input will have new values. It leads to input pipelining. The clock zones with time period is shown in Figure 2.

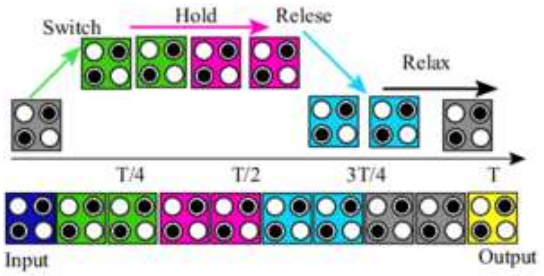


Figure 2. QCA Clocking

1.3. Advantages of QCA

- The QCA technology is known to be a "edge driven". Since it has the input at one edge &respective related output is obtained at another edge.
- It does not require any power line for power internally for transferring input to output.
- As it does not require any power, it just requires the proper presence of selection to motivate the flow of output wave form from ground state.
- Quantum cells are very small measured in nano-scale, requires less very less area, cell count power.

2. Reported Works

Tiago Teodosio *et al.* [1] was the first team to found this QCA designer tool. This tool helped to design the logical circuits in automatically generating their layout using quantum cells. Some of the examples like basic logic gates inverter, AND and OR Gates, QCA layouts are generated. They are compared with the truth table to verify the output. The sop transactions in nano technology was explained [2]. They have designed the 2:1 Mux, 4:1 Multiplexers with some changes in their parameters like cell count, area usage, delays, power and energy, *etc*. J.Huang *et al.* [3] has designed some sequential circuits using quantum dot nano technology. In their paper they explained about some Flip-flops like D Flip-flop, SR Flip-flop, JK Flip-flop, T Flip-flops. The details about the clocking scheme in QCAD tool were also explained. Each and every Flip-flops output were verified with their respective truth table. Bahniman Ghosh *et al.* [4] designed some combinational and sequential circuits using QCA. They are 4:2 priority encoder, 8:3 simple encoder, scan Flip-flop, pseudo random bit sequence generators layout was generated and they were compared with the CMOS technology. Finally these all designed circuits are cascaded into a big complex circuit design to form some designs like ALU (or) Arithmetic Logic Circuit, FPGA (or) Field Programmable Gate Array Circuits. These circuits are more suitable for physical implementation due to the majority voters fault tolerance.

The RAM Memory cell and some other various memory cells are designed and explained by JhonTimler *et al.* [5][6]. In this paper they have given the full description related to power and energy dissipation. All the memory cells are designed using majority voter with five QCA cells. He also explained about the shift register and the power flow taking place manner. In paper [7] by K.Walns *et al.*, has briefed about the RAM memory cell designing with 1*4 RAM and also designed the decoder layout. In this, the RAM has the storage capacity about 1.6 Gb/cm.sq . The design layout of 1*4 RAM is combines with 2 to 4 decoder layout within it .In paper [8] , a brief and clear information about the

basics of QCA, the QCA cells and the quantum dots . They also explained about clocking schemes. In paper [9], They described about the sequential circuit designs. They also explained about RAM memory cell. In this differently explained about the comparison of QCA layout with Intel core. They had the high input feedback during read and write operation. V.Vankamamidi [10] has given full description about the advantages and disadvantages of QCA over CMOS technology. They have explained what is the use of reducing cell count, area, so because of it power dissipation is efficient in QCA with less cell count and area. In [11] , Praveen Venkataramani *et al.* and in [12] Durgamadhad *et al.* explained about the sequential circuit designing using quantum dot and how the derivation is carried out for energy and power dissipation and has compared their derived values with CMOS VLSI circuit designing .

R.Vennila *et al.* [13] have given the analysis for decoder circuit using the quantum dot. They also have said about the memory cell like serial and parallel m/m , The working of serial and parallel m/m in QCA with logical diagram . X.Gao *et al.* [14] exposed about the quantum bit especially for targeting silicon multi-level quantum dots. They explained the quantum basics with Boolean expressions and their truth table for majority voter. Xiao Zhang *et al.* [15] has addressed the problems we deal with to achieve throughput and to obtain high speed without any fairness in crossbar switch. P.Donglas Tongan *et al.* [16] and In [17], Huzefa Saifee *et al.* has demonstrated the how coulumbie interaction takes place and their polarisation properties and their two states foe polarisation. He also done the simulation for programmable logic gates and the complex gates also. In this paper [18] by Mrinal Gosnamy *et al.* shown that there is an alternate technology for CMOS technology that is QCA technology. In this paper they have designed D-Latch, Multiplexers, Counters, T-Latch, ALU, etc . The advantages of QCA for logic synthesis and the cell count, area, delay were also discussed. Kun Kong *et al.* [19] and [20] by Sanjukta Bhanja proposed the majority gate and their synthesis for logic circuits. The proposed QCA designed is taken as reference and have explained about the optimization of cells in a layout and they have explained the power dissipation in upper bound in QCA circuits.

3. Earlier Work

3.1 2. 1 MUX

The mechanism of plugging one or more signal and imparting into a single passage is known as Multiplexing. This can be effectuated by the gadget called Multiplexer. The logical diagram of 2:1 MU is shown in Figure 3. These are mostly widely used in digital circuits and systems. Also the majority voter cell is also shown in Figure 4.

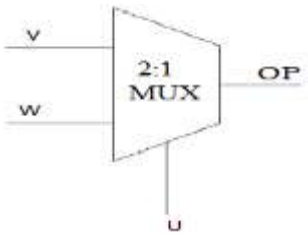


Figure 3. Logical Diagram of 2:1 MUX

Table 1. 2:1 MUX Truth Table

SELECT IP=SEL	OP
0	V
1	W

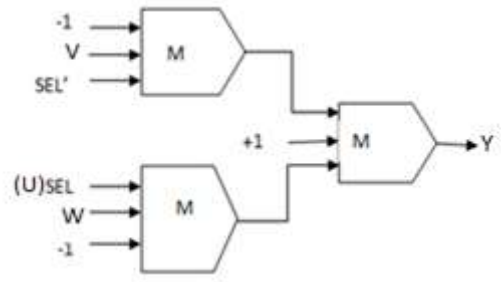


Figure 4. Majority Voter Block for 2:1 MUX

The 3 signal inputs are U, V, W. The selector input is corresponds to U and the multiplexer output signal is Y. A Block was included in this design, which is an AND Block and an OR block. When the clocking phases are adjacent to one another they help to admit the correct signal propagation. Figure 5 represents the circuit diagram of earlier 2:1 MUX and simulation results.

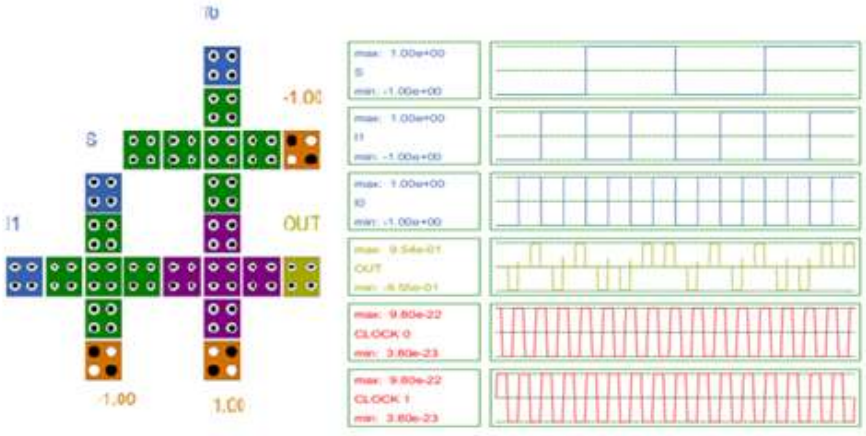


Figure 5. Circuit Diagram of Earlier 2:1 MUX Unit with Simulation Result

3.2. Scan Flip-flop

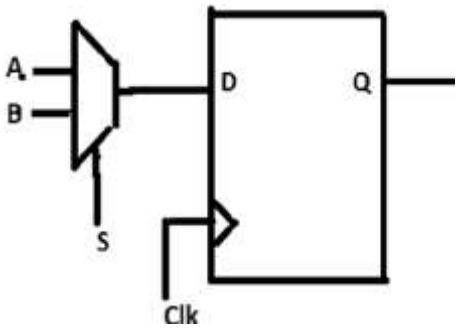


Figure 6a: Block Diagram of Scan Flipflop

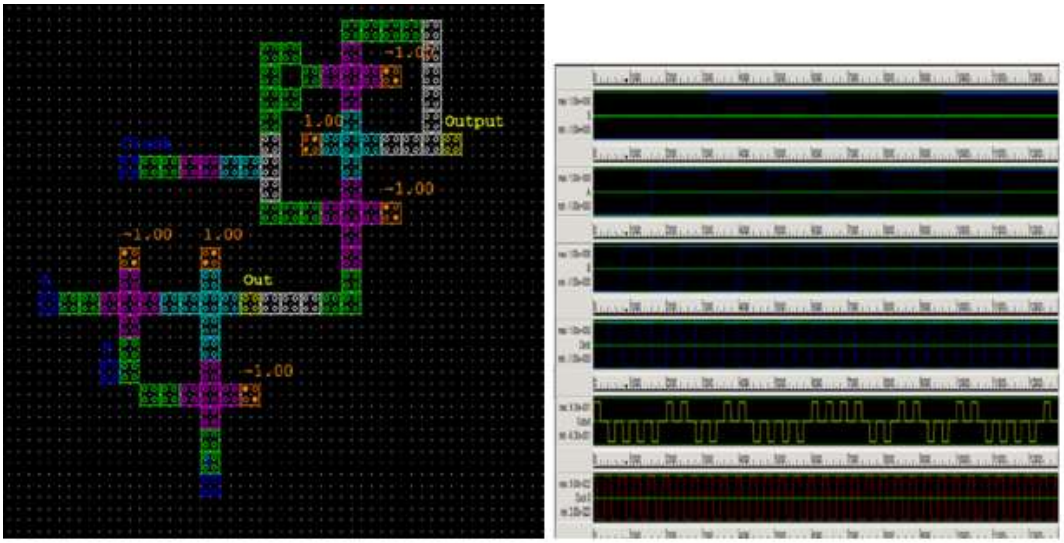


Figure 6b: QCA Layout and Waveform of Scan Flip-flop

Earlier scan flip-flop Block diagram is shown in Figure 6a, also layout and waveform are represented in Figure 6b.

4. Proposed Work

4.1. 2:1 MUX

A new design for 2:1 mux is proposed here where efficient MUX design with required performance was achieved. For the same, conventional approach was also tried, where two AND gates are used for anding two inputs with the selection line and One OR gate to add them. **Figure 7** shows circuit layout and simulation result of proposed 2:1 mux

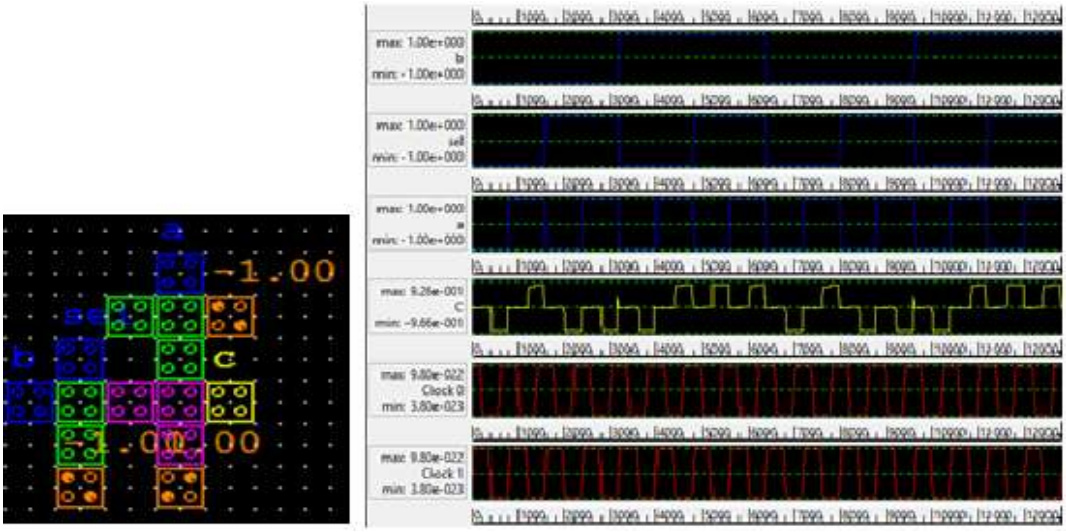
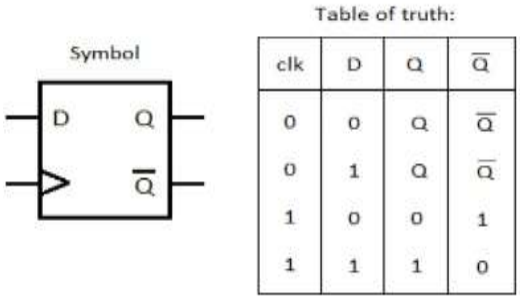


Figure 7. Circuit Diagram and Simulation Result of Proposed 2:1 Mux

4.2. D Flip-flop

D flip-flop is considered as the basic memory cell. D stands for “data”. This stores the values (either logic ‘0’or logic ‘1’) present on the data line. The D flip-flop changes its

state for edge triggering clock. A set/reset flip-flop can be used to implement D flip-flop by tying the set to the reset through an inverter**.** D flip-flop circuit layout and simulation results are shown in Figure 9.



clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Figure 8. D Flip-Flop Block Diagram and Truth Table

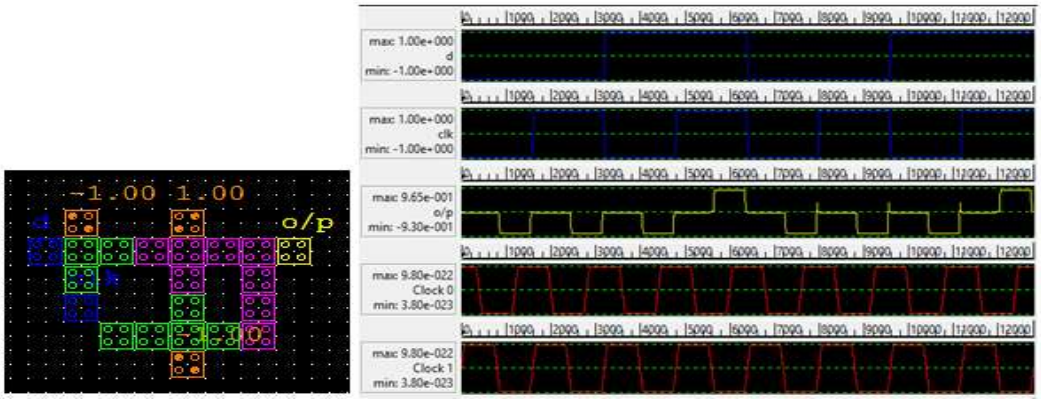


Figure 9. QCA Design and Simulation Result of D Flip-flop

4.3. Scan Flip-flop

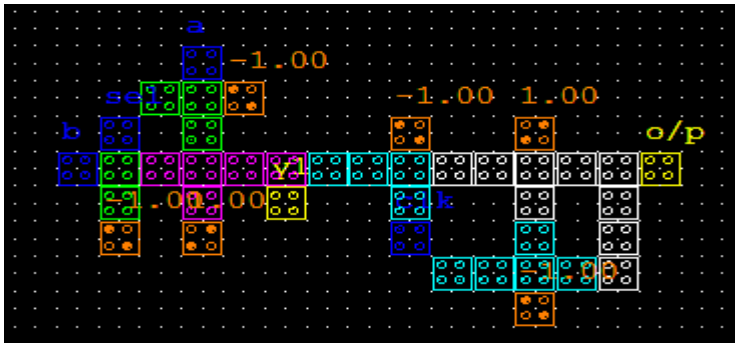


Figure 10. Proposed Scan Flip-flop

This is the proposed design of our scan flip-flop. Here we have reduced the cell count, area, less power dissipation and delay less , more efficient circuit design. Figure 10 shows the proposed scan flip-flop layout and Figure 11 shows the simulation result of scan flip-flop. The output of 2:1 mux is provided as input for D flip-flop which constitute a scan flip-flop.

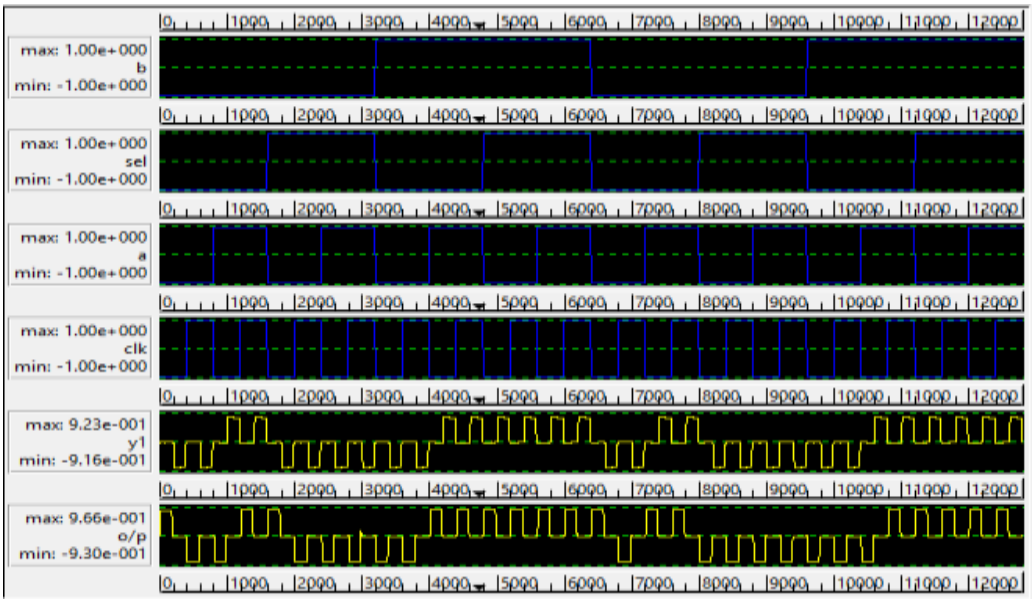


Figure 11. Output of Scan Flip-flop

Scan flip-flop simulation result and synthesized report are shown in Figure 12 and Figure 13. Also cell report is shown in fig14. All this reports are generated using cadence tool. The area occupied by CMOS design is 18µm.

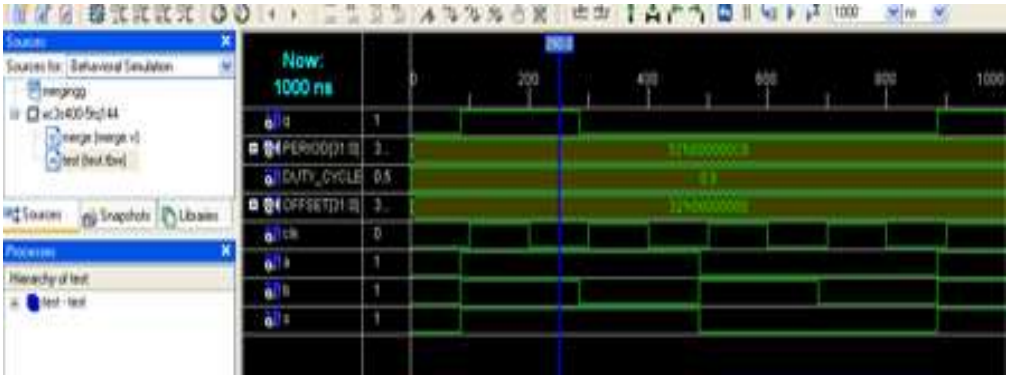


Figure 12. VHDL Simulation Output of Scan Flip-Flop

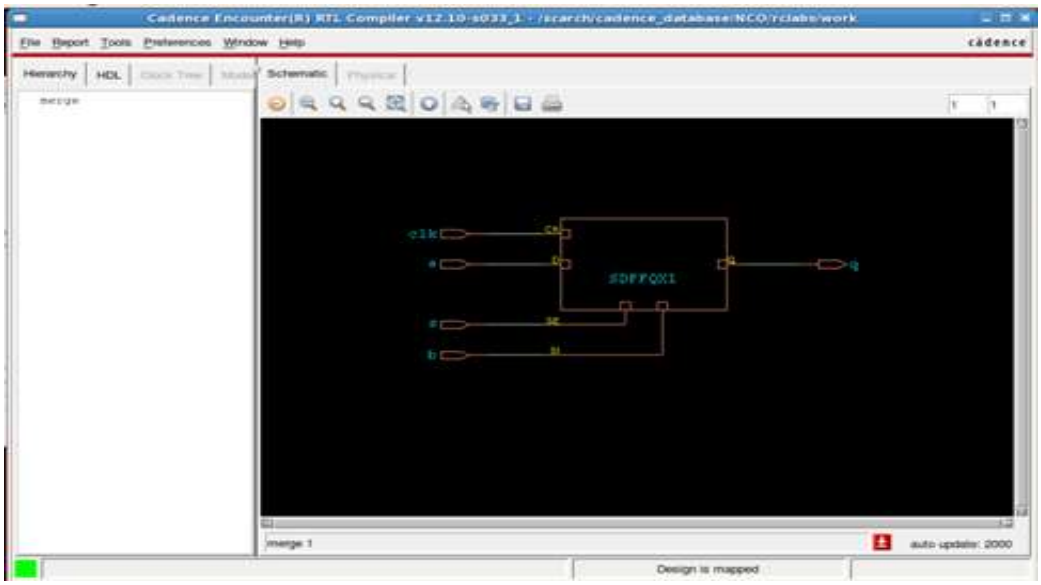
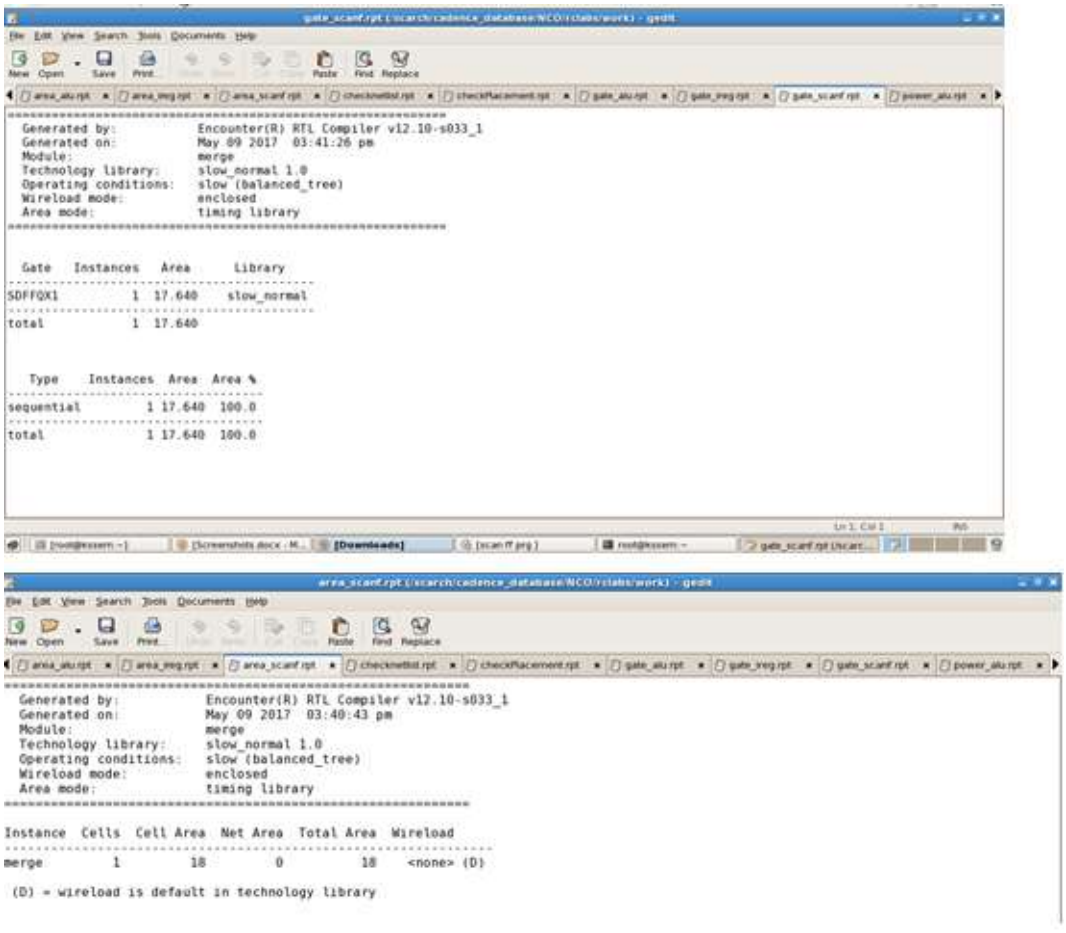


Figure 13. Cadence Synthesized Output of Scan flip-flop



```
  Generated by:           Encounter(R) RTL Compiler v12.10-s033_1
  Generated on:           May 09 2017  03:41:26 pm
  Module:                 merge
  Technology library:     slow_normal 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
------------------------------------------------------------------


  Gate   Instances   Area      Library
------------------------------------------
SDFFQX1          1  17.640    slow_normal
------------------------------------------
total            1  17.640


   Type    Instances  Area  Area %
-----------------------------------
sequential         1 17.640  100.0
-----------------------------------
total              1 17.640  100.0
```



```
  Generated by:           Encounter(R) RTL Compiler v12.10-s033_1
  Generated on:           May 09 2017  03:40:43 pm
  Module:                 merge
  Technology library:     slow_normal 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
------------------------------------------------------------------

Instance  Cells  Cell Area  Net Area  Total Area  Wireload
-----------------------------------------------------------
merge         1        18         0          18    <none> (D)

 (D) = wireload is default in technology library
```

Figure 14. Area Usage of Scan Flip-Flop in Cadence

Table 2. Comparative Study of Two Designs

PARMETERS	CELL COUNT		CELL AREA OF PROPOSED DESIGN	CLOCKING
	PREVIOUS DESIGN	PROPOSED DESIGN		
2:1 MUX	23	15	18607.95 nm^2	2
D FF	23	21	24353.89 nm^2	4
SCAN FLIPFLOP	90	40	56602.80 nm^2	4

Table 3. Result of Power and Energy Dissipation Calculation Using Kink Energy

ENERGY DISSIPATION	$0.079X10^{-15}$ J
POWER DISSIPATION	$0.079X10^{-15}$ J / τ

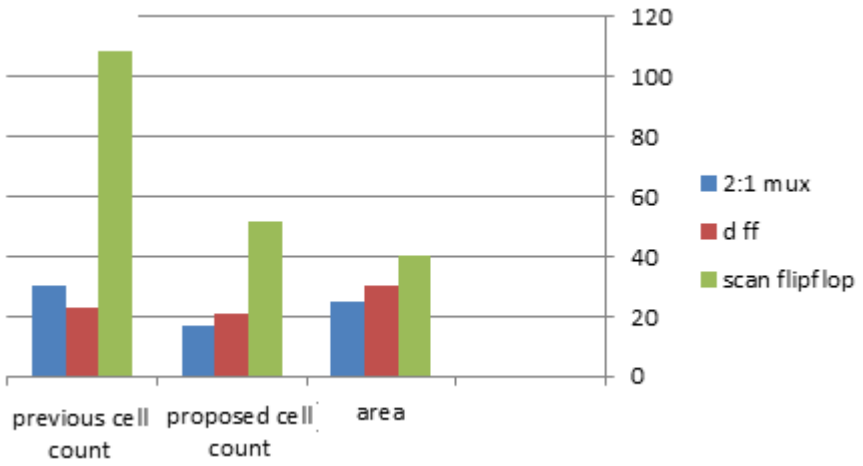


Figure 15. Comparison of Important Parameters of MUX, D Flip-Flop and Scan Flip-Flop

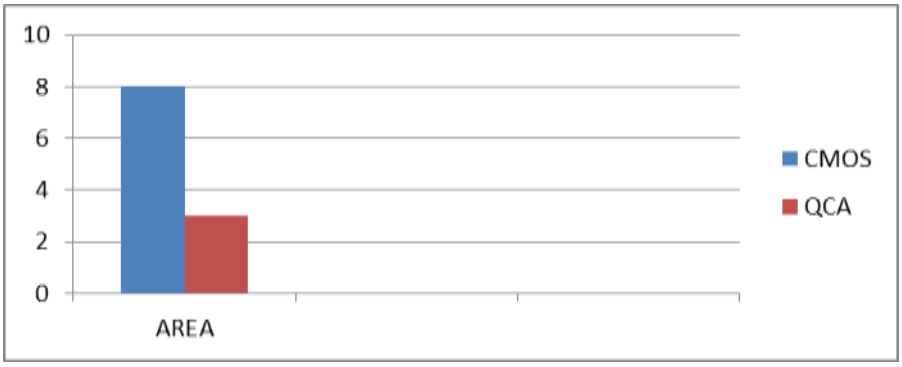


Figure 16. Comparison of Area Using QCA and CMOS Technology

5. Conclusion and Future Scope

Classical QCA method is used for designing the circuit. The energy and power dissipation is very low for scan flip-flop using QCA technology. Also comparison of few parameters designed using QCA technology showed beneficial output. The proposed methodology is an resourceful way to reduce the time and cost of digital circuits defects before to fabrication. The design using QCA technology helps further to reduce the size, area, delay of the circuit, making them more efficient. By this technique we can design more complicated digital circuits. In future optimized N bit controllers can be built and tested using this.

Acknowledgement

I would like to thank Dr. Preeta Sharan for her immense support for the completion of this work.

References

[1] E. N Gamesh, "Power Analysis of Quantum Dot Cellular Automata Circuits", 2nd International conference on Nanotechnology by ELSEVIER, **(2014)**.
[2] D. Mukhopadhay, "Improves Quantum Dot Cellular Automata 4:1 Multiplexer Circuit Unit", sop Transactions on Nanotechnology, vol. 1, no. 1, **(2014)**.
[3] J. Haung, M. Momenzadeh and F. Lombardi, "Design of Sequential Circuit by Quantum Dot Cellular Automata", Microelectromics Journal, **(2007)**.
[4] B. Ghost, S. Gupta and S. Kumari, "Novel Design of combinational And Sequential Logical Structures in Quantum Dot Cellular Automata", Department Of Ece, Iit, **(2013)**.
[5] J. Timler and C. S. Lent, "Power Gain and Energy Dissipation in Quantum Dot Cellular Automata", Journals Appl. Phys., American Institute of physics, vol. 91, **(2002)**.
[6] S. Angizi, S. Sarmadi and S. Sayedselehi, "Deisgn and Evaluation of New Majority Gate Based Ram Cell in Quantum Dot Cellular Automata", Microelectronics Journal, vol. 46, **(2015)**.
[7] C. S. Lent and B. Isaksen, "Clocked Molecular Quantum Dot Cellular Automata", IEEE Trans. Electron Devices, vol. 50, **(2003)**.
[8] K. Walus, G. A Jullien and V. S. Dimitrow, "Ram Design Using Quantum Dot Cellular Automata", ATIPS Laboratory, University of Galary, Alberta, **(2004)**.
[9] W. Liu, L. Lu and M. O'Neill and E. E. Swartzlander Jr., "Design Rules for Quantum-dot Cellular Automata", IEEE Journal, **(2011)**.
[10] S. Frost, A. F. Rodrigues, A. W. Janiszewswi, R. T. Rush and P. M. Kogge, "Memory in motion: A study of storage structures in QCA", first workshop on non-silicon computing, **(2002)**.
[11] K. Das and D. De, "Characterization, test and logic synthesis of novel conservative and reversible logic gates for QCA", International Journal of Nano-science, vol. 9, no. 3, **(2010)**, pp. 201-214.
[12] V. Vankamamidi, M. Attavi and F. Lombardi, "Tile-based design of a serial memory in QCA", In proceedings of the 15th ACM Great Lakes Symposium on VLSI (GLSVLSI"05), **(2005)**.
[13] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. sinder, "Realisation of a functional cell for quantum dot cellular automata", science, vol. 277, no. 5328, **(1997)**, pp. 928-930.
[14] P. Venkataramani and S. Bhanja, "Sequantial circuit design in quantum dot cellular automata", IEEE conference on nanotechnology, **(2008)**.
[15] H. P Koringa, V. A. Shah and D. Misra, "Estimation and Optimisation of power dissipation in CMOS VLSI circuit design: A reviewer paper", International Journal of emerging Trends in Electrical and Electronics (IJETEE), **(2013)**.
[16] M. Ottavi, V. Vankamamidi and F. Lomabardi, "Nolvel Memory Designs for QCA implementation", IEEE conference on nanotechnology Nagoya, Japan, **(2005)**.
[17] A. Khan and R. Chakrabarty, "Novel design of high polarised inverting using minimum number of rotated cells and related kink energy calculation in quantum dot cellular automata", International Journal of soft computing and engineering IISN:2231, **(2013)**.
[18] A. Vetteh, K. Walus and V. A. Jullien, "Quantum dot cellular automata of flipflops", ATIPS Laboratory, Canada, **(2005)**.
[19] S. Sheikhfaal, S. Angizi, S. Sarmadi and M. H. Moaiyeri, "Designing efficient CQA logical circuits with power dissipation analysis", Microelectronics Journal, **(2015)**.
[20] M. Prabakaran, N. Indhumathi and R. Vennila, "Design and analysis of decoder circuit using quantum dot cellular automata", IJIRS, Engineering and Technology, **(2015)**.

Authors

G. M. Shanthala, Receive M. Tech degree from VTU in the year 2005. Perusing Ph.D in VTU, Belagavi. Currently working as Associate professor in K.S School of Engineering and Management. Member of LMISTE and MIEI.

P. Karthik, Received his M.E in the area of Applied Electronics during 2006 and Ph.D in the Electronics and Communication during 2013. His areas of Interest are Embedded System, Acoustic Sensors, Image Processing, Signal Processing, Big DATA, Communication and Mobile Networks. He is the member of LMISTE, MIAENG, MACM, MIEI and IEEE Senior Member.