International Journal of Control and Automation
Vol. 10, No. 6 (2017), pp.127-136
http//dx.doi.org/10.14257/ijca.2017.10.6.13

Parameter Tuning for Double Close-loop Control System of Three-level VSR

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Abstract

A decoupler is designed to eliminate the coupling of current regulator of three-level NPC VSR double-loop control system. By this mean, the current regulator is linearized. The PI parameter of current regulator and voltage regulator is tuned by engineering design methods and a set of method of dual close-loop parameters tuning is developed. The tuned parameter is used in the simulation and experiment. Simulation and experimental results show that the control system has a good dynamic and static characteristics and the method of parameters tuning is correct and effectiveness.

Keywords*: VSR, PI regulator, dual close loop, parameter tuning*

1. Introduction

Three-level VSR which has the advantage of sine net side current, unit power factor control, two-way transmission power, and fast dynamic performance [1]. To control the net side current is sine and to keep the DC voltage stability is the goal of rectifier control [2, 3]. So, the controller is designed to current and voltage dual closed-loop controller. It is clear that the tracking performance of current and power factor are dependent on the characteristic of the current inner loop. The stability and anti-interference characteristic of system is guaranteed by voltage outer loop, using which the DC side output voltage is kept to a constant [4-7]. Design strategy of the PI parameter gains of dual closed-loop is an important issue to assure the static and dynamic characteristics of the three-level VSR [8-11].

The model of three-level VSR is firstly given, using which the model of the current regulator is constructed. A decoupler is designed to eliminate the coupling of the current regulator. Based on this, the corresponding closed-loop block diagrams of the current and the voltage are formulated, respectively. Parameter tuning method for double closed-loop control System of three-level VSR is developed. The validity of all theoretical results is verified by simulation and experiment.

2. NPC Three-level VSR Model

2.1. Model of VSR

Topology structure of NPC three-level VSR is depicted in Figure 1 Firstly, the dynamic model of VSR viewed from the synchronous reference frame is given by (1), (2) and (3).

$$L\frac{di_d}{dt} + Ri_d = e_d + L\omega i_q - V_d \tag{1}$$

ISSN: 2005-4297 IJCA

$$L\frac{di_q}{dt} + Ri_q = e_q - L\omega i_d - V_q \tag{2}$$

$$\frac{2}{3}\cdot\frac{U_{dc}^*}{e_d}\cdot C\frac{dU_{dc}}{dt} = i_d - \frac{\frac{2}{3}P_L}{e_d} \tag{3}$$

Where

e_d, e_q is the d-axis and q-axis component of ac electromotive force synthetic vector in *d-q* coordinate system, respectively.V_d,V_q is the d-axis and q-axis component of voltage vector in *d-q* coordinate system, respectively.i_d,i_q is the d-axis and q-axis component of current vector in*d-q* coordinate system, respectively.

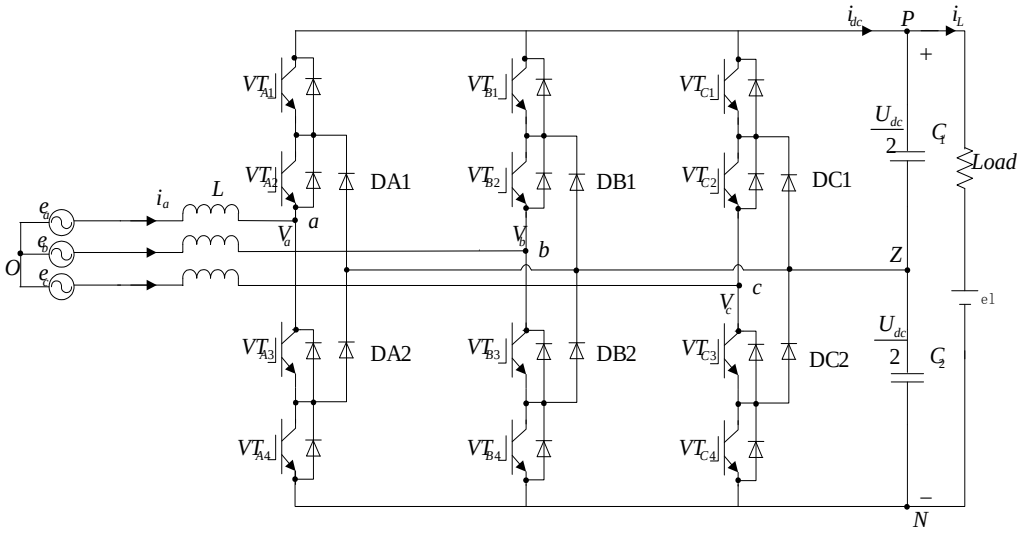

Figure 1. The Topological Structure of Neutral Point Clamped Three-level Rectifier

2.2. The Decoupling of Current Regulator

From the model (1) and (2), d-axis and q-axis exists coupling in the VSR. To resolve this, the current forward-feed control strategy based on input-output is used. Substituting $V_d = (\hat{e}_d + L\omega\hat{i}_q + \Delta V_d^*)$ and $V_q = (\hat{e}_q + L\omega\hat{i}_d + \Delta V_q^*)$ into (1) and (2) respectively, it follows that

$$\begin{cases} \Delta V_d^* = k_p\left(i_d^* - i_d\right) + k_I\int_0^t\left(i_d^* - i_d\right)dt \\ \Delta V_q^* = k_p\left(i_q^* - i_q\right) + k_I\int_0^t\left(i_q^* - i_q\right)dt \end{cases} \tag{4}$$

From the model (4), it is clear that it is two independent first-order inertia model after decoupling.

3. Parameter Tuning of Current Regulator and Voltage Regulator

3.1. Parameter Tuning of Current Regulator

The fast dynamic response and good anti-interference characteristic is the final goal for the design of current regulator. The sample delay of the current inner loop and small inertia link of PWM control is considered, the structure of the current inner loop is simplified in Figure 2.

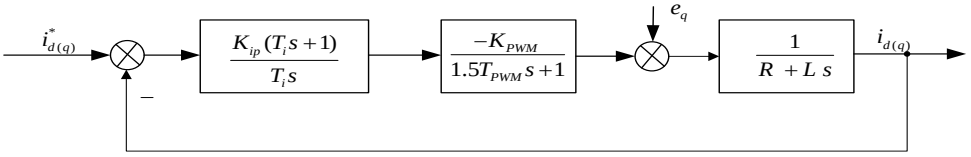

Figure 2. Control Block Diagram of Current Loop

The ac side resistance can be ignore according the actual system. From Figure2, the open loop transfer function can be derived as

$$W_k(s)=\frac{K_{iP}K_{PWM}}{T_i L}\frac{(T_i s+1)}{S^2(1.5T_{PWM}s+1)} \tag{5}$$

Where, K_{PWM} is the equivalent gain of bridge road PWM, when SVPWM is used, its value is 1. T_i is time constant of current loop. T_{PWM} is sample period, which is also PWM switching cycle. Considering rapidity and anti-interference characteristic together, let h_i=5 is the best parameter selection. According the typical Ⅱ type system parameters design guidelines, the equation is derived as

$$\frac{K_{iP}K_{PWM}}{T_i L}=\frac{h_i+1}{2T_i^2} \tag{6}$$

From (6), we can conclude

$$\begin{aligned} K_{ip}&=\frac{(h_i+1)L}{2T_i K_{PWM}}=\frac{6L}{15T_{PWM}K_{PWM}} \\ K_{iI}&=\frac{K_p}{T_i}=\frac{6L}{112.5T_{PWM}^2K_{PWM}} \end{aligned} \tag{7}$$

3.2. Parameter tuning of Voltage Regulator

The stabilization of DC bus voltage and the anti-interference characteristic is dependent on voltage outer loop controller, which is consisted of current inner loop controller and the VSR model by series connect. The current loop can be reduced order because it is a second-order system. So, we replace it by a first-order inertia link [1].

The open loop transfer function can be in Figure2 can be equivalent to transfer function as equation (8). Current time constant T_{id} is smaller than the time constant of voltage outer loop controller. So, the transfer function can be simplified approximately when the voltage controller is designed.

$$W_{ci}(S)=\frac{1}{T_{id}S+1} \tag{8}$$

The output of current controller Δi_d^* is designed as

$$\frac{2U_{dc}}{3e_d}C\frac{dU_{dc}}{dt}=\Delta i_d^* \tag{9}$$

DC voltage control block diagram is shown in Figure 3.

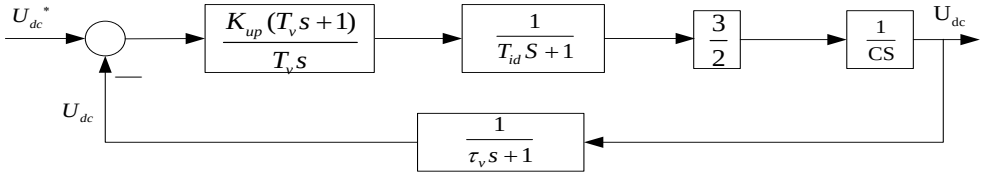

Figure 3. Control Block Diagram of DC Voltage Loop

Voltage sampling small inertia link and the equivalent small time constant current inner loop can be consolidated. The voltage open loop transfer function can be derived as

$$W_k(s)=\frac{1.5K_{up}(T_v s+1)}{cT_v s^2(T_{v\Sigma}s+1)} \tag{11}$$

Where, $T_{id}=\frac{L}{K_{ip}}$, $T_{v\Sigma}=\tau_v+T_{id}$。

Considering tracking performance and anti-interference characteristic together, let intermediate frequency bandwidth is 5. The PI pains of voltage loop can be derived as

$$T_v=5(\tau_v+\frac{L}{K_{ip}}),\ K_{uP}=\frac{2C}{(\tau_v+\frac{L}{K_{ip}})} \tag{12}$$

DC voltage PI regulator is designed as

$$\Delta i_d^*=k_p(U_{dc}^*-U_{dc})+k_I\int_0^t(U_{dc}^*-U_{dc})dt \tag{13}$$

4. The Transient Current Control

From Figures 4 and 5, it can be seen that there is a big fluctuation in the instantaneous reactive current and a very big overshot in the actual current when disturbance is added suddenly. The system can be leaded into over-current protection status. The vector control is adopted based on the grid voltage orientation. Regardless of the resistant, the reactive current should be control to 0.

It can be derived as

$$\begin{cases}L\dfrac{di_d}{dt}=e_d-V_d\\ V_q=-\omega Li_d\end{cases} \tag{13}$$

From(13), the scope of active current control is

$$\frac{e_d-V_{\max}}{L}\le\frac{di_d}{dt}\le\frac{e_d+V_{\max}}{L} \tag{14}$$

Is the output value of controller. $V_{\max}$ where

When we need added i_d, i_d can be changed more faster By superimposing V_d on e_d. But, if we want reduce i_d, overcoming the margin of e_d will slow down the speed of current adjustment. Thus, it seems that the control of VSR is asymmetric. The tracking time of different symbol of di_d/dt is obviously different and the DC voltage regulator can also affect the tracking speed of the current and then affect the dynamic process of the

current. The instantaneous voltage and sustained high current will affect the normal operation of the equipment and even damage equipment in the transient process. Therefore, it is necessary to improve the existing control method by reactive current compensation.

It can be derived as

$$\frac{U_m + \omega L i_q - V_d}{L} = \frac{di_d}{dt} \tag{15}$$

5. Simulation and Experiment

5.1. Simulation Debugging

Rated power is 3KW. Input three-phase ac line-voltage is 380V. The ac inductance is 3.7mH. DC load is $R_L = 120\Omega$.The given value of DC bus voltage is 600V. DC side capacitor is 2200uF. Switching frequency is 2 KHz.

From (7) and (12), we can calculate $K_{iP} = 2.54$, $K_{iI} = 78.9$, $K_{uP} = 0.55$, $K_{uI} = 27.5$. We find that the stable value of DC voltage is bigger than the given value and the overshot is also bigger in the debugging. It is clear that the DC stability voltage is dependent on K_{iP} and K_{uP}. The simulation result demonstrates that a better performance of controller can be achieved with a higher K_{iP} and a lower K_{uP}. The adjustment process is given priority to adjust K_{uP} Because of its influence on DC voltage is bigger. On the other hand, we find the stale speed is slower, which can be adjusted by reducing K_{iI} and K_{uI} appropriately. Then, a better series of parameters can be derived as $K_{iP} = 4.5$, $K_{iI} = 34.5$, $K_{uP} = 0.25$, $K_{uI} = 12.5$. Considering the dynamic process, The DC voltage will produce a very big overshot when the error of DC voltage has a sudden change. In order to avoiding this, a limiter should be designed. The output of voltage loop will be in a limiting state when the deviation is too large. As long as the limiting value selection is reasonable, the stability of DC voltage will be ensured. D-axis current can be calculated according the capacity of VSR. Taking 1.5 times of its limiting value and doing a fine-tuning, the limiting value is ± 25 .

The output of voltage loop is the given value of the current inner loop which requires the voltage controller has a higher stability and avoids oscillation. The simulation waveform of the voltage loop controller is shown in Figure 4 when the system is suddenly added rated load. It can be seen from Figure4 that the output of voltage controller has a certain overshot under the condition of disturbance. But, the overshot will disappear and the output can be restored stability in a short period.

As shown in Figure 6, the rectifier is added from no-load to full load suddenly at 0.3s, the three-phase current waveform is better. The DC bus voltage fluctuation and the phase relation of ac voltage and current simulation waveform are shown in Figure7 and Figure8. It can be seen, the dc bus fluctuation is not big in the situation of a sudden sharp reduction of overloading, and can quickly be restored stability which reflects the stability of the dc voltage. The voltage has the same phase with current from waveform. the simulation results prove that the net side current of rectifier has a perfect dynamic performance and has realized the unity power factor rectifier. From Figure7 and Figure8., we can see that DC bus voltage has a strong anti-interference ability which can meet with the design requirements.

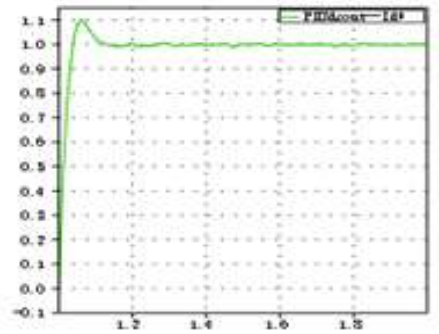

Figure 4. Waveform of the Voltage Loop Controller

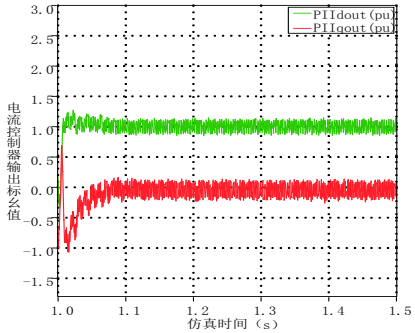

Figure 5. Waveform of the Current Loop Controller

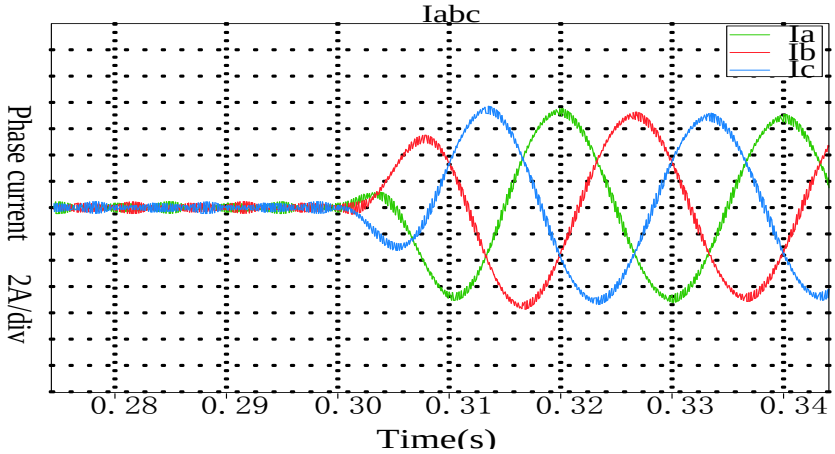

Figure 6. Waveform of Three-phase AC Current when No-load suddenly Increase to Full Load

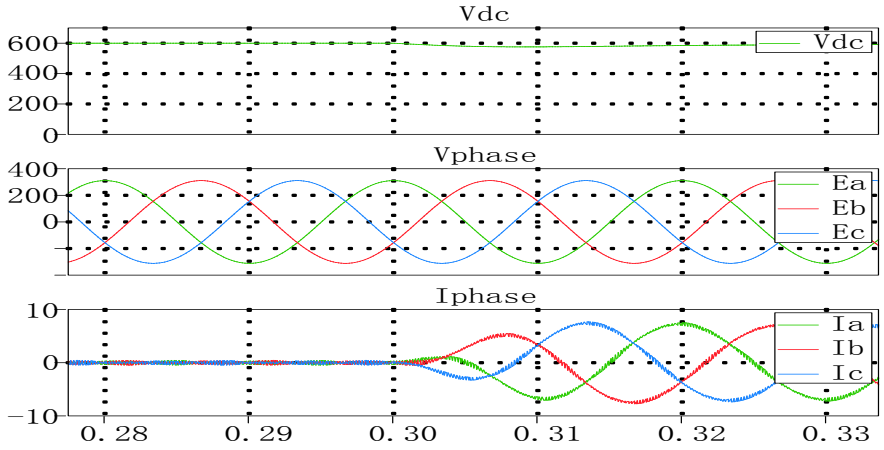

Figure 7. Waveform of DC Bus Voltage, AC Voltage and AC Current when No-load Suddenly Increase to Full Load

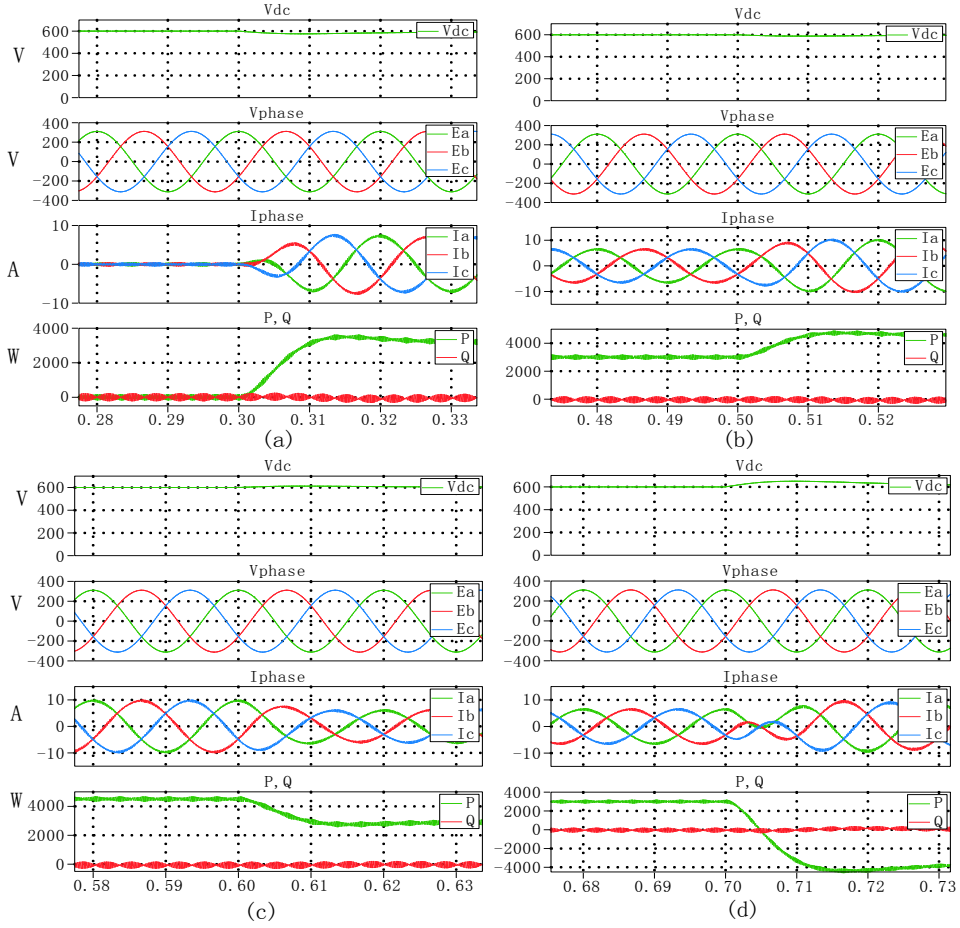

Figure 8. Waveform of AC Voltage and AC Current AC Current and Power of the Rectifier

5.2. Experimental Results

Figure 9 and Figure 10 show the experimental waveform of the rectifier DC bus voltage during startup and DC voltage and the AC side current of the rectifier from no load to full load. Figure the experimental results with the same operating condition and PI gains as those of the simulation.

The experimental waveform of DC bus voltage during the startup of three-level rectifier is shown in Figure9. The system is controlled to diode uncontrollable rectifier. The PWM rectifier will be started until DC bus voltage achieves stability. dc bus voltage until the charging resistance removed when a given value is reached. The experimental results show that the given value from the start to a stable value just needs less than 1s, furthermore, the system has very good rapidity and small overshoot. All this proved that the designed rectifier has good dynamic performance.

The DC bus voltage and current experimental waveform is shown in Figure10 for rectifier when the load is added from no-load to full load suddenly. From Figure10, we can see that the DC bus voltage is reduced about 20V under the condition of sudden increase load. But, we can also see that the DC bus voltage will recovery to given value within 1s, which proves that the rectifier has a good dynamic performance and the ability to resist interference. Furthermore, it can be seen that the current has the very good tracking performance. All the experimental results conform well to the simulation results. It can be, therefore, concluded that the design guideline is valid and application in practice.

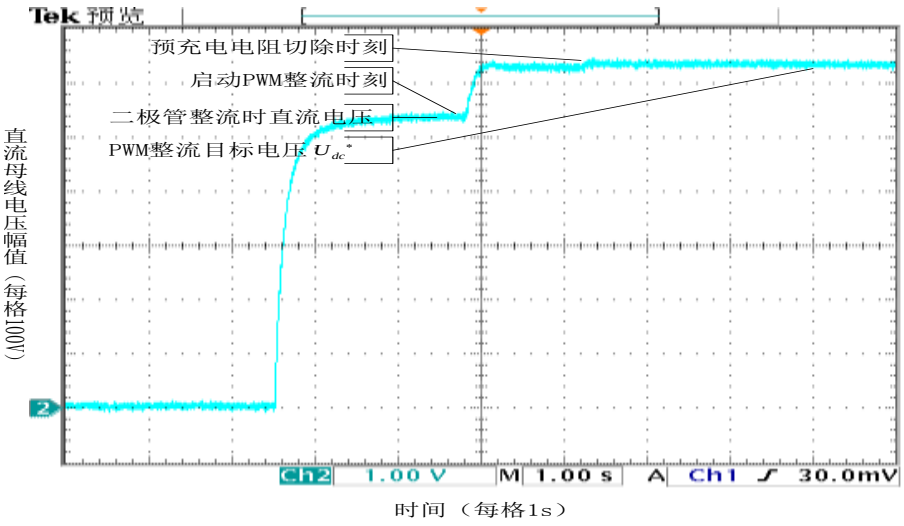

Figure 9. Experimental Waveform of the Rectifier DC Bus Voltage during Startup

6. Conclusion

In this paper, we have proposed design guidelines for dual close-loop of VSR. According this, PI gains are calculated by considering practice application. The approximate PI gains are selected to make the DC bus voltage can track the rated value from no-load to full load suddenly and assure the stability of system during startup. The current regulator and the voltage regulator have strong anti-interference ability and perfect dynamic response which can meet with the design requirements. The validity of the guidelines is verified by simulation and experiment.

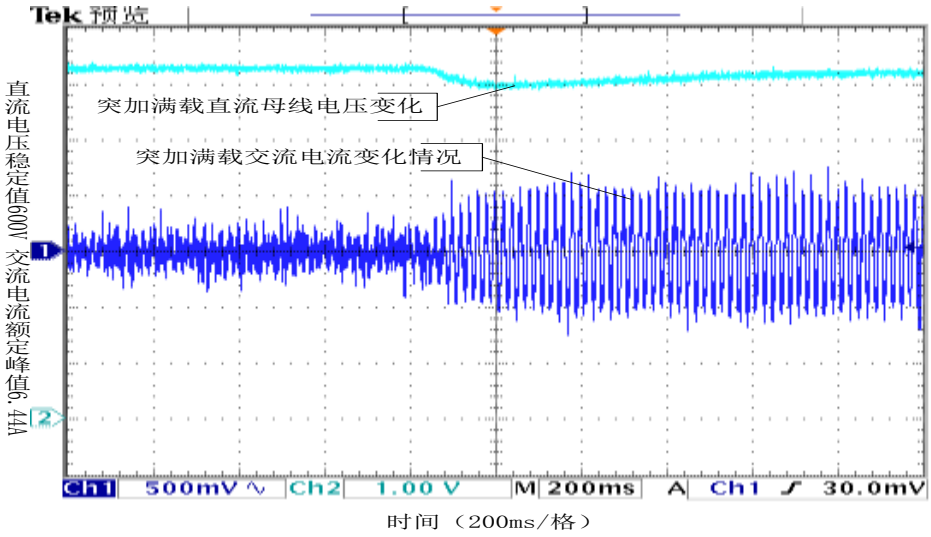

Figure 10. Experimental Waveform of DC Voltage and the AC Side Current of the Rectifier from No Load to Full Load

Acknowledgements

This work is supported by Program of Liaoning Provincial Key Laboratory of Functional Textile Materials, the National Natural Science Funds under 60474040 and Liaodong University Foundation of China under 2015JC005.

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