International Journal of Control and Automation
Vol. 10, No. 5 (2017), pp.135-146
http//dx.doi.org/10.14257/ijca.2017.10.5.13

An Optimized Phase Disposition Modulation for MMC and Capacitor Voltage Balancing Method

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Abstract

The modular multilevel converter (MMC) is one of the most potential converter topologies for high-voltage direct current (HVDC). The sub-module (SM) capacitor voltage balancing is a vital issue for MMC. The traditional PD modulation method requires the voltage sorting algorithm, leading to heavy computational burden when the number of SMs is large. This paper proposes an optimized phase disposition modulation and capacitor voltage balancing method. The SM capacitor voltages can be balanced excellently in steady state. It also can work in dynamic state when the capacitor voltages in upper/lower arm deviate from reference value. The proposed method neither requires the individual sorting of the SM capacitor voltage nor causes unnecessary switching actions. At last, both the simulation and experimental results verify the effectiveness and correctness of the proposed modulation and control method.

Keywords*: modular multilevel converter (MMC), capacitor voltage balancing, phase disposition modulation*

1 Introduction

With power electronic technology becoming more and more popular in energy conservation and intelligent power grid in recent years, multilevel converters have been the best choice to solve high voltage power conversion. The modular multilevel converter (MMC) topology has recently drawn huge interest in high-voltage applications. MMC was first proposed in [1] and regarded as one of the next-generation high-voltage multilevel converters without bulky transformer and filter [2-5].

Many papers and reports have been published on MMC in recent years. These papers mainly concentrated on modeling, pulse width modulation (PWM), voltage balancing, circulating current control, and so forth. Basic principles and modeling of operation about MMC are introduced in [6, 7]. Modulation methods are the key to the MMC's final performance. Currently, the main modulation strategies for the MMC are phase disposition PWM (PDPWM) [8], carrier phase-shifted PWM (CPS-PWM) [9], selective harmonic elimination PWM (SHEPWM) [10] and nearest level modulation (NLM) [11].

Voltage balancing of the floating sub-module(SM) capacitors influences on the stability of MMC, so it remains one of the major challenges. There are many researches in the past few years [12, 13]. The sorting method is adopted in [8] to keep the SM capacitor voltages balanced. This method is simple and practical, but the capacitors' voltage sorting would be a burden to the controller if the number of SMs is large. What's more, the strategy leads to extra switching actions.

A new voltage balancing control method is proposed in [14]. This method utilizes the carrier phase-shifted PWM to control high-frequency current components for capacitor voltage balancing in the MMC without measuring the arm currents. It can reduce the hardware requirement. However, the voltage sorting is still required, which can't reduce the computational complexity. An improved PD modulation method for MMC is proposed

ISSN: 2005-4297 IJCA

in [15, 16]. Its main idea is to change the bias of the carrier wave cycling. This method has no issues of capacitor voltage sorting. However, the strategy has the problem of extra switching actions, which increases the switching frequency and the switching losses of the converter.

To overcome the weakness of the aforementioned methods, this paper proposes an optimized phase disposition modulation and capacitor voltage balancing method. The method adopts certain algorithm which allocates reasonable carrier for each SM to keep the capacitor voltage balanced instead of sorting. In addition, it reduces switching frequency of the power device, without noticeably increasing the capacitor voltage ripples. This method also has the ability to keep the capacitor voltage balanced in dynamic state when the capacitor voltages of upper/lower arms deviate from reference value. Simulation and experimental results have both been presented to justify the proposed control and modulation method.

2. Basic Principle of MMC

Figure 1 illustrates the topology of MMC. The typical structure of MMC is shown in Figure 1a). Each phase consists of two arms, upper and lower. Each arm has N SMs and one inductor (L_0). Figure 1b) depicts a scheme representation of the SM, which is composed of two IGBT switches S1 and S2, two anti-parallel diodes D1 and D2, and a capacitor C. The two switches (S1 and S2) in each SM are controlled with complementary signals and produce two active switching states that can realize each SM be connected or bypassed to the converter.

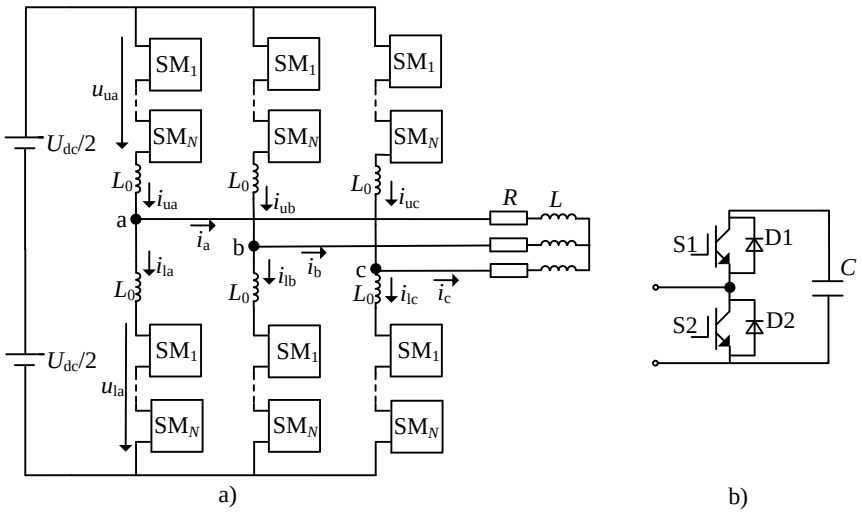


Figure 1. Topology of MMC a) Typical Structure of MMC b) Structure of SM

Based on Figure 1 and literature [17], the mathematical equations of phase j (j=a, b, c) are as follows:

$$\frac{U_{\mathrm{dc}}}{2} - u_{\mathrm{uj}} - L_o \frac{di_{\mathrm{uj}}}{dt} = u_j \tag{1a}$$

$$-\frac{U_{\mathrm{dc}}}{2} + u_{\mathrm{lj}} + L_o \frac{di_{\mathrm{lj}}}{dt} = u_j \tag{1b}$$

$$i_j = i_{\mathrm{uj}} - i_{\mathrm{lj}} \tag{2a}$$

$$i_{zj} = \frac{1}{2}(i_{\mathrm{uj}} + i_{\mathrm{lj}}) \tag{2b}$$

where U_{dc} is the dc-bus voltage. u_{uj} and u_{lj} represent the sum of the voltage of the

switched-on SMs in the upper arm and lower arm of phase *j*. i_{uj} and i_{lj} are the upper arm current and the lower arm current of phase *j*. u_j and i_j stand for the output voltage and output current of phase *j*. i_{zj} is circulating current of phase *j*.

Substituting (2a) into the sum of (1a) and (1b) yields

$$u_j = \frac{1}{2}(u_{uj} - u_{lj}) - \frac{L_0}{2}\frac{di_j}{dt} \tag{3}$$

Substituting (2b) into the difference between (1a) and (1b) yields

$$\frac{U_{dc} - (u_{uj} + u_{lj})}{2} = L_0 \frac{di_{zj}}{dt} \tag{4}$$

The value of arm inductor (L_0) is generally small in MMC, and the output current is relatively smooth. So the voltage of the arm inductor can be ignored, namely the second part on the right side in expression (3). The output voltage can be approximately expressed as

$$u_j = \frac{1}{2}(u_{uj} - u_{lj}) \tag{5}$$

At the same time, the dc-bus voltage and the sum of the upper and lower arm capacitor voltages should be kept balanced, otherwise, an enormous current shock will occur in the circulating current. Expression (4) can be approximately rewritten as

$$U_{dc} = u_{uj} + u_{lj} \tag{6}$$

Generally, the reference output voltage for phase *j* of MMC can be expression

$$u_{j\_ref} = m\frac{U_{dc}}{2}\cos\left(\omega t + \varphi_j\right) \tag{7}$$

where m ($0 \le m \le 1$) is the modulation index and φ_j represents the angular displacement of the fundamental frequency.

From (5)-(7), the reference voltage for the upper and lower arms can be expressed as

$$\begin{cases} u_{uj\_ref} = \dfrac{U_{dc}}{2} - u_{j\_ref} = \dfrac{U_{dc}}{2} - m\dfrac{U_{dc}}{2}\cos\left(\omega t + \varphi_j\right) \\ u_{lj\_ref} = \dfrac{U_{dc}}{2} + u_{j\_ref} = \dfrac{U_{dc}}{2} + m\dfrac{U_{dc}}{2}\cos\left(\omega t + \varphi_j\right) \end{cases} \tag{8}$$

3 Phase Disposition Modulation for MMC

3.1. Conventional Phase Disposition Modulation

Phase disposition (PD) modulation is one of the most important modulation methods for MMC, which has detailed analysis in [8]. This method can generate an output voltage with maximally 2*N*+1 levels. At first, the reference voltage of the upper or lower arms u_{xj_ref} (*x*=u, l; *j*=a, b, c) divided the reference SM capacitor voltage U_{C_ref} to get *m*. Then the capacitor voltages are sorted. When the i_{xj} (*x*=u, l; *j*=a, b, c) is positive or zero, the *floor(m)* SMs are turned on whose capacitor voltage are relatively lower in this arm, and the *n- floor(m)*-1 SMs will be bypassed whose capacitor voltage are relatively higher in this arm, and the last SM will be PWM-switched in this arm. The opposite thing happens when the i_{xj} (*x*=u, l; *j*=a, b, c) is negative. This modulation method keeps the SM capacitor voltage balanced through sorting. If the bubble method is used to sort, the number of sorting time in each arm is *T*:

$$T = (N-1) + (N-2) + \cdots + 1 = \frac{N(N-1)}{2} \tag{9}$$

It can be seen that a large number of sorting times causes the computation of the controller greatly increased when the number of SM is enormous. To solve this matter, this paper proposes an optimized PD modulation, which can balance the SM capacitor voltages without sorting.

3.2. Optimized Phase Disposition Modulation

Illustration of the optimized PD modulation will be based on 4 SMs in each arm, the upper arm PD modulation scheme of phase a is shown in Figure 2.

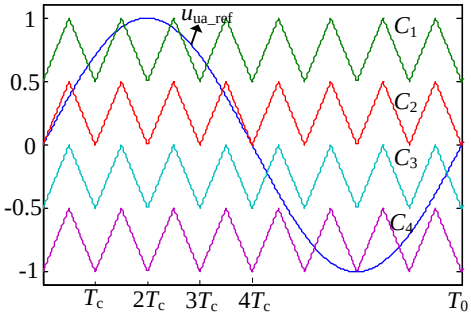


Figure 2. PD Modulation Scheme

For the convenience of narrative, the modulation frequency ratio k_c can be defined as

$$k_c = \frac{f_c}{f} \tag{10}$$

where f and f_c are the fundamental frequency of output voltage and the frequency of the carrier signals respectively.

Optimized PD modulation adopts the following steps to implement, choosing the upper arm of phase-a as an example.

1) First of all, the SM capacitor voltages in this arm are compared to each other (U_{Cua1}, U_{Cua2}, U_{Cua3}, U_{Cua4} are the upper arm capacitor voltages of phase-a). The corresponding module serial numbers of the maximum and minimum capacitor voltages can be obtained. Then these serial numbers are stored into matrix A. Suppose A(1) is the serial number of the maximum capacitor voltage, and A(4) is the serial number of the minimum capacitor voltage. The rest of serial numbers stored into A(2) and A(3) by descending order. For example, the value of U_{cua2} is highest and the value of U_{cua3} is lowest. Then we can get A(1) and A(4) are 2 and 3 respectively. The value of A(2) and A(3) are 4 and 1 respectively.

2) In order to keep the SM capacitor voltage balanced, a count-up counter which ranges from 0 to k_c is generated. Its frequency should be the same as the frequency of modulation wave. The value of the count-up counter is different in each carrier period T_c. Define the following variable:

$$k_{c\_rem} = k_c \% (n-2) = k_c \% 2 \tag{11}$$

where k_{c_rem} is the complementary function of the modulation frequency ratio k_c.

According to the Equation (11), the pulses in each carrier period T_c are shown in Figure 3.

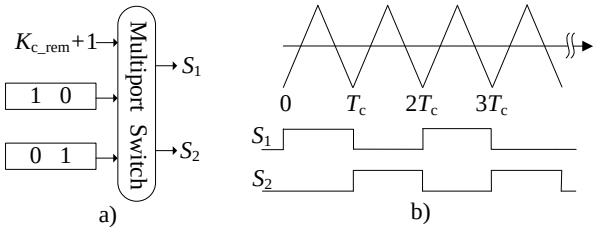


Figure 3. Pulses in Each Carrier Period T_c a) Choose Pulse According to k_{c_rem} b) The Pulses of S1, S2

Assuming the matrix A is consistent with step 1). When the upper arm current of phase-a i_{ua} is positive or zero, carrier distribution is shown in Table 1. Then the carrier of each SM ($C_{ua}(1)$, $C_{ua}(2)$, $C_{ua}(3)$, $C_{ua}(4)$) can be obtained, which is shown in Table 2. The carrier of each SM can be expressed as

$$\begin{cases} C_{ua}(1) = C_{ua}\left(\mathrm{A}(3)\right) = C_3S_1 + C_2S_2 \\ C_{ua}(2) = C_{ua}\left(\mathrm{A}(1)\right) = C_1S_1 + C_1S_2 \\ C_{ua}(3) = C_{ua}\left(\mathrm{A}(4)\right) = C_4S_1 + C_4S_2 \\ C_{ua}(4) = C_{ua}\left(\mathrm{A}(2)\right) = C_2S_1 + C_3S_2 \end{cases} \tag{12}$$

Table 1. Carrier Distribution When i_{ua} Is Positive or Zero

	T_c	$2T_c$	$3T_c$
A(1)	C_1	C_1	C_1
A(2)	C_2	C_3	C_2
A(3)	C_3	C_2	C_3
A(4)	C_4	C_4	C_4
			Repeat T_c

Table 2. Carrier of Each SM When i_{ua} Is Positive or Zero

	T_c	$2T_c$	$3T_c$
$C_{ua}(1)$	C_3	C_2	C_3
$C_{ua}(2)$	C_1	C_1	C_1
$C_{ua}(3)$	C_4	C_4	C_4
$C_{ua}(4)$	C_2	C_3	C_2
			Repeat T_c

When the upper arm current of phase-a i_{ua} is negative, carrier distribution is shown in Table 3. Then the carrier of each SM ($C_{ua}(1)$, $C_{ua}(2)$, $C_{ua}(3)$, $C_{ua}(4)$) can be obtained, which is shown in Table 4. The carrier of each SM can be expressed as

$$\begin{cases} C_{ua}(1) = C_{ua}\left(\mathrm{A}(3)\right) = C_2S_1 + C_3S_2 \\ C_{ua}(2) = C_{ua}\left(\mathrm{A}(1)\right) = C_4S_1 + C_4S_2 \\ C_{ua}(3) = C_{ua}\left(\mathrm{A}(4)\right) = C_1S_1 + C_1S_2 \\ C_{ua}(4) = C_{ua}\left(\mathrm{A}(2)\right) = C_3S_1 + C_2S_2 \end{cases} \tag{13}$$

Table 3. Carrier Distribution When i_{ua} Is Negative

	T_c	$2T_c$	$3T_c$
A(1)	C_4	C_4	C_4
A(2)	C_3	C_2	C_3
A(3)	C_2	C_3	C_2
A(4)	C_1	C_1	C_1
			Repeat T_c

Table 4. Carrier of Each SM When i_{ua} Is Negative

	T_c	$2T_c$	$3T_c$
$C_{ua}(1)$	C_2	C_3	C_2
$C_{ua}(2)$	C_4	C_4	C_4
$C_{ua}(3)$	C_1	C_1	C_1
$C_{ua}(4)$	C_3	C_2	C_3
			Repeat T_c

3) It is clear that the carrier is changing frequently in continuous carrier cycles from the above analysis. While the value of the modulation wave changed little in two continuous carrier cycles, leading to extra switching actions. This paper adopts the following way to improve [18]. Define the voltage deviation between the actual voltage U_C and reference voltage U_{C_ref} of each SM is ΔU and it can be expressed as

$$\Delta U = \left| U_C - U_{C\_ref} \right| \tag{14}$$

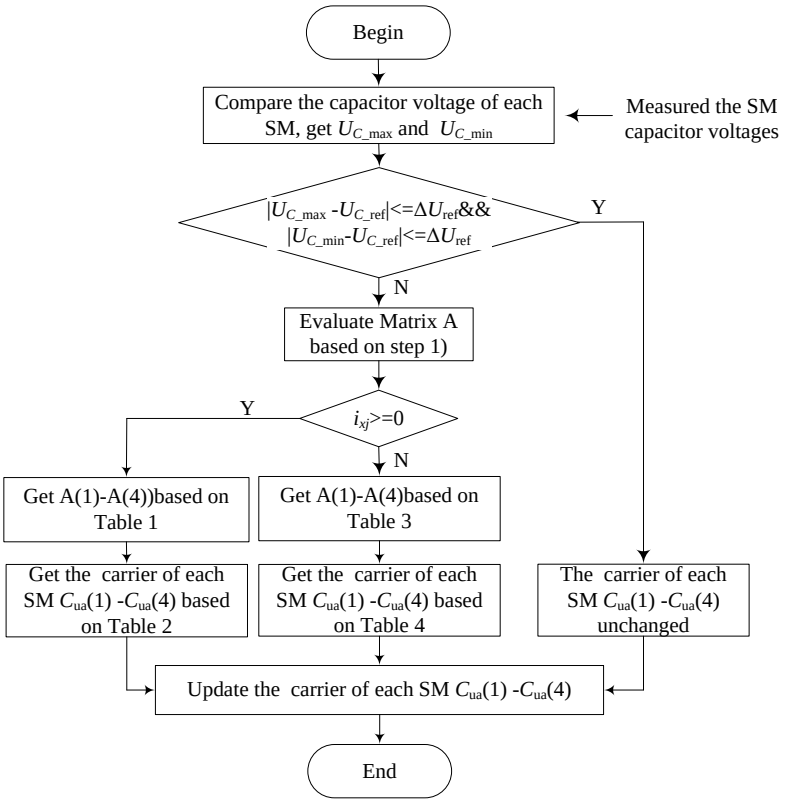


Figure 4. Flow Chart of the Optimized PD Modulation

ΔU_{ref} is the prespecified value which is the allowable range for the variation of the capacitor voltage deviation. By comparing the capacitor voltage has been get the

maximum voltage U_{C_max} and minimum voltage U_{C_min} in step 1). It is obvious that their voltage deviation ΔU is larger than the voltage deviation of other SMs. So we only need to calculate theirs voltage deviation ΔU. If their voltage deviation ΔU is less than the prespecified value ΔU_{ref}, the output carrier remains the same as last carrier cycle, otherwise the output carrier obeys the step 1) and step 2).

The flow chart of the optimized PD modulation is shown in Figure 4. Through the above analysis with the optimized PD modulation only obtain the maximum and the minimum capacitor voltages. The number of each arm sorting times is 2(N-1) in one sampling period. Compared with the conventional PD modulation whose sorting times is N(N-1)/2, the optimized PD modulation reduces the computation of the controller obviously, especially when the number of SM is extremely large. Figure 5 is the number of sorting times trend comparison of traditional method and optimized method.

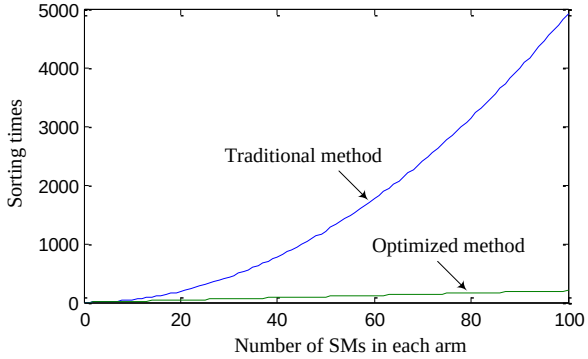


Figure 5. Number of Sorting Times Trend Comparison of Traditional method and Optimized Method

4. Simulation Results

In order to verify the validity of the optimized PD modulation, a three phase MMC has been built in Matlab/Simulink software. The parameters are shown in Table 5.

Table 5. Parameters of Three Phase MMC for Simulation

Parameter	Value
modulation index, m	0.8
No. of SMs in each arm, N	4
DC-bus voltage, U_{dc}	800V
Carrier frequency, f_c	2kHz
Arm inductance, L_0	5mH
SM capacitor, C	1.88mF
Load resistance, R	25Ω
Load inductance, L	5mH

In order to verify the optimized PD modulation can reduce the switching frequency, a five-level MMC simulation model was built. The prespecified value ΔU_{ref} which is equal to 0, 5V and 10V respectively was carried out in the same conditions. Figure 6 is the simulation waveforms of the capacitor voltages and gate signals of one power device. Figure 6a) b) c) compare the capacitor voltages of the upper arm SM of phase-a for three cases, that is, the prespecified value ΔU_{ref} is equal to 0, 5V and 10V. As shown, the capacitor voltages for all cases are balanced at its reference value. However, the capacitor voltage ripple is largest when the prespecified value ΔU_{ref} is 10V. Figure 6d) e) f) compare the gate signals of one power device for three cases. Figure 6d) shows the gate

signals of one power device when the prespecified value ΔU_{ref} is 0, namely the reduction of switching frequency is not taken into consideration. In this case, the output carrier is different from last carrier cycle, leading to high switching frequency. Figure 6e) shows the gate signals of one power device when the prespecified value ΔU_{ref} is 5V. Compared with Figure 6d), the frequency f_{sw} is reduced from 936Hz to 522Hz. Figure 6f) shows the gate signals of one power device when the prespecified value ΔU_{ref} is 10V, and the frequency f_{sw} is reduced further.

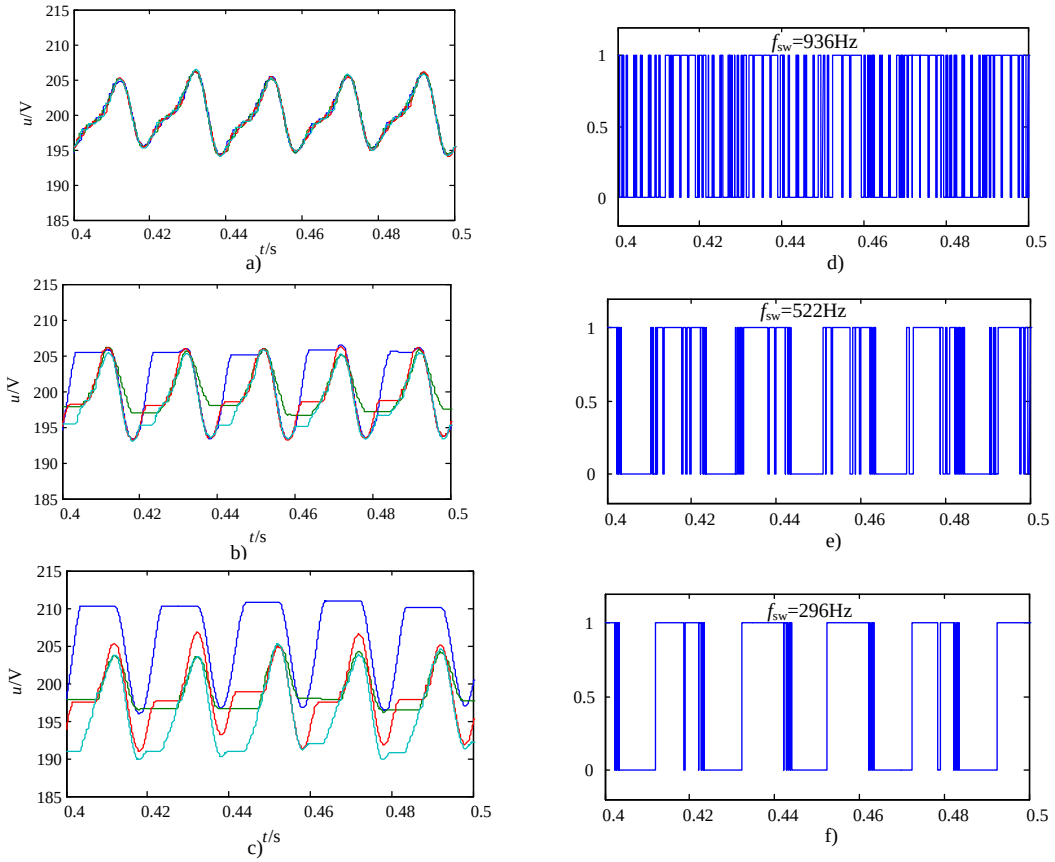


Figure 6. Simulation Waveforms of the Capacitor Voltages a) ΔU_{ref} =0 b) ΔU_{ref} =5V c) ΔU_{ref} =10V and Gate Signals of One Power Device d) ΔU_{ref} =0 e) ΔU_{ref} =5V f) ΔU_{ref} =10V

Figure 7 is the simulation waveforms when the prespecified value ΔU_{ref} is 5V. Figure 7a) and Figure 7b) shows the upper and lower arm SM capacitor voltages. All the capacitor voltage average 200V with roughly 10V peak-to-peak ripple, indicating the optimized PD modulation can keep SM voltage balanced. Figure 7c) and Figure 7d) show the output voltage and the output current respectively.

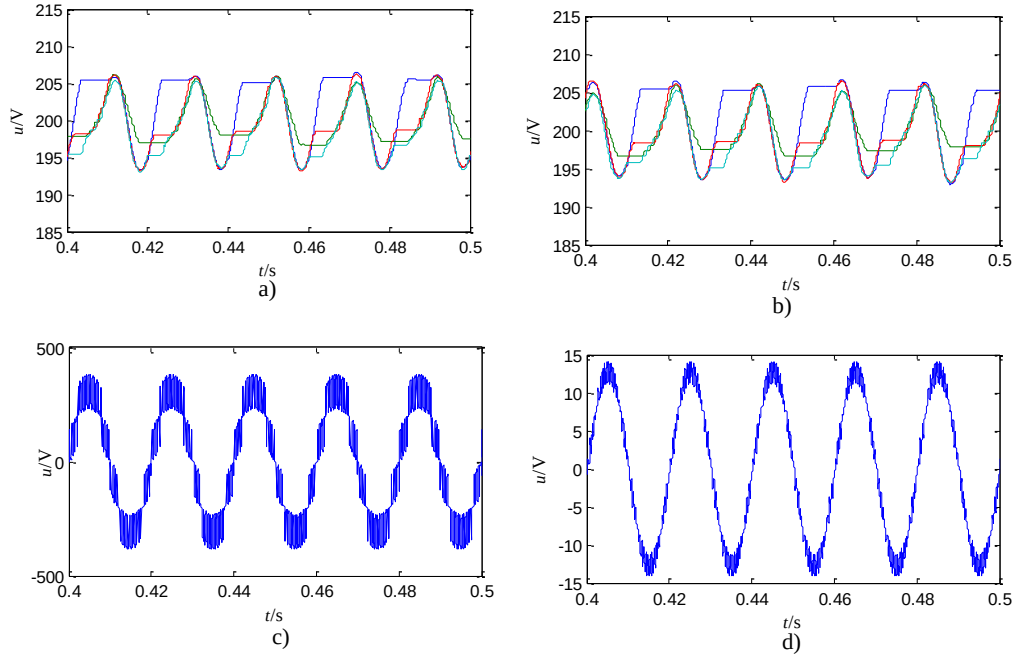
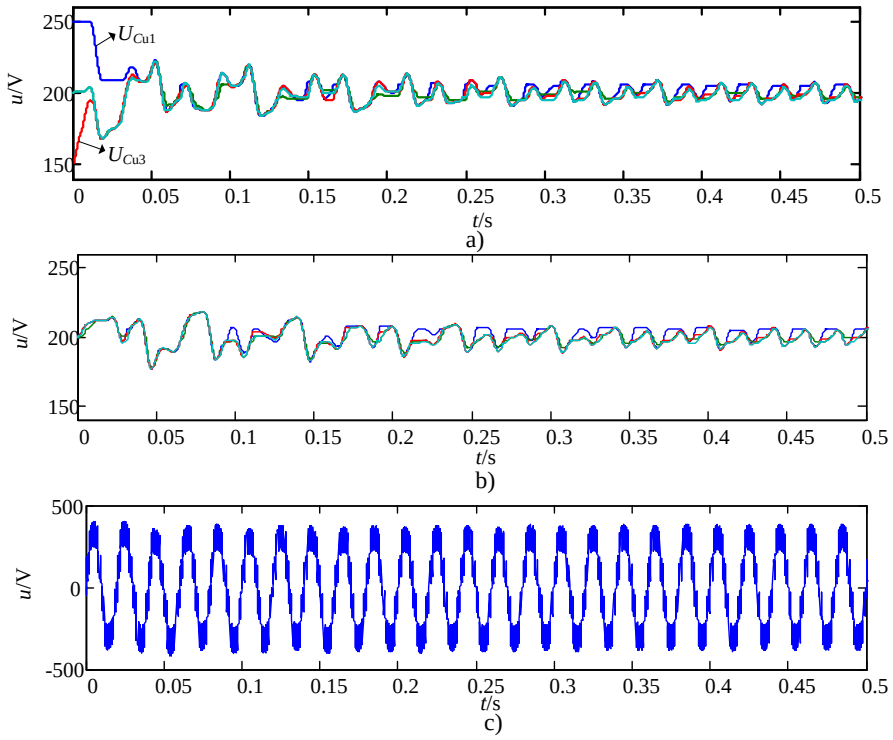


Figure 7. Simulation Waveforms with the Optimized PD Modulation in Steady State a) Upper Arm SM Capacitor Voltages b) Lower Arm SM Capacitor Voltages c) Output Voltage d) Output Current

Assuming that the capacitor voltage of SM1 is deviated to 250V, and the voltage of SM3 is deviated to 150V. Figure 8 is the simulated waveforms with the optimized PD modulation. Figure 8a) and Figure 8b) show the upper and lower arm SM capacitor voltages. It is clear that the voltages of SM1 and SM3 are balanced. Figure 8c) and Figure 8d) show the output voltage and output current respectively.



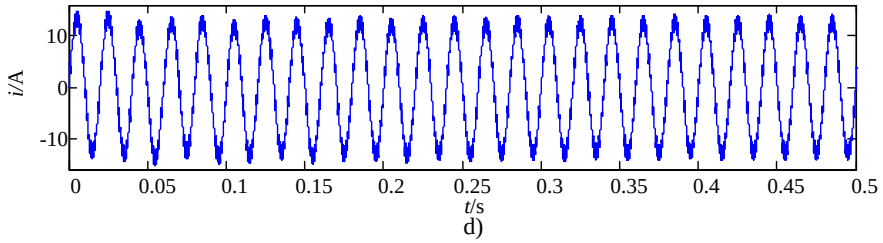


Figure 8. Simulation Waveforms with the Optimized PD Modulation in Dynamic State a) Upper Arm SM Capacitor Voltages b) Lower Arm SM Capacitor Voltages c) Output Voltage d) Output Current

5. Experimental Results

A down-scaled prototype of three phase MMC has been implemented to validate the optimized PD modulation. The experimental parameters are listed in Table 6. The main modulation and control algorithms are implemented with a TI TMS320F28335 DSP and a Xilinx XC3S400 FPGA.

Table 6. Parameters of Three Phase MMC for Experiment

Parameter	Value
modulation index, m	0.9
No. of SMs in each arm, N	4
DC-bus voltage, U_{dc}	100V
Arm inductance, L_0	5mH
SM capacitor, C	1.88mF
Load resistance, R	25Ω
Load inductance, L	15mH

Figure 9 shows the experimental results with the optimized PD modulation in steady state. Figure 9a) is the upper arm capacitor voltages of phase-a. Figure 9b) gives the output voltage and output current. It is clear that the SM capacitor voltages are balanced. In addition, the MMC is operating with the expected performance.

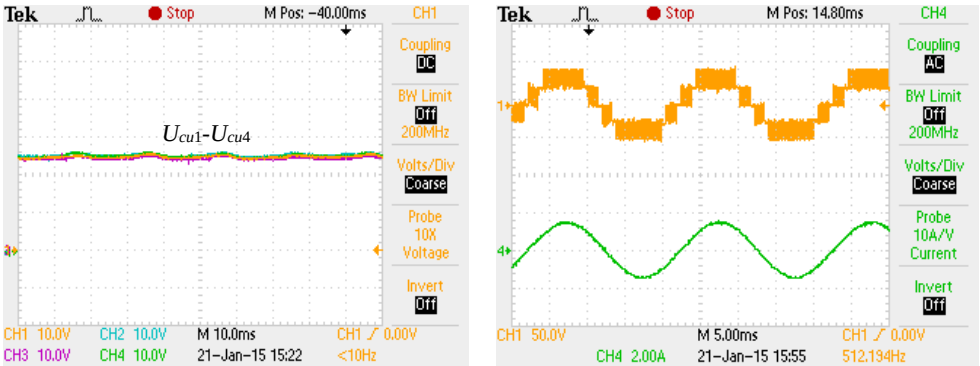
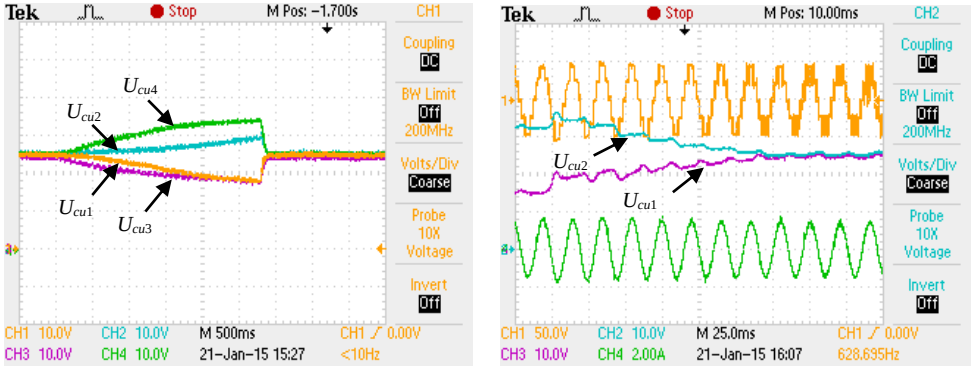


Figure 9. Experiment Waveforms with the Optimized PD Modulation in Steady State a) Capacitor Voltages b) Output Voltage and Output Current

Figure 10 shows the experimental results with the optimized PD modulation in dynamic state. At first, the capacitor voltages are kept balanced. Then make some SM capacitor voltages deviation artificially. As a consequence, the capacitor voltages U_{Cu2} and U_{Cu4} will be increased gradually, and the voltages U_{Cu1} and U_{Cu3} will be reduced gradually.

After the optimized PD modulation is enabled again, the capacitor voltages are balanced again, as shown in Figure 10a). Figure 10b) gives the capacitor voltages U_{Cu1}, U_{Cu2} and the output voltage, output current when the optimized PD modulation is enabled again. The waveforms show that the output power quality is not affected.



a) b)

Figure 10. Experiment Waveforms with the Optimized PD Modulation in Dynamic State a) Capacitor Voltages b) Output Voltage, Output Current and Capacitor Voltages

6. Conclusions

This paper proposes an optimized PD modulation and capacitor voltage balancing method. The SM capacitor voltages can be balanced excellently in steady state. It also can work in dynamic state when the capacitor voltages in each arm deviate from reference value. The proposed method does not require the individual sorting of the SM capacitor voltages, which reduce the control system complexity and computational burden. Furthermore, it avoids unnecessary switching actions, which reduce the switching losses of the converter. To validate the proposed method, the simulation and experiments are respectively conducted in Matlab/Simulink and prototype. The SM capacitor voltages can be well balanced in steady state as well as dynamic state. The results show that the proposed method is feasible and correct.

Acknowledgments

This research was supported by the Qinglan Project of Jiangsu Province and the Graduate Student Research and Innovation Program of Jiangsu Province (KYLX_1384).

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