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Design of Novel Low-power and High-efficiency Class-D Audio Amplifier

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Abstract

This study develops and evaluates a novel architecture for class-D CMOS power amplifier. In this new architecture all stages of class-D amplifier are designed carefully. A second order delta sigma modulation, high switching frequency and three passive feedbacks are used in modulation stage. A special filter is designed to improve the quality of this system. This paper idea is simulated using MATLAB. The simulation results show that the developed class-D CMOS power amplifier architecture has low THD (<0.001), High SNR (>80dB), and high efficiency (>95%), which show that this new architectural design for class-D amplifier has the best performance in terms of THD, and efficiency in comparison with other class-D CMOS power amplifier architectures.

Keywords*: Class-D CMOS power amplifier, THD, SNR, Efficiency, Power amplifier*

1. Introduction

In the last decades, high power audio amplifiers have been widely used in our life [1]. The goal of amplifiers is to reproduce the input signal with the desired power and quality in the output [1]. Audio amplifiers can be categorized in 5 groups: (a) class-A, that consist of a simple Bipolar Junction Transistor (BJT), which is shown in Figure1, (b) class-B, (c) class-AB, (d) class-C, and (e) class-D CMOS power amplifiers [2].

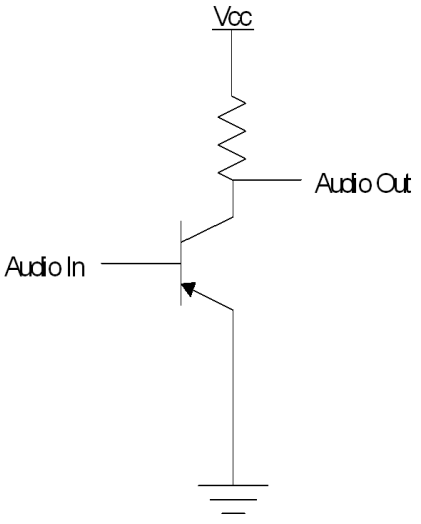

Figure 1. The Architecture of Class-A CMOS Amplifier [2]

The efficiency of these amplifiers is less than 50% [1, 3].

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To improve amplifiers' quality, several system configurations have been utilized such as class-A, class-B or class-AB CMOS power amplifiers, but the efficiency of these linear amplifiers is less than 78% [2]. To achieve higher efficiency and improve the quality of amplifiers, the class-D configuration can be utilized [4]. The class-D configuration contains three main stages: (a) modulation stage, (b) power stage, and (c) filtering stage [4].

The utilized method in the modulation stage can be divided into two categories: (a) Pulse Width Modulation (PWM) [3], and (b) Pulse Density Modulation (PDM) such as delta sigma modulator [4]. In the PWM modulation, the comparator generates a pulse signal, but this method leads to unwanted signals and harmonics due to carrier signal's low frequency [5].

On the other hand, the PDM method is utilized to design low power amplifiers. However, unwanted harmonic in this method is lower than the PWM method [6]. Several methods and structures have been proposed to increase class-D CMOS power amplifiers' efficiency [7-21].

In this study, a novel design is presented and evaluated for the PDM class-D CMOS power amplifier. Modulation stage is composed of a second order delta sigma modulator with three state feedbacks. The power stage configuration and component are designed very carefully. The filtering stage is designed to improve the output quality with respect to the power stage output. The proposed architecture for class-D CMOS power amplifier was simulated using MATLAB. Based on our simulation results, the developed architecture for class-D CMOS power amplifier has several advantages compared to other class-D audio amplifiers in [17 - 21]

The remaining of this study is organized as follows: Section 2 provides the background of class-D amplifier. In Section 3, the proposed method is discussed and simulated. Section 4 compares the developed class-D CMOS power amplifier with other class-D amplifiers. Finally, this study is concluded in Section 5.

2. Background

2.1. Class-D amplifier

Figure2 shows the block diagram of a simple PDM class-D audio amplifier [7, 9].

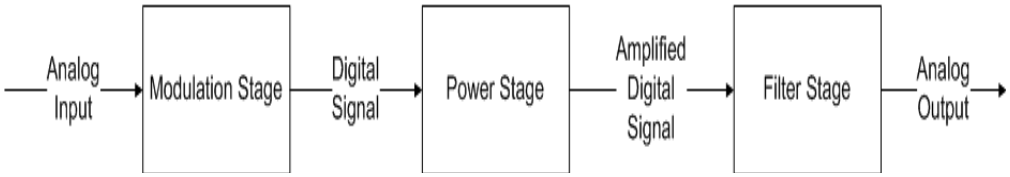

Figure 2. A Simple PDM Class-D Audio Amplifier Block Diagram [7, 9]

As it is shown in Figure2, this type of amplifier has multiple stages. Note that to have better output and improve the efficiency of this amplifier, these stages should be optimized. Figure3 shows a simple class-D CMOS power amplifier with an LC filter [8].

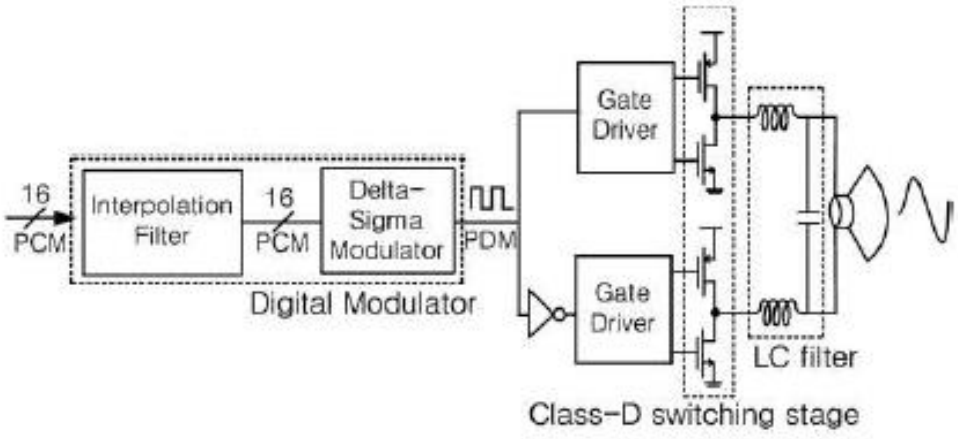

Figure 3. A Simple Class-D Audio Amplifier Using LC Filter [9]

The first block of this Figureis used to modulate and convert the input analog signal into a digital signal. Then, the modulated signal is applied to the gate of Metal Oxide Field Effect Transistors (MOSFETs). The power stage, class-D switching stage, is responsible for increasing the power of achieved signal [10]. The most important factor for these MOSFETs is their triode region. This factor must be decreased as much as possible [11].

2.2. PDM Method

The first order delta sigma modulation with one state feedback block diagram is shown in Figure4 [14].

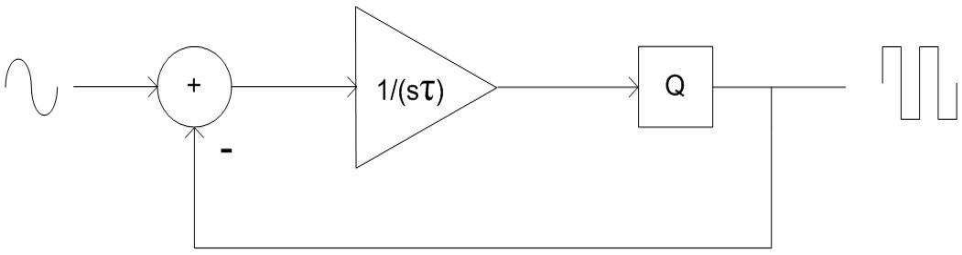

Figure 4. First Order Delta Sigma Modulation Block Diagram [14]

Figure5 shows the utilized circuit for first order delta sigma modulation. This architecture is simulated using Proteus.

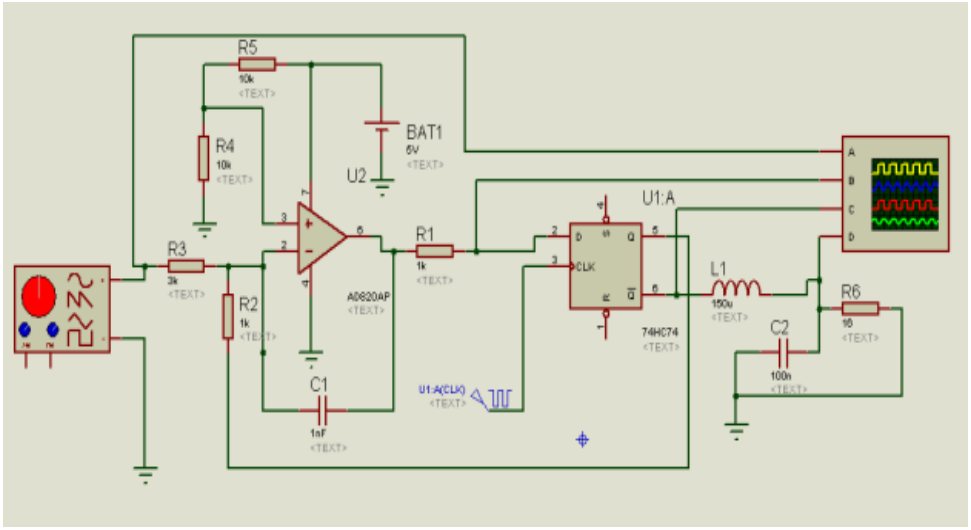

Figure 5. First Order Delta Sigma Modulation with One State Feedback

The results of this simulation are shown in Figure6.

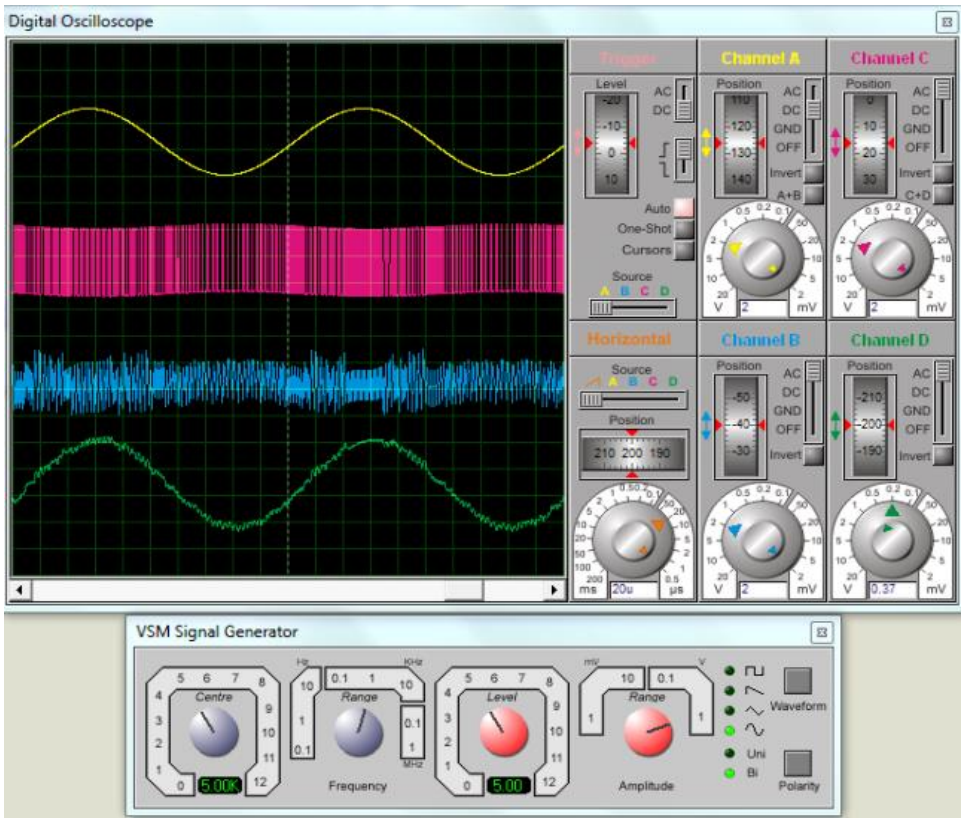

Figure 6. Result of First Order Delta Sigma Modulation with One State Feedback

It should be noted that the quantize complexity and non-linearity can be a source of some disturbance in the output. To simulate a first order delta sigma modulation with consideration of these unwanted signals, a simple noise signal is added as an input to this system. This system formula is shown as follows [14]:

$$V_{OUT} = \left[\frac{1}{1+sT}\right]V_{IN} + \left[\frac{sT}{1+sT}\right]\epsilon \quad (1)$$

To gain a perfect output, it is needed to push the noise far from audio band and filter it at filtering stage [15]. This equation shows that by finding the perfect frequency for modulation, it may be possible to filter this unwanted noise.

2.3. The Power Stage

There are two configurations for power stage in class-D amplifiers: (a) half-bridge configuration, and (b) full-bridge configuration. In both of these configurations, the main purpose is done by MOSFETs and their drivers. To improve this stage performance, the used MOSFETs must be chosen carefully and for high efficiency purpose, some of new designed MOSFETs are used and their results are compared to achieve the best possible output. Full-bridge configuration has more components compared to half-bridge configuration, but in audio amplifiers, it is needed to cancel DC offsets and harmonic distortion. This problem can be solved only in full-bridge configuration. So, the full-bridge configuration is suitable for class-D amplifier. Figure7 shows a simple full-bridge configuration [16].

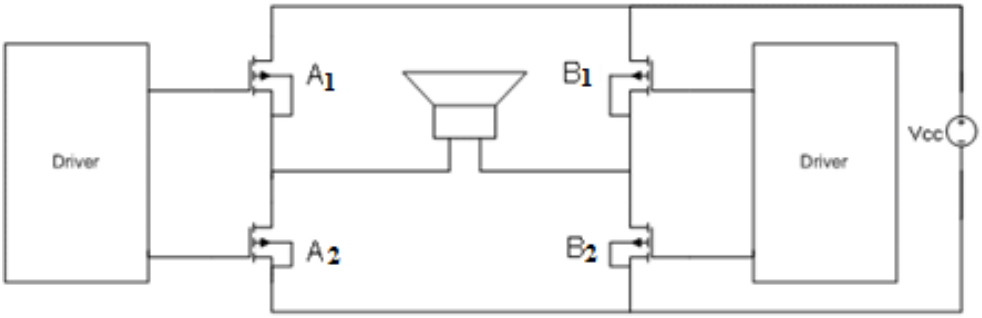

Figure 7. A Simple Full-Bridge Configuration [16]

As it is shown in Figure7, in full-bridge configuration, two MOSFETs are in on-state, for example A_1 and B_2, and the other MOSFETs are in off-state, A_2 and B_1 [15]. The most important rule to follow is that, A_1 and A_2 or B_1 and B_2 should never be in on-state at the same time. To control the MOSFETs, a circuit called MOSFET's driver is needed. This circuit must be designed based on the MOSFET's characteristics such as MOSFET's gate capacitance (C_g) or drain source resistance (r_{ds}) [16].

2.4. The Filter Stage

At this stage any unwanted noise or signal must be filtered before they reach the output. After the input signal is modulated and amplified, it would be still in digital form and speaker's input must be an analog signal [17]. Before choosing a suitable filter, it is important to evaluate system's output. To test and evaluate a system output's quality, three factors must be calculated: (a) Total Harmonic Distortion (THD), (b) Spurious Free Dynamic Range (SFDR) and (c) Signal to Noise Ratio (SNR) [6].

SNR is used to determine the power of signal in relation to noise's power and it is formulated as follows [6]:

$$SNR = 10\ log\ \frac{P_{signal}}{P_{noise}} \quad (2)$$

SNR measures the noise power in the background, which is in audio range, and compares it with the main signal [6].

SFDR is a very important parameter, which is used when an Analog to Digital Converter (ADC) is utilized in system [18]. This evaluation is used to determine the ratio

between desired signal and any unwanted signals, which may be the results of harmonics or system complexity [19]. Sometime SFDR is the result of a harmonic, but to evaluate the ratio between all of the harmonics and output another parameter is used, which is called THD [15, 17]. This two parameters depend on modulation technique and the complexity of system.

Filters are divided into two categories: (a) passive filter and (b) active filter. Passive filters contains only passive component such as capacitors, inductors and resistors, where active filters contains active components.

3. The Proposed Model

This study proposes a novel class-D CMOS power amplifier. In the developed class-D CMOS power amplifier, all amplifier stages are carefully designed as follows.

3.1. The Modulation Stage

Figure8 shows the modulation stage in the developed class-D CMOS power amplifier.

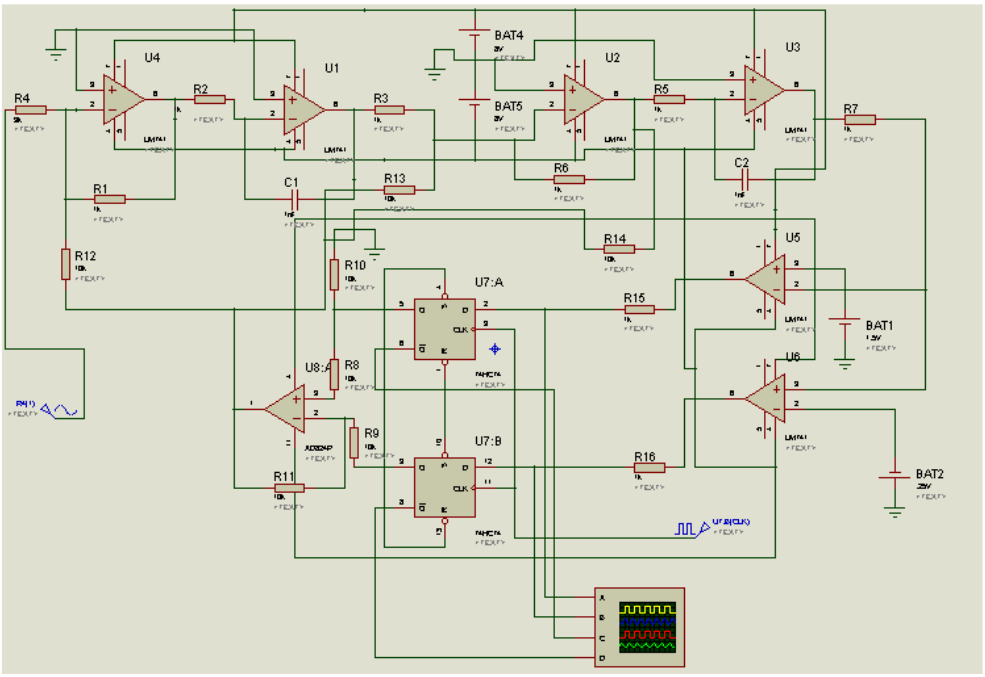

Figure 8. The Utilized Circuit for the Modulation Stage of the Developed Class-D CMOS Power Amplifier

An integrator is added to the first order delta sigma modulator. Therefore, it is changed into a second order delta sigma modulator. So, this new system can have two or three feedbacks to have a steady state output. The output is improved slightly, but it is not enough; however, when the value of three feedback resistors is changed, a steady state signal with a good quality is achieved in the output. This system model is simulated in MATLAB. Figure9, shows the utilized model in MATLAB.

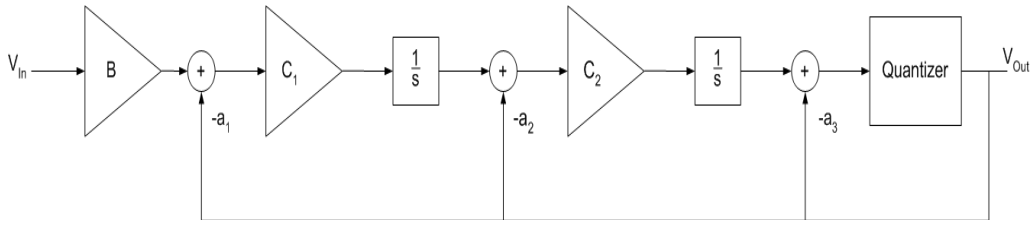

Figure 9. Delta Sigma Modulation with Three State Feedbacks

By changing each parameter of the modulation stage, the signal of output is also changed. Therefore, the modulation output quality varies. To determine the value of each coefficient, all of these parameters are changed in MATLAB to have a steady state system with a good quality output signal. It should be noted that these values can be changed if the following term's value remains the same $-a_3.s^2$, $-a_2.C_2.s$, $-a_1.C_1.C_2$ and B.C1.C2. This stage output is given in Figure10.

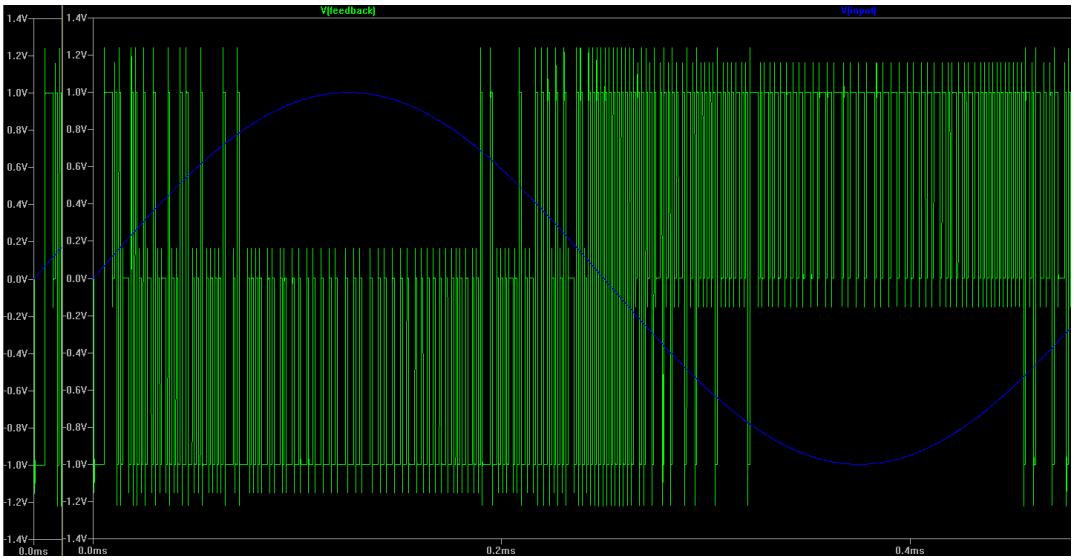

Figure 10. Second Order Delta Sigma Modulation Output

The modulator frequency has an important role in the performance of the class-D CMOS power amplifier. If an extremely high frequency is used for modulator, the component might break down, but these high frequencies have never been used, due to system's limitation. To find the best modulation frequency, first the other two stage's configuration must be designed, and then in relation to the output efficiency and quality, each stage's parameters would be determined.

3.2. The Power Stage

In this paper, we utilized full-bridge configuration to increase the efficiency of the proposed amplifier. So, an inverted form of the input is shown in the output with the amplitude of 45v. This result concluded that this stage works properly.

As it is explained before, a very important part of the power stage is MOSFET's driver. To drive these MOSFETs, a new circuit should be designed. The utilized circuit for the MOSFET driver is shown in Figure11.

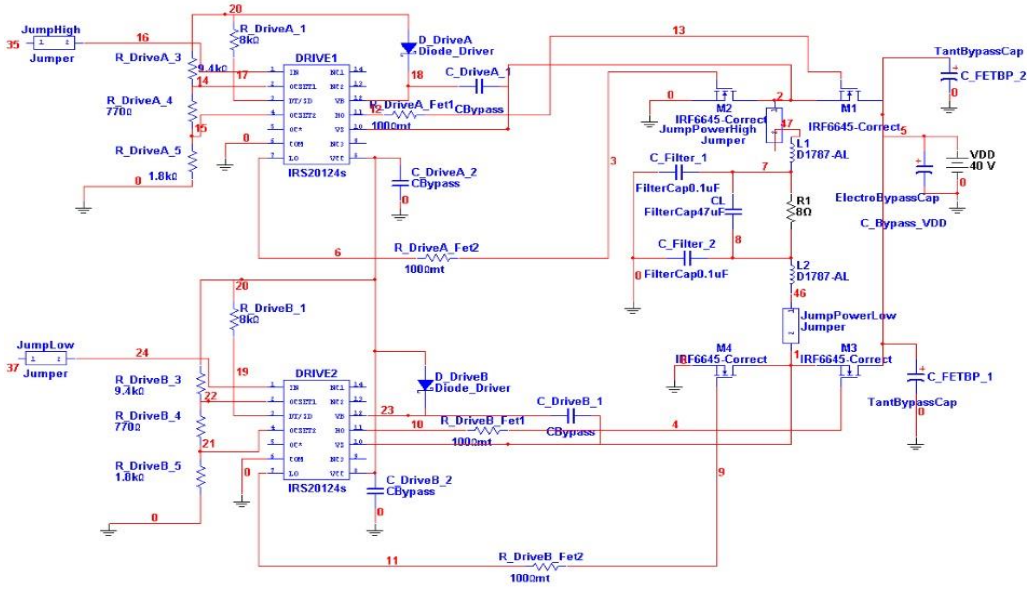

Figure 11. The Utilized Driver for the Mosfets in the Developed Class-D CMOS Power Amplifier

3.3. The Filter Stage

In this study, we utilized passive filter. The Butterworth filter is an important filter, which is chosen to be used in the developed class-D CMOS power amplifier. This filter formula and specification are determined based on its components and their configurations. The second order half circuit Butterworth filter is shown in Figure12.

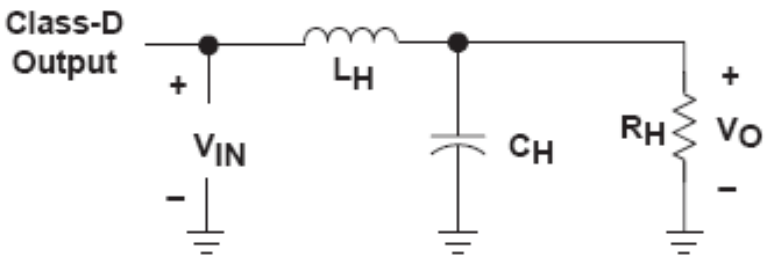

Figure 12. The Butterworth Filter Schematic

This filter formula is as follows:

$$R_H = \frac{R_L}{2} \tag{3}$$

$$C_H = \frac{1}{2\pi f_c \sqrt{2} R_H} \tag{4}$$

$$L_H = \frac{\sqrt{2} R_H}{2\pi f_c} \tag{5}$$

Using these equations, the ideal values for these components are computed. To gain the outmost efficiency, the filter configuration should be changed. Instead of using two capacitances, which are connected to the ground, one capacitor is placed between two half circuits. Moreover, to compensate the other capacitors, the two resistors are replaced with capacitors. These changes help to improve the efficiency. The final configuration for this filter is given in Figure13.

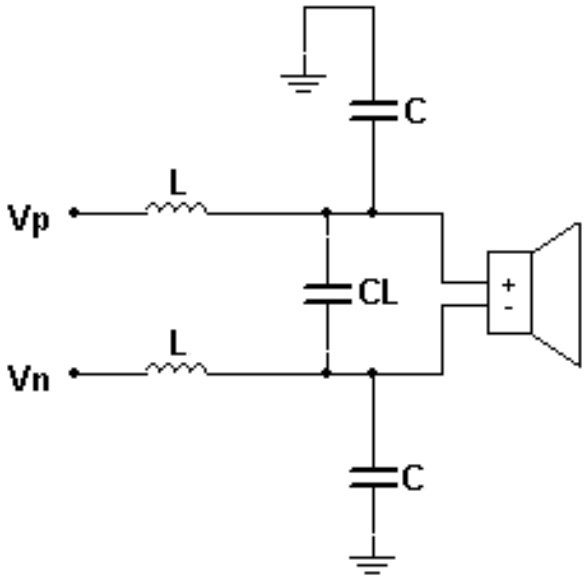

Figure 13. The Utilized Filter in the Developed Class-D CMOS Power Amplifier

This configuration is final, but the value of these components should be selected in relation to the system's output efficiency.

3.4. The Quality Parameters

This system quality parameters can be categorized in 4 groups: (a) efficiency, (b) frequency response, (c) THD, and (d) SNR [2, 6]. The first and most important parameter for this system is efficiency, which is computed as follows:

$$Efficiency = \frac{P_{out}}{P_{in}} \tag{6}$$

Where:

$$P_{in} = V_{in(DC)} . I_{in(DC)} \tag{7}$$

$$P_{out} = \frac{V_{ouut(RMS)}^2}{R_{load}} \tag{8}$$

Then

$$Efficiency = \frac{V_{in(DC)} I_{in(DC)}}{\frac{V_{ouut(RMS)}^2}{R_{load}}} \tag{9}$$

It should be noted that SNR is computed using (2).

The frequency response is formulated as follows:

$$Gain = \frac{V_{out(RMS)}}{V_{in(RMS)}} \tag{10}$$

The THD of this system is also computed as follows:

$$THD = \frac{\sqrt{h_1^2+h_2^2+h_3^2+h_4^2+h_5^2}}{original\ signal} . 100 \tag{11}$$

To find the perfect MOSFET, the system output is observed and tested by changing the modulator frequency from 1MHz to 30MHz. For each transistor, there is an ideal frequency, for example: IRF3808 ideal frequency is 2MHz. In this study, we utilized IRS20124S (Pbf) at 5MHz modulation frequency, which leads to a near perfect power efficiency (96%) and low THD. This transistor special characteristic is its low drain source resistance (r_{ds}).

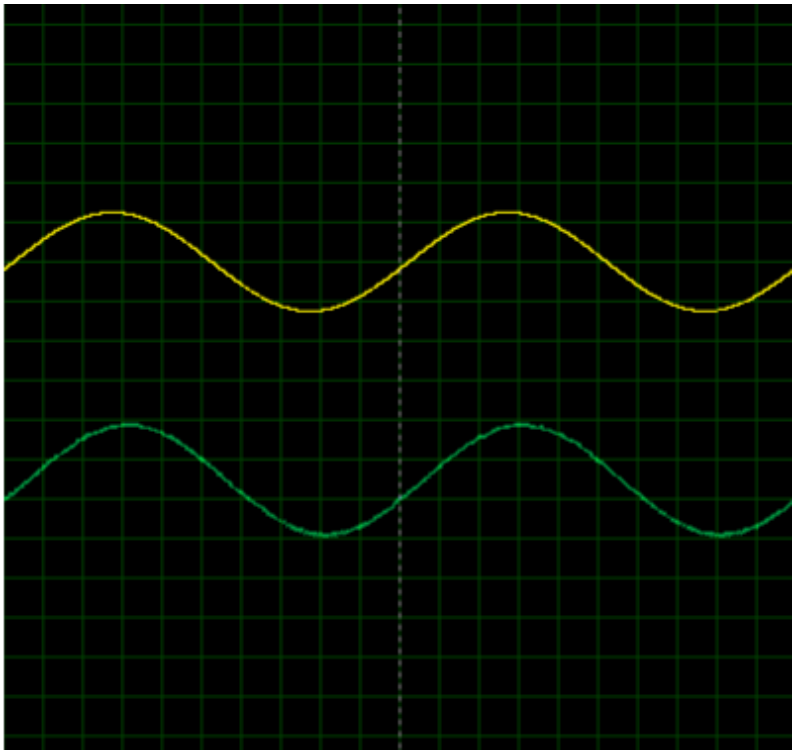

Figure 14. The Simulation Results of the Developed Class-D CMOS Power Amplifier

The selected values for filter components are C_L=0.47$_{\mu F}$ and C=0.1$_{\mu F}$ and L=20$_{\mu H}$. A very important parameter for choosing the inductor is that this component must have a low resistance. It is because all of the system output is passed through the inductors and then into the speakers. So, they must have the lowest possible resistance.

4. Comparison

The developed architecture for the class-D CMOS power amplifier is simulated using MATLAB 2016b. Table 1 summarizes the simulation results of the developed class-D CMOS power amplifier compared to other class-D audio amplifiers in [17-21].

Table 1. The Comparison Table for Class-D Audio Amplifiers

Parameters	This paper	[17]	[18]	[19]	[20]	[21]
Modulator architecture	Digital ΣΔ	PWM	PWM	PWM	DSP	Digital ΣΔ
VDD_P	50V	60V	20V	50V	18V	80V
$P_{Out\ max}$	80W	200W	20W	240W	13W	45W
Peak SNR (dB)	78	82.2	91	74.1	87	92.8
THD+N	0.001%	0.017%	0.01%	0.1%	0.07%	0.015%
Efficiency (%)	97	90	89	N/A	88	93
Bandwidth (kHz)	30	20	20	20	14	20

Based on these results, the developed class-D CMOS power amplifier has an improvement compared to class-D CMOS power amplifier in [17-21] in terms of THD, efficiency, and bandwidth. Although, the SNR comparison shows that this parameter is decreased by about 15% compared to [21], but the output power and bandwidth are increased by about 70% compared to [21]. Moreover, these results denote that the performance of this system is improved. So, the developed class-D CMOS power amplifier is more useful compared to other class-D audio amplifiers.

5. Conclusion

Amplifiers play an important role in today's technology. Its main concerns are efficiency, output quality and power. In this study, a novel design for the PDM class-D CMOS power amplifier is developed. Modulator architecture is composed of a second order delta sigma modulator using three state feedbacks. The power stage configuration and component are tested and chosen very carefully. The filtering stage is designed to improve the output quality with respect to the power stage output. The proposed architecture for the class-D CMOS power amplifier is simulated in MATLAB. Our simulation results show that the developed class-D CMOS power amplifier has several advantages compared to other class-D audio amplifiers in [17 - 21].

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