International Journal of Control and Automation
Vol. 10, No. 2 (2017), pp.137-146
http//dx.doi.org/10.14257/ijca.2017.10.2.12

Alternative Erase Verify : The Optimization for Longer Data Retention of NAND FLASH Memory

Juwan Seo[1], Namgi Kim[2] and Min Choi*[1]

[1] *Dept. of Information and Communication, Chungbuk National University, Chengju, 28644, South Korea*
E-mail : Juwan.seo@sk.com, mchoi@cbnu.ac.kr
[2] *Dept.of Computer Science, Kyonggi University*
E-mail : ngkim@kyonggi.ac.kr

Abstract

The NAND FLASH memory is a popular type of memory that is with a DRAM (Dynamic Random Ac-cess Memory). NAND Flash memory is a non-volatile memory that can retain data even without power. NAND FLASH memory is likely to increase the level of integration than the NOR-type cell. Because NAND FLASH memory is advantageous in miniaturization, it has been widely used in the eMMC (mobile devices) and SSD (Solid State Drive). This is because the NAND Flash Memory is advantageous for high bandwidth operations than NOR Flash..

Keywords*: NAND Flash, Erase Verify, Cell Retention*

1. Introduction

NAND FLASH memory is a popular type of memory that is with a DRAM (Dynamic Random Ac-cess Memory). NAND Flash memory is a non-volatile memory that can retain data even without power. NAND FLASH memory is likely to increase the level of integration than the NOR-type cell. Because NAND FLASH memory is advantageous in miniaturization, it has been widely used in the eMMC (mobile devices) and SSD (Solid State Drive)

As previously mentioned, NAND FLASH is clearly present in some drawbacks, while very advan-tageous in a non-volatile memory cell integrated in accordance with a scaling device. Essentially '1' and the operating mechanism itself, to make the state of "0" high bias (at least greater than ~ 10V) to the floating gate or well applied to inject charge and (program operation), Remove (erase operation) for FN taking place -tunneling-based, resulting in clear because of the accompanying gate oxide (tun-nel oxide) degradation of the cell necessarily, accompanied by a limited number of times of writing operation, and accompanied by a limited period of time to preserve the data. By default, the NAND flash in the program cell (0) and erase cell (1) for how to make the cell gate or well on the bias applied to floating gate of the charge potential adjustment by cell of threshold voltage (Vth: threshold voltage) to the desired level the operation to change to.

Thereafter, the state of the cell produced the desired level there is the specific (read operation) that can read the data applying a bias read bias operation, if the position as level a Vth of the cell you want in this process, but the problem, desired location If it is to me contrast variations are reading the wrong data. Thus, the write operation (program) and erase (erase) long but have a certain degree of error or dispersion in operation, it can be called a very important process in the Vth as target to create and maintain the most

[1] *Corresponding Author : Prof. Min Choi (mchoi@cbnu.ac.kr)
This research was supported by Basic Science Research Program through National Research Foundation of Korea(NRF) funded by Ministry of Science, ICT & Future Planning(NRF-2016R1C1B1012189)

ISSN: 2005-4297 IJCA

uniform Vth. In reality, however, each cell Vth states do not remain and it is changed by a various number of factors.

In this paper, the slow cell deterioration rate by reducing the amount of stress in self-erase cell per-spective, discusses the erase operation method that reduces the disturbance caused by the Vth changes ultimately.

2. Related Works

Recently many researches for improving the life NAND FLASH have been actively studied. There are two types of Flash memories : NAND type vs. NOR type. NAND flash has reduced erase and write times, and requires less chip area per cell, thus allowing greater storage density and lower cost per bit than NOR flash; it also has up to 10 times the endurance of NOR flash. However, the I/O interface of NAND flash does not provide a random-access external address bus. Rather, data must be read on a block-wise basis, with typical block sizes of hundreds to thousands of bits. This makes NAND flash unsuitable as a drop-in replacement for program ROM, since most microprocessors and microcontrollers require byte-level random access. In this regard, NAND flash is similar to other secondary data storage devices, such as hard disks and optical media, and is thus, highly suitable for use in mass-storage devices, such as memory cards.

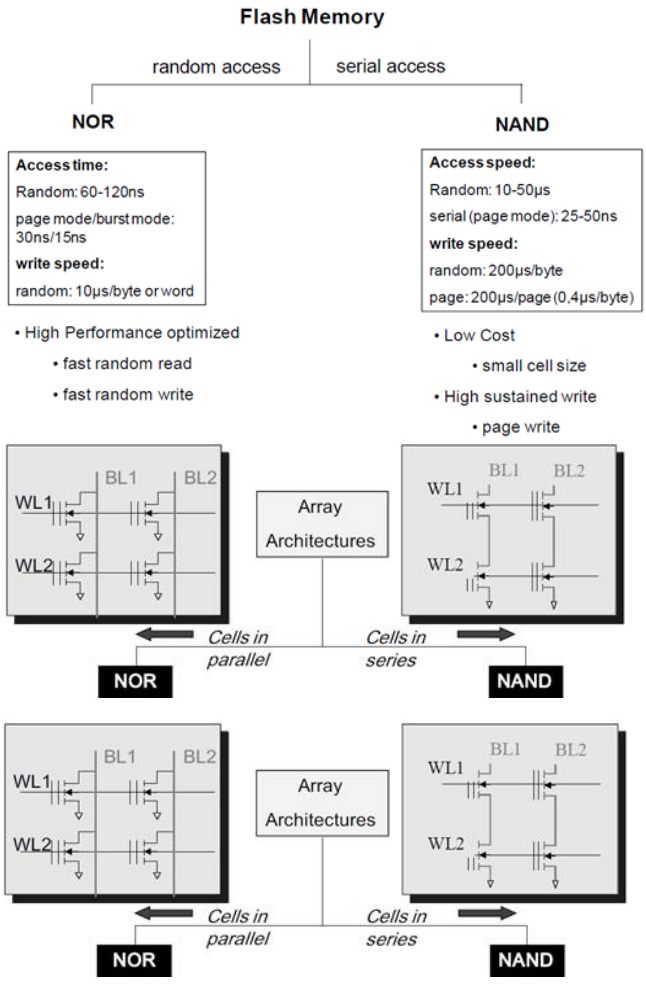

Figure 1. Flash Memory Classification and Unit Cell Structure

In NOR flash, each cell has one end connected directly to ground, and the other end connected directly to a bit line. This arrangement is called "NOR flash" because it acts like a NOR gate: when one of the word lines (connected to the cell's CG) is brought high, the corresponding storage transistor acts to pull the output bit line low. NOR flash continues to be the technology of choice for embedded applications requiring a discrete non-volatile memory device. The low read latencies characteristic of NOR devices allow for both direct code execution and data storage in a single memory product.

Previously, this section introduces the basic principles and methods of the NAND cell and erase, a descrip-tion will be given of the features and problems in each conventional method.

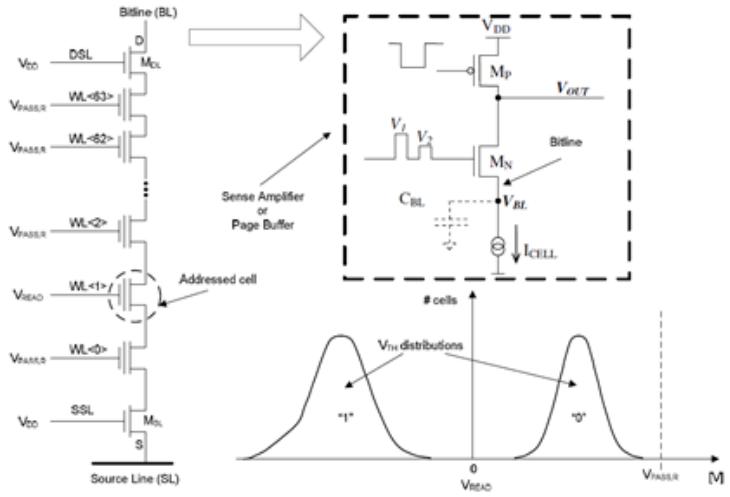

Figure 2. Determining Logic '0' or logic '1' on NAND Flash Memory (cell Vth)

Each cell, as shown in the figure, is tailored to Vth with the value creating a Vth. The cell have a positive value to the program operation to make a state "0", to the erase operation to make a state of '1' nega-tive . Since, through the read operation, the cell is to determine if a '1' or '0'.

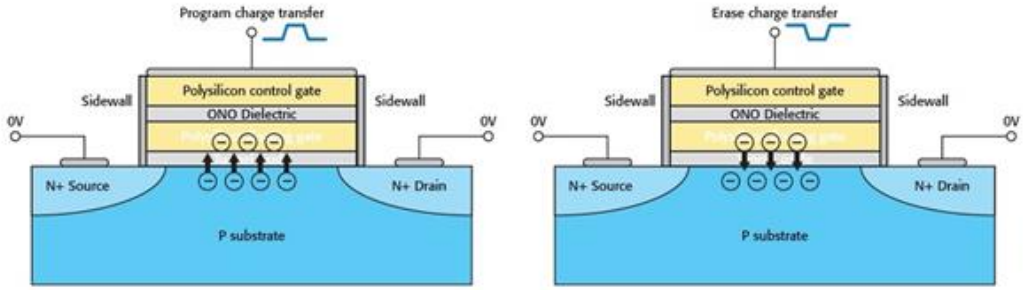

Figure 3. Bias Condition of Program and Erase Operation on Unit Cell

This is a process that left the bulk electron injection from the program to operate as floating gate, and the right actions that the charge is injected into the floating gate to the erase operation in bulk. The charge moves by both FN-tunneling operation. The verify operation for determination after forming the cell vth of the erase state requires the desired non-random voltage level applied. This level is known as "program verify level" or "erase verify level". The erase bias is applied

until you reach to the point of verify level. If there are cells over the verify level, they are inhibitly operated(e.g., applying Vcc voltage to bitline on PGM cell, resulting in FN tunnelling disabled), so that it should no longer occurred in Vth variation.

3. Proposed Approach : Alternative Erase Verify

As previously mentioned, NAND FLASH is clearly present in some drawbacks, while very advantageous in a non-volatile memory cell integrated in accordance with a scaling device. Essentially the operating mechanism itself to make the state of '1' and "0" requires high bias (at least greater than ~ 10V) to the floating gate being applied to inject charge and (program operation). This operation results in the accompanying gate oxide (tunnel oxide) degradation of the cell by FN-tunneling. Therefore, there is a limitation to the number of times of writing operation, and accompanied by a limited period of time to preserve the data.

If almost NAND flash cell of the initial state are not the operations, we can set the vth bring no problem of the cell to the desired level. We can read the changed Vth. We have no difficulty in determining the "1", "0" from the data. If there are several writing operations or repeated erase operations, there are problems that some change occurred in Vth generated. This is because the Vth was biased for the initial cell setting. In general NAND flash is characterized in that upon reaching the operating program the cell vth level more quickly. At the same time, NAND flash is characterized in that the deterioration Vth variation. Further, in the NAND flash memory cell during erase operation it is more latetly reached Vth level. If after the erase cycle during program operation, we should provide low program bias. When erase operation, we shall be applied for higher erase bias. So that we are able to locate a verify level Vth dispersion has a stable NAND flash memory. With high bias during program / erase, ISPE ISPP operation has advantage in that it can make the desired cell Vth level in the fastest time. The higher the erase operation bias operation is a deep deterioration of the film quality NAND Flash. Eventually, it becomes impossible to ensure a desired service life light. A term of life but ensure as much as possible, and the program / erase speed is held fast, it shall minimize deterioration Cell Vth distribution.

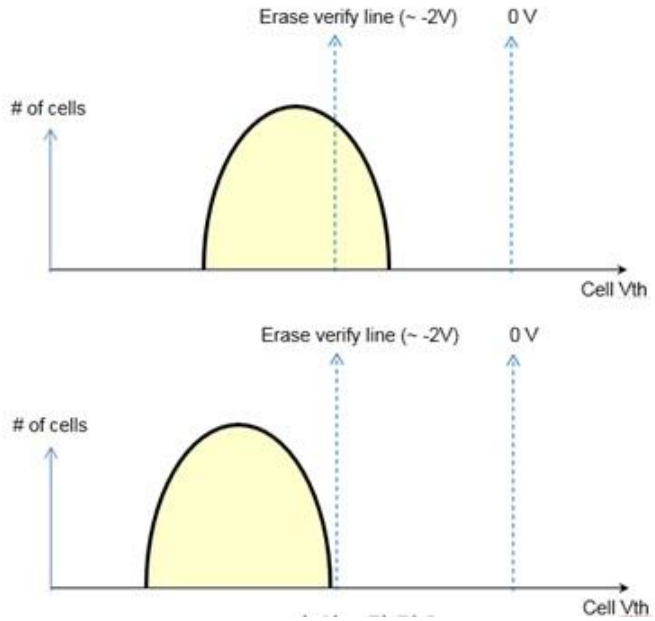

Figure 4. Erase Verify Concept

After applying the erase operation during erase pulse, we have to make sure the NAND Flash cell reach the desired level below the erase Vth, resulting in the erase verify operation. Basically, verify operation is an operation similar to the operation 'read'. After the program / erase operation ends, the read operation the value of the cell is the purpose of the determination of '1' and '0'. The verify operation performed in the erase / program process must ensure that you have reached the desired level of Vth. Erase operation is an operation of a process for applying an erase pulse. Therefore verify operation or condition gives a direct impact on determining the next erase bias.

In conventional erase verify, the verify operation is sure to reach every cell in good negative level. To this end, applying the same bias for all WL to verify that cell will erase. Thus, Since the bias is applied to the cell string of the entire WL, less current flowing in each cell string, if there is some Vth variation. It results in failure of erase verify operation. Usually, we apply a bias of 0V ~ 1V all about WL. There is no problem when all cells were well erased. But, if a cell has variation that erase speed is slow, then erase verify resulted in fil because of the cell. Then, another erase operation should be operated again with higher bias voltage.

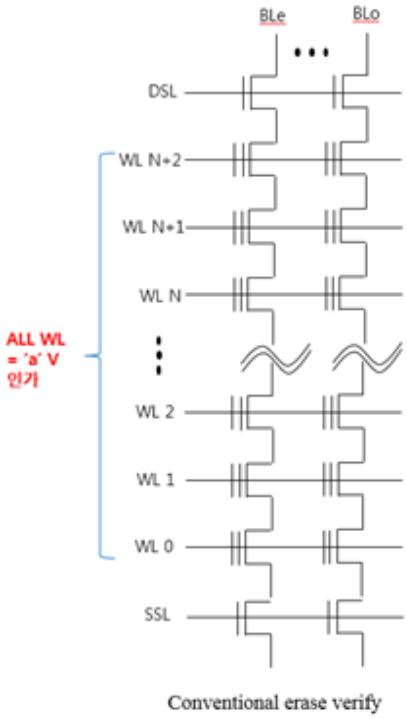

Figure 5. Conventional Erase Verify Approach

In this paper, we applied a little modification into conventional approach in that a bias to verify alternately applied to the word-line one. As a result, we have a method of performing erase verify twice. If you use this approach, we apply bias 1/2 of the total WL rather than applying same bias once at a time to total WL, so that we can obtain more stable cell current.

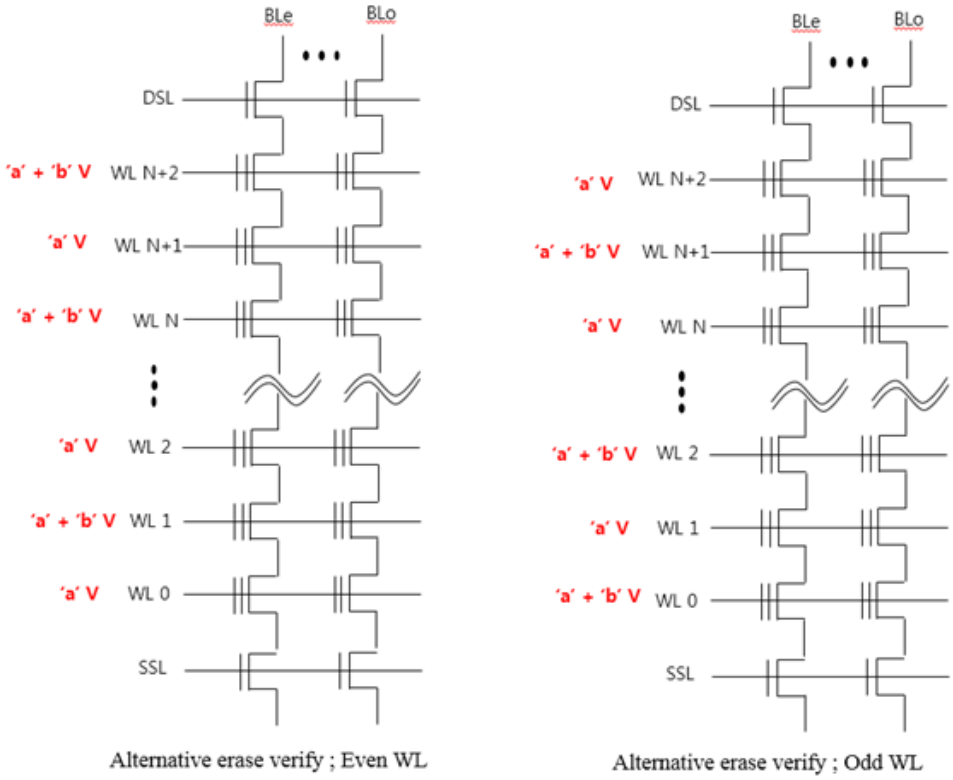

Figure 6. Alternative Erase Verify Approach

Ultimately, even if the operation is similar to verify, alternative erase verify in the case of a conventional erase verify if the cell current than the back pattern dependency, or it can be minimized to reduce the erase bias may be to suppress the rise. Instead, verify the number is doubled in terms of total erase time to increase the downside, but the actual erase pulse is applied to the preparation time (to a few ms), because very little time (to a few us) is judged as negligible.

Erase verify the more likely it will end, because it is not necessary to talk further erase bias, that is to stop talking about the increasing erase bias.

Conventional erase verify case :

17V erase – E.V(Fail) – 18V erase – E.V(Fail) – 19V erase – E.V(Pass)

Alternative erase verify case :

17V erase – E.V(Fail) – 18V erase – E.V(Pass)

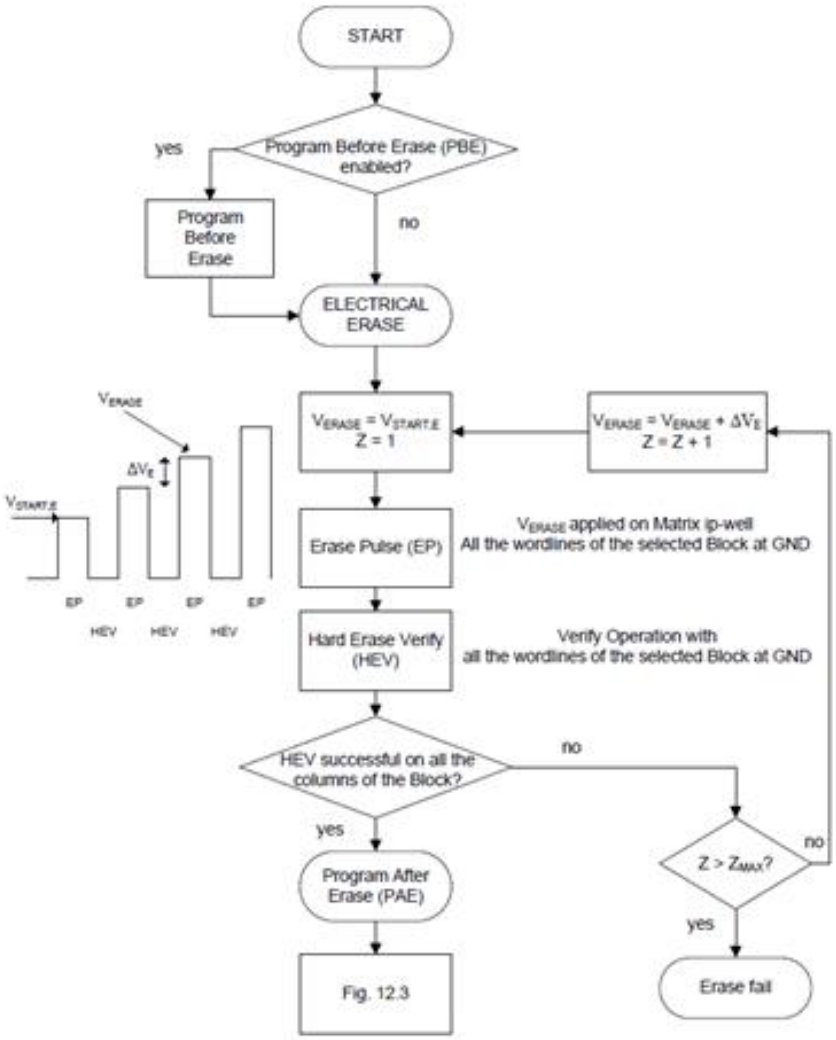

Figure 7. ISPE Concept and Alternative Erase Verify Flow Chart

A memory block may be programmed one page at a time using an Incremental Step Pulse Program (ISSP) and erased using a similar Incremental Step Pulse Erase (ISPE). The ISPP and/or ISPE may be performed by flash controller 107 in response to one or more instructions (for example, commands) received from controller 101. For example, using an ISPP, a page operation may be performed by applying a voltage at the gates of each cell in the memory page. A corresponding selection at the bit lines creates a voltage potential in the selected group of memory cells to create one or more distributions that are different than the erased L0 distribution state

In the depicted Figure 7, memory cells in a 2-bit/cell (MLC) NAND flash memory are returned to an erased state (L0). In this regard, flash memory 103 may be instructed by controller 101 to perform an Incremental Step Pulse Erase (ISPE) procedure to apply a series of voltage pulses to the memory cells which are being erased. The amplitude polarity may be reversed (from ISPP) during the erase operation to remove electrons from the floating gates of the memory cells. The voltage evolution of such an erase operation is depicted in FIG. 2 by the arrows 201 representing cells of the L1 distribution, L2 distribution, and L3 distribution being returned to the L0 distribution state, with the voltage level of each cell falling below a threshold voltage 202 corresponding to an erased state (for example, zero volts). In some aspects, the status of the cells may be verified by applying an erase verify (EV) voltage 203 (for example, at a second threshold voltage) to

confirm that the cells have indeed been erased. As described herein, the subject technology implements a pulse voltage high enough to return all cells in any given distribution to the erased (L0) distribution state in a single pulse.

According to various implementations, the erase parameters may be defined separately for each pulse or series of pulses. The erase parameters may be set within a given flash memory device 103 by the manufacturer of the flash memory device. In some implementations, one or more of the erase parameters may be set via registers of flash memory device 103, for example, by controller 101. Given a manufacturer's specification for a particular type of flash memory it will be recognizable how to select the appropriate parameters as input to an ISPE to achieve an erased distribution

Thus, erase verify when sufficient cell current flowing to verify pass is given the chance to be so high, erase some extent though well though, verify cell when erase bias due to such variation between the rise will be prevented.

4. Experimental Results

We have tested and evaluated the proposed approach using the Teradyne's Magnum memory tester. The process is based on NAND FLASH SLC memory 4Xnm.

In order to show the erase deterioration rate by the bias increases we make use of cycling Vth shift which is used as an index to determine the degree to which the cell is deteriorated. The greater the degree of deterioration accelerates cycling around the cell speed. The higher the number, the greater the degree of cell deterioration.

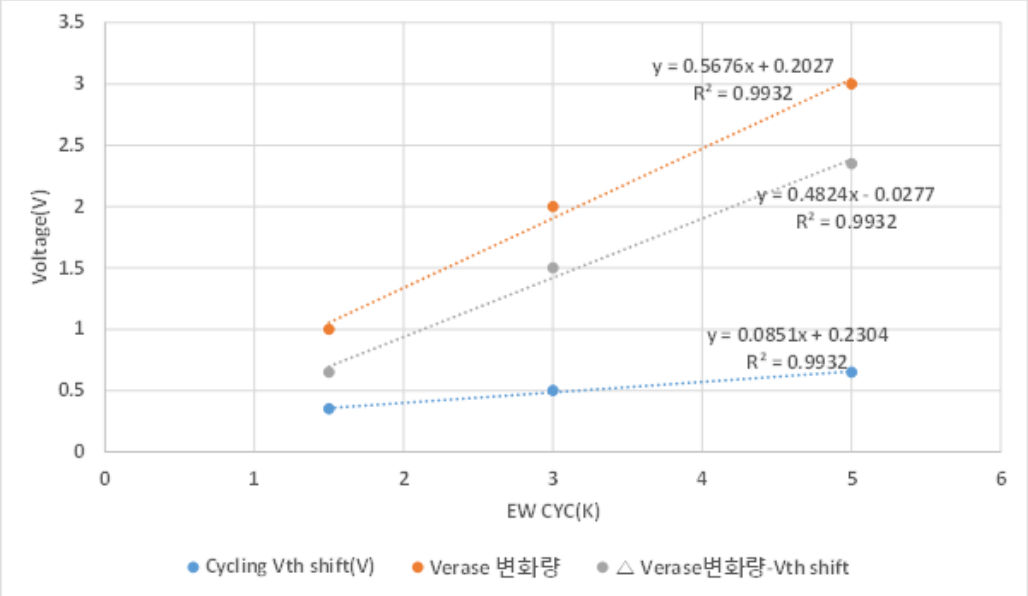

Figure 8. Voltages Depending on EW Cycle

Figure 9 shows the change in the erase verify pass erase bias point according to EW cycle on alternative erase verify. In contrast to conventional approach, 5K (5000 times) even though cycling is in progress bias increment is only 0.5V ~ 1V.

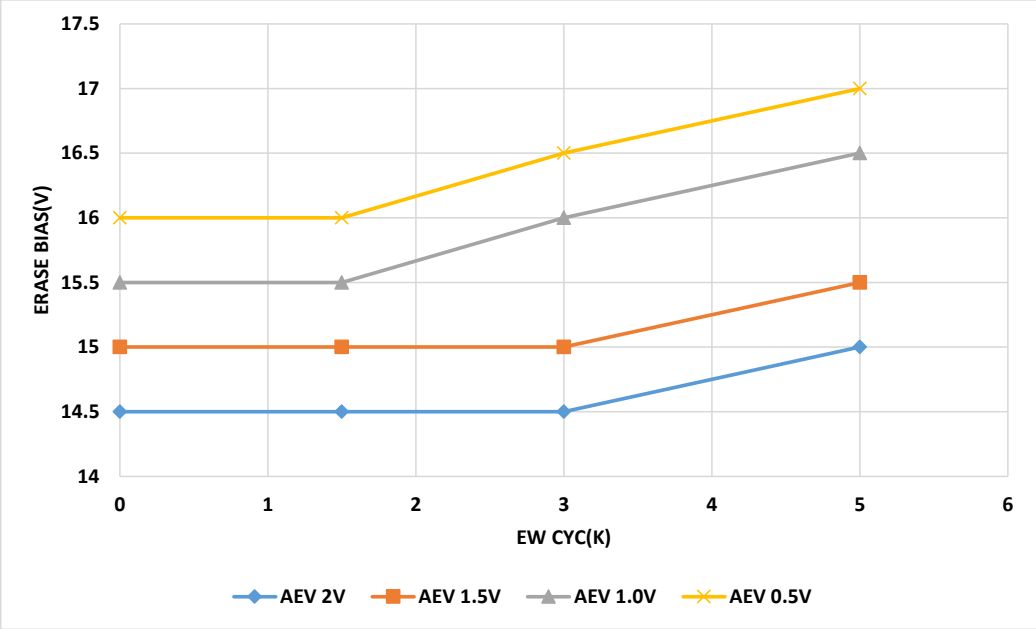

Figure 9. Erase Bias Increment using Proposed Approach

In figure 10, Vth shift amount are compared between conventional and alternative approach. The number of cycling progresses the more Vth shift difference is gradually increasing. Conventional methods that erase bias is increasing faster than alternative methods. Therefore, the longer cycle progresses the greater the degree of degradation of the cell

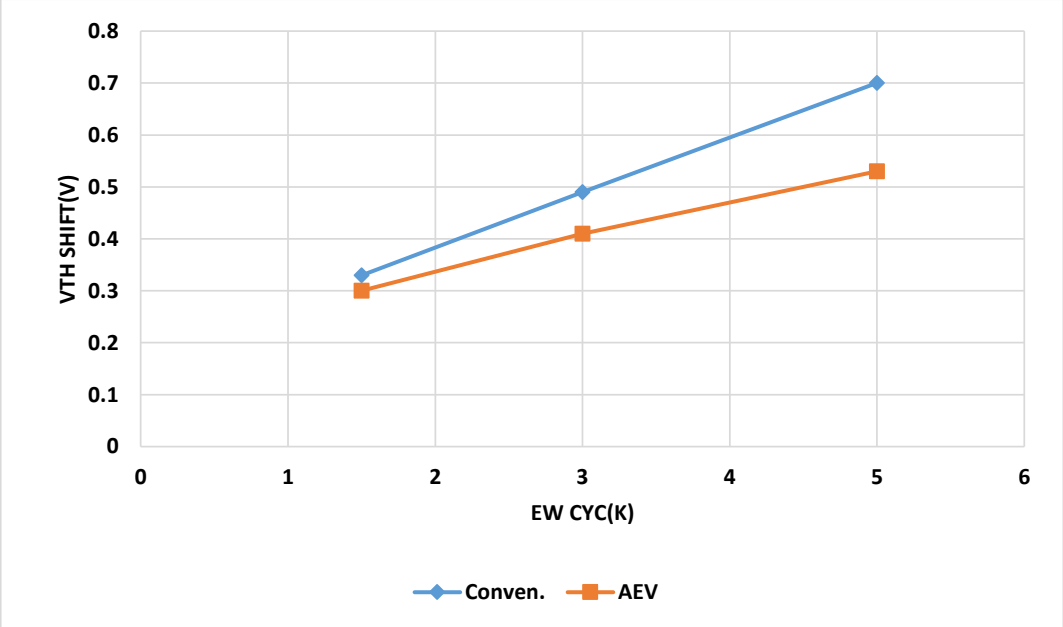

Figure 10. Cell Deterioration Rate between Conventional and Proposed Approach

4. Conclusion

There are currently a variety of ways and seek to improve the life of NAND FLASH, this paper is how the kkoehan Heavy Nine improve life conditions by changing the erase operation.

As such, but also the intrinsic improvement research, including improved process or film quality characteristics should be conducted in future when read, including the operation algorithm improved method, error occurs even if the software typically is more Incidence powerful algorithm developed to modify or process it that is determined.

References

[1] N. Mielke et al. Bit error rate in NAND flash memories. In Proc. Of IEEE International Reliability Physics Symposium, IRPS'08, pages 9–19,2008
[2] Y. Pan et al. Exploiting memory device wear-out dynamics to improve NAND flash memory sys-tem performance. In Proc. of the 9th USENIX conference on File and stroage technologies, FAST'11, pages 18–18, 2011.
[3] J. Choi et al., "3D Approaches for Non-volatile Memory," in Proc. IEEE Symp. VLSI Technology, 2011.
[4] A. A. Chien et al., "Moore's Law: The First Ending and A New Beginning," Tech. Report, Dept. of Computer Science, the Univ. of Chicago, TR-2012-06.
[5] J.-W. Hsieh et al., "Efficient Identification of Hot Data for Flash Memory Storage Systems," ACM Trans. Storage, vol. 2, no. 1, pp. 22-40, 2006.

Authors

Juwan Seo
Senior Researcher, SK Hynix Semiconductor from 2004.
M.S., Dept. of Information and Communication Engineering, Chungbuk National University, 2016
B.S., Dept of Electornic Material Engineering, Kwangwoon University, 2004

Min Choi
Associate Professor, Chungbuk National University from 2011
Senior Researcher, Samsung Electronics from 2008 to 2010
Ph.D., Dept. of Computer Science, KAIST, 2009

