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Scaling of Supply Voltage in Design of Energy Saver FIR Filter on 28nm FPGA

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Abstract

In this work, we are going to analyze the effect of main supply voltage, auxiliary supply voltage, local voltage of different power bank, and supply voltage in GTX transceiver and BRAM on power dissipation of our FIR design using Verilog during implementation on 28nm FPGA. We have also taken three different level of voltage with 16 IO standards and we get three different power analysis for each IO Standards. IO power dissipation of FIR filter is 150mW with SSTL_18_II IO standard. When we migrate our design with HSTL_I, HSUL_12, LVCMOS15, LVTTL, MOBILE_DDR, and PCI33_3 IO standards then there is 53.33%, 86%, 90.67%, 65.33%, 52%, and 48.67% reduction in IO power dissipation of FIR Filter design on CSG324 package of Artix-7 FPGA family.

Keywords*: Supply Voltage, Input Voltage, Output Voltage, Auxiliary Voltage, Power Dissipation, Energy Efficient, FIR Filter*

1. Introduction

VCCINT supply power with internally connected metallization in chip. Internal connection have to ensure good decoupling capacitors, minimum IR drop, and lesser noise on the power rails. VCCAUX bumps on the die connect with common metal interconnect. This interconnect has a common connection on the laminate package. VCCO pins tied together for pins in the same bank [1]. VCCO33, VCCO25, VCCO18, VCCO15, VCCO135 and VCCO12 are 6 difference VCCO pins for six following voltage of bank 3.3V, 2.5V, 1.8V, 1.5V, 1.35V and 1.2V respectively. We have also taken three different level of voltage for three different power analysis with 16 IO Standards of 7 different family. For example, minimum voltage is 0.95V, average voltage is 1.0V and maximum voltage is 1.05V for VCCINT as shown in Table 1. SSTL IO standards family is the most power hungry IO standards. LVCMOS is the most energy efficient IO standards for our FIR filter design on FPGA. Power dissipation of other 5 IO standards family like, HSTL, HSUL, LVTLL, MOBILE_DDR and PCI33_3 give intermediate results in terms of power.

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Table 1. Scaling of Voltage in FIR Filter on 28nm FPGA

Voltage	Minimum	Average	Maximum
Vccint	0.950	1.000	1.050
Vccaux	1.710	1.800	1.890
Vcco33	3.000	3.300	3.450
Vcco25	2.380	2.500	2.630
Vcc018	1.710	1.800	1.900
Vcco15	1.430	1.500	1.580
Vcco135	1.300	1.350	1.400
Vcco12	1.140	1.200	1.260
Vccaux_io	1.710	1.800	1.890
Vccbram	0.950	1.000	1.050
MGTAVcc	0.950	1.000	1.050
MGTAVtt	1.140	1.200	1.260
Vccadc	1.710	1.800	1.890

In 7 series FPGA, average VCCINT, VCCAUX, VCCBRAM, and VCCADC voltage for power analysis are 1.0V, 1.8V, 1.0V and 1.8 V respectively as shown in Table 1. The recommended GTX transceiver power up sequence is VCCINT, MGTAVCC, MGTAVTT. Whereas, the recommended GTX transceiver power down sequence is MGTAVTT, MGTAVCC, VCCINT. The current and voltage associated with MGTAVTT, MGTAVCC are shown in Figure 1.

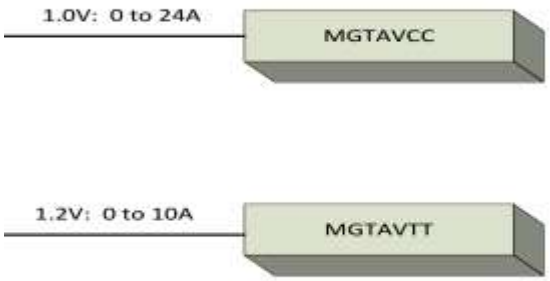

Figure 1. Xilinx MGT Reference Design [2]

VCCINT, VCCAUX, and VCCBRAM capacitors are listed as the quantity per device, while VCCO capacitors are listed as the quantity per I/O bank [3]. There are 41,600 FF, 90 DSP and 210 IO available on CSG324 package of Artix-7 FPGA family. Our current design of FIR filter, is using flip-lop (FF), digital signal processing (DSP) blocks and input/output (IO) port available on Artix-7 FPGA as shown in Table 2.

Table 2. Resource Availability and Usage by FIR Filter Design

Resource	Utilization	Available
FF	48	41600
DSP	9	90
IO	28	210

Our design is using only 1% (48 out of 41600), 10% (9 out of 90) and 13% (28 out of 210) FF, DSP and IO as shown in Figure 2 and Table 2.

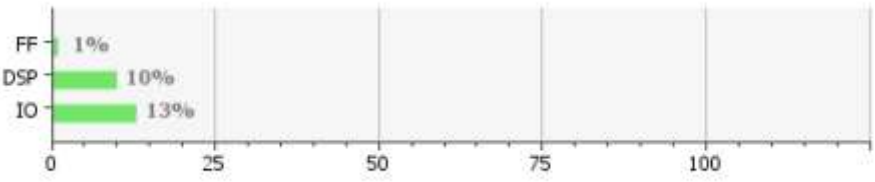

Figure 2. Resource Availability and Usage in Artix-7 FPGA

2. Related Work

Scaling of supply voltage on 28nm 7 series FPGA means variation of voltage between 0.95 V to 1.5 V. Voltage scaling in this paper is variation of voltage between 0.95V to 3.45V. In [4], energy efficient counter is developed with use of technique called voltage scaling. In [5], energy efficient mobile battery charge controller sensor is developed with voltage scaling. Voltage scaling is also used in FPGA based design of cyclic redundancy check [6], flip-flop [7] and Wi-Fi Ah Channel enable ALU [8]. [9] Investigates the possibility of reductions possible in commercially available FPGAs configured to support voltage, frequency and logic scalability combined with power gating. Voltage and frequency scaling is based on in-situ detectors that allow the device to detect valid working voltage and frequency pairs at run-time while logic scalability is achieved with partial dynamic reconfiguration [9].

3. Artix-7 FPGA

Dynamic power is related to switching activity and clock frequency of design. For power analysis of our design, we have to create timing constraints and add that clock to our design. In this work, our waveform has 10ns period, 0ns rising edge time and 5ns falling edge time as shown in Figure 3.

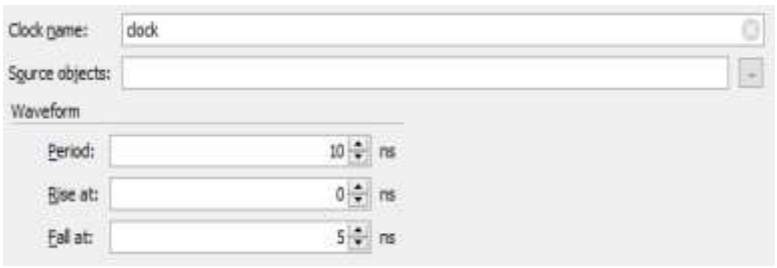

Figure 3. Clock Information of our FIR Filter Design

Table 3. Power Dissipation with Different IO Standards

IO STANDARDS	POWER DISSIPATION (Watt)
LVCMOS15	0.014
LVCMOS18	0.017
SSTL135_R	0.021
SSTL15_R	0.023
LVCMOS25	0.033
SSTL135	0.041
SSTL15	0.048
LVCMOS33	0.052
LVTTL	0.052
HSTL_I	0.07

MOBILE_DDR	0.072
PCI33_3	0.077
SSTL_18_I	0.09
HSUL_12	0.107
HSTL_II	0.118
SSTL_18_II	0.15

When we are using LVCMOS15, IO Power dissipation of FIR filter is the lowest *i.e.*, 14 mW. Whereas, IO power dissipation of FIR filter is the highest *i.e.*, 150mW with SSTL_18_II IO standards as shown in Table 3. Other family of IO standards like LVTTL, HSTL_I, MOBILE_DDR, PCI33_3 and HSUL is taking 52 mW, 70mW, 72mW, 77mW and 107mW respectively as shown in Table 3 and Figure 4.

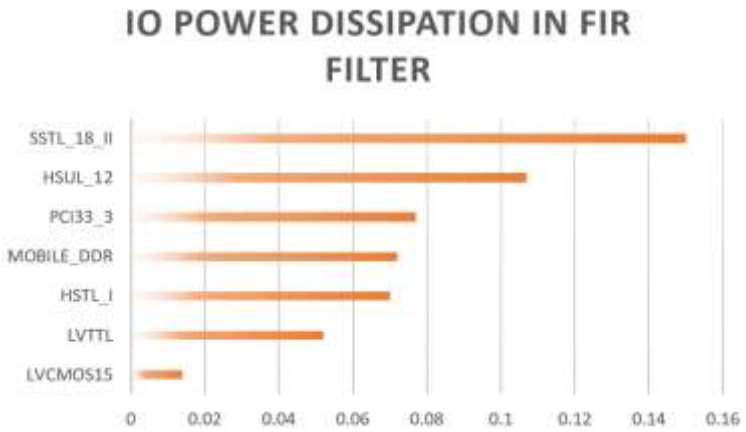

Figure 4. IO Power Dissipation on Artix-7 FPGA with 7 IO Standards

A. Power Analysing Using LVCMOS18 For 3 Different Voltage Level: Minimum, Average, Maximum

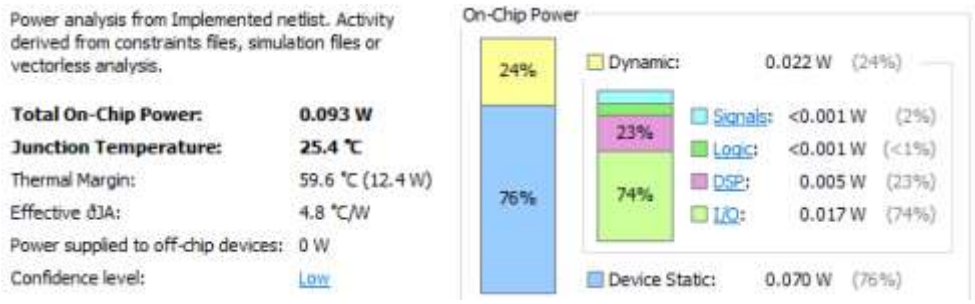

Figure 5. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, total on-chip power is 93mW as shown in Figure 5. It increases to 98mW for average voltage level as shown in Figure 5. It is 110mW for maximum voltage level as shown in Figure 7.

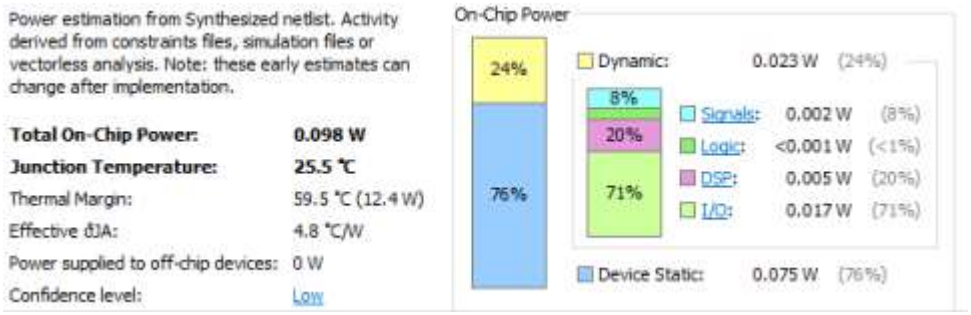

Figure 6. Power Analysis of FIR Filter for Average Voltage Level

Dynamic power is 22mW, 23mW and 25mW for minimum, average and maximum voltage level as shown in Figure5-7

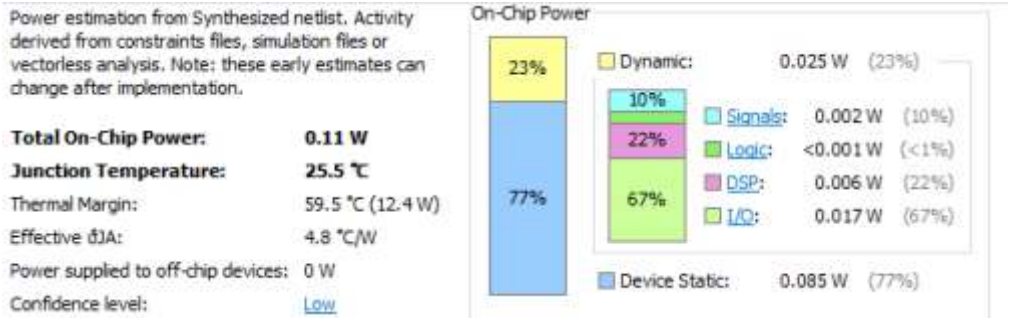

Figure 7. Power Analysis of FIR Filter for Maximum Voltage Level

B. Power Analysing Using HSTL_I For 3 Different Voltage Level: Minimum, Average, Maximum

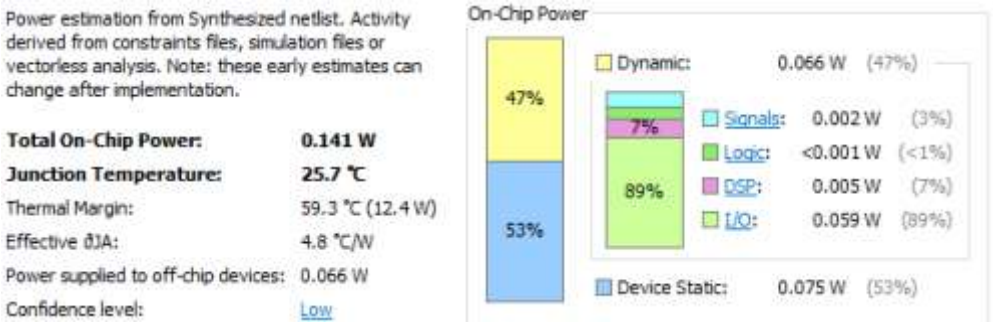

Figure 8. Power Analysis of FIR Filter for Minimum Voltage Level

Dynamic power is 66mW, power supplied to off-chip device is 66mW as shown in Figure 8.

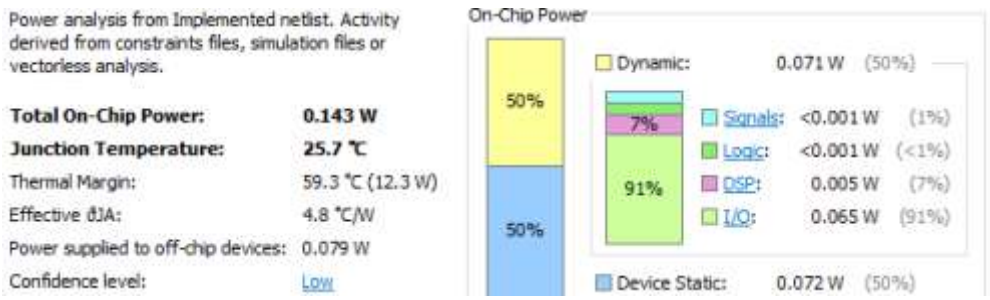

Figure 9. Power Analysis of FIR Filter for Average Voltage Level

Dynamic power is 71mW. Total on-chip power is 143mW and power supplied to off-chip device is 79mW as shown in Figure 9.

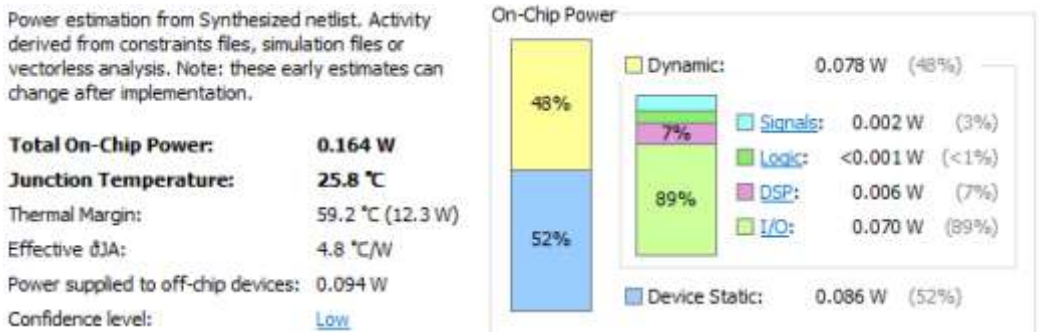

Figure 10. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 71mW. Junction Temperature is 25.8ºC. Total on-chip power is 164mW and power supplied to off-chip device is 79mW as shown in Figure 10.

C. Power Analysing Using HSUL_12 For 3 Different Voltage Level: Minimum, Average, Maximum

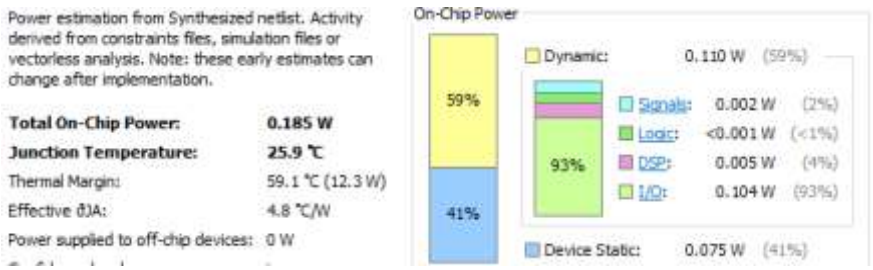

Figure 11. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 110mW. Junction Temperature is 25.9ºC. Total on-chip power is 185mW as shown in Figure 11.

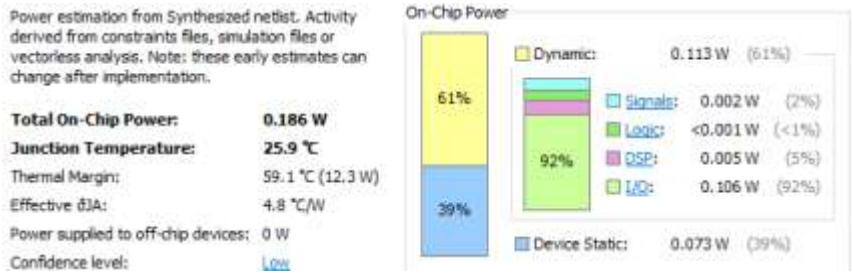

Figure 12. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 113mW. Junction Temperature is 25.9ºC. Total on-chip power is 186mW as shown in Figure 12.

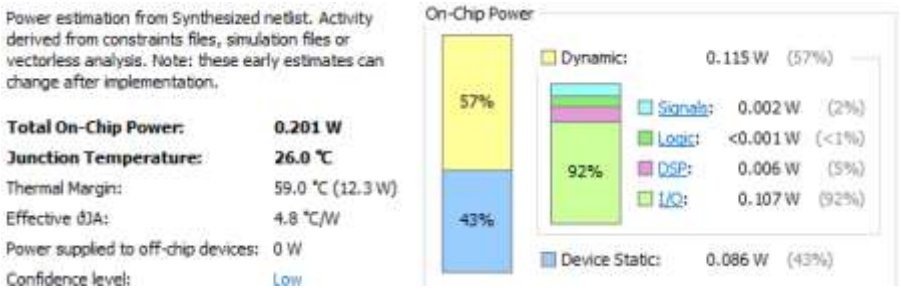

Figure 13. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 115mW. Junction Temperature is 26.0ºC. Total on-chip power is 201mW as shown in Figure 13.

D. Power Analysing Using LVCMOS15 For 3 Different Voltage Level: Minimum, Average, Maximum

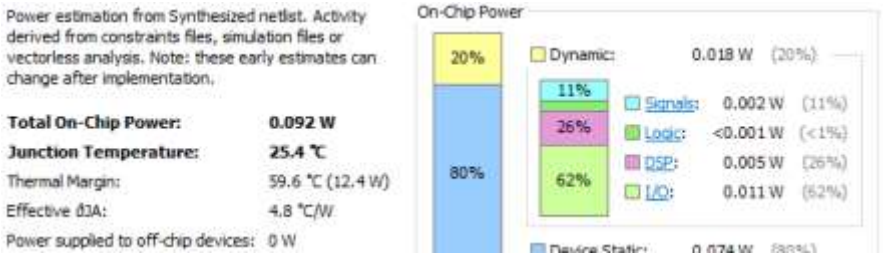

Figure 14. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 18mW. Junction Temperature is 25.4ºC. Total on-chip power is 92mW as shown in Figure 14.

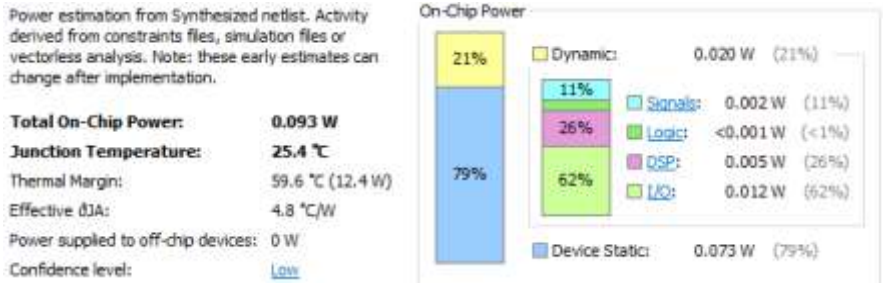

Figure 15. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 20mW. Junction Temperature is 25.4ºC. Total on-chip power is 93mW as shown in Figure 15.

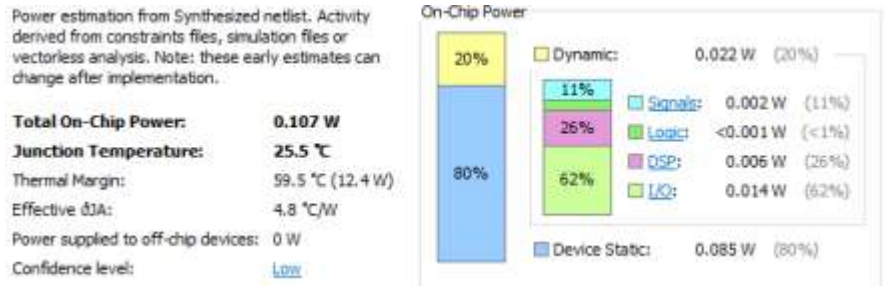

Figure 16. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 22mW. Junction Temperature is 25.5ºC. Total on-chip power is 107mW as shown in Figure 16.

E. Power Analysing Using LVTTL For 3 Different Voltage Level: Minimum, Average, Maximum

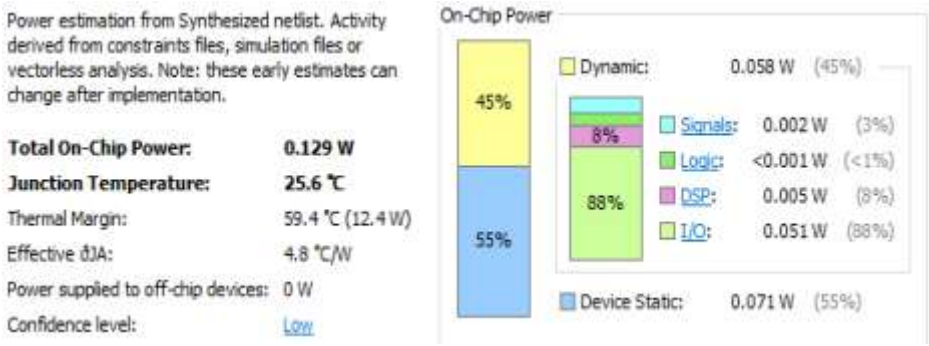

Figure 17. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 58mW. Junction Temperature is 25.6ºC. Total on-chip power is 129mW as shown in Figure 16.

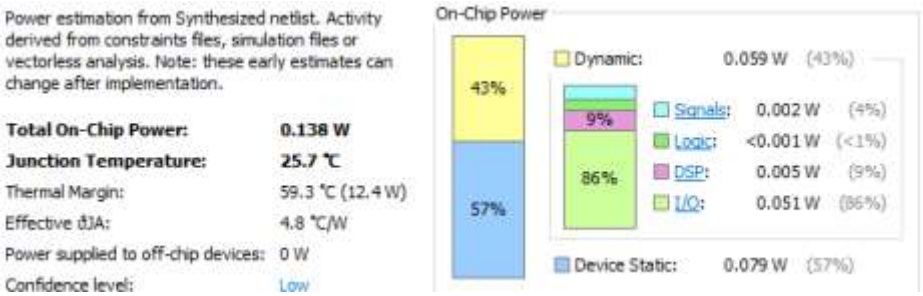

Figure 18. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 59mW. Junction Temperature is 25.7ºC. Total on-chip power is 138mW as shown in Figure 18.

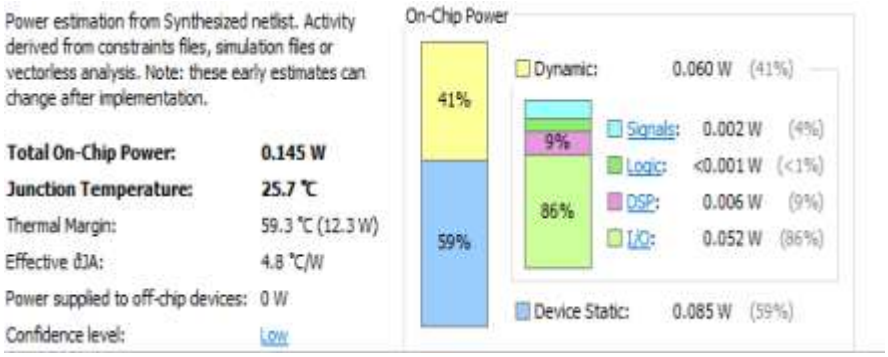

Figure 19. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 60mW. Junction Temperature is 25.7°C. Total on-chip power is 145mW as shown in Figure 19.

F. Power Analysing Using MOBILE_DDR For 3 Different Voltage Level: Minimum, Average, Maximum

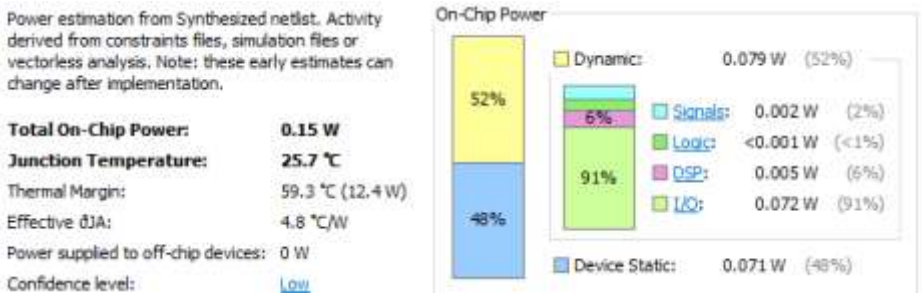

Figure 20. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 79mW. Junction Temperature is 25.7°C. Total on-chip power is 150mW as shown in Figure 20.

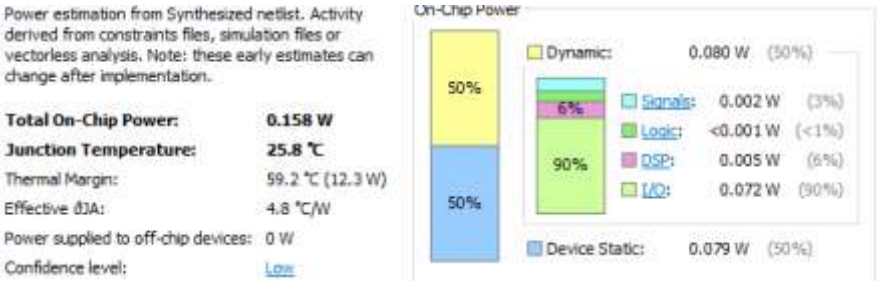

Figure 21. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 80mW. Junction Temperature is 25.8°C. Total on-chip power is 158mW as shown in Figure 21.

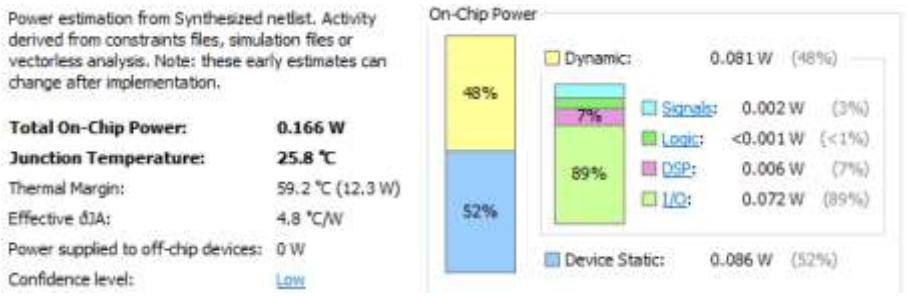

Figure 22. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 81mW. Junction Temperature is 25.8ºC. Total on-chip power is 166mW as shown in Figure 22.

G. Power Analysing Using PCI33_3 For 3 Different Voltage Level: Minimum, Average, Maximum

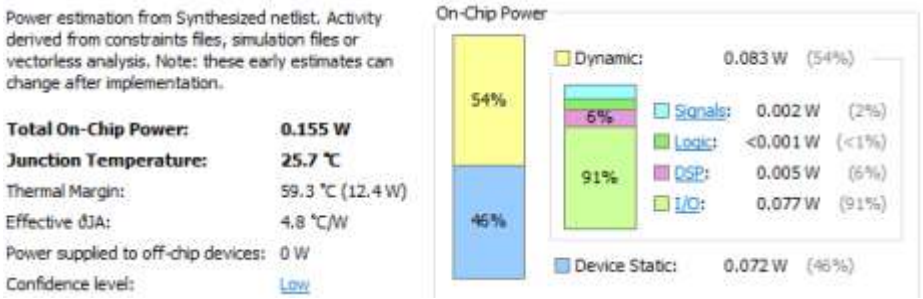

Figure 23. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 83mW. Junction Temperature is 25.7ºC. Total on-chip power is 155mW as shown in Figure 23.

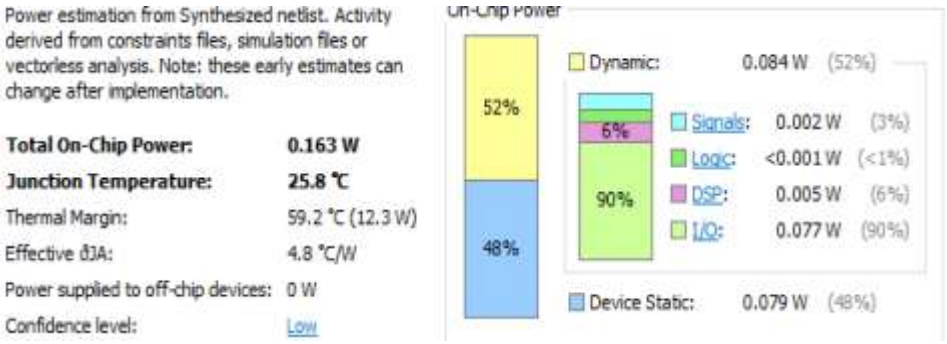

Figure 24. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 84mW. Junction Temperature is 25.8ºC. Total on-chip power is 163mW as shown in Figure 24.

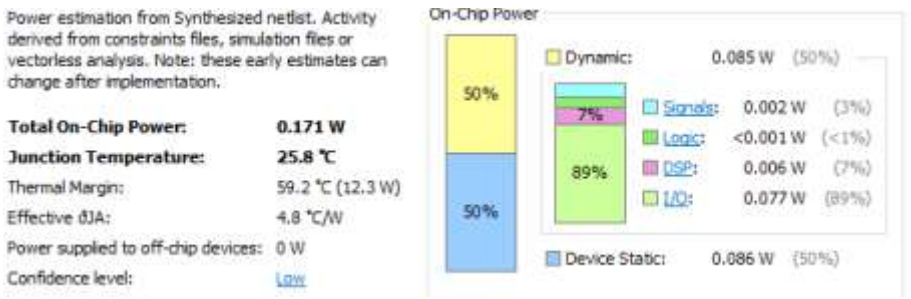

Figure 25. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 85mW. Junction Temperature is 25.8ºC. Total on-chip power is 171mW as shown in Figure 25.

H. Power Analysing Using SSTL_18_II For 3 Different Voltage Level: Minimum, Average, Maximum

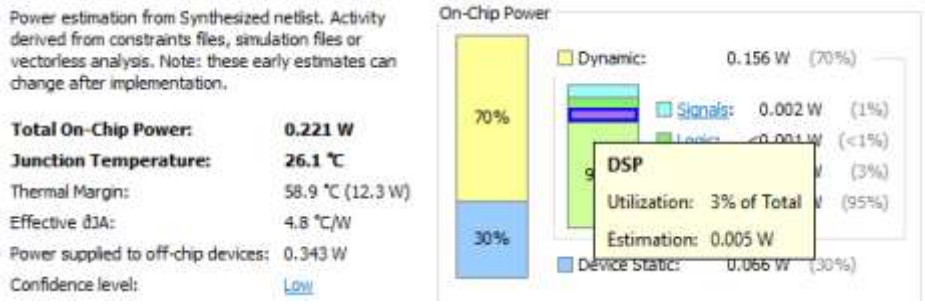

Figure 26. Power Analysis of FIR Filter for Minimum Voltage Level

For minimum voltage level, dynamic power is 156mW. Junction Temperature is 26.1ºC. Total on-chip power is 221mW as shown in Figure 26.

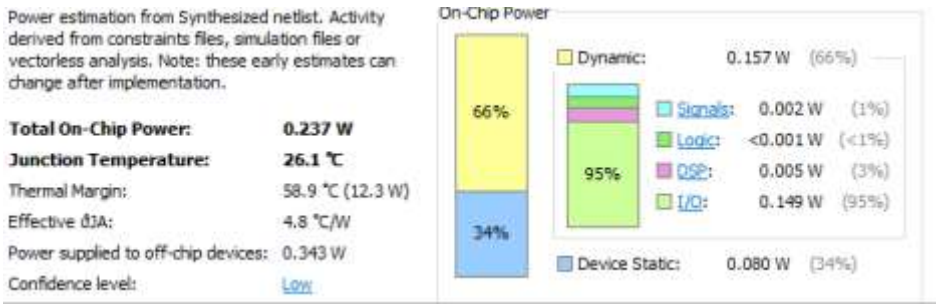

Figure 27. Power Analysis of FIR Filter for Average Voltage Level

For average voltage level, dynamic power is 157mW. Junction Temperature is 26.1ºC. Total on-chip power is 237mW as shown in Figure 27.

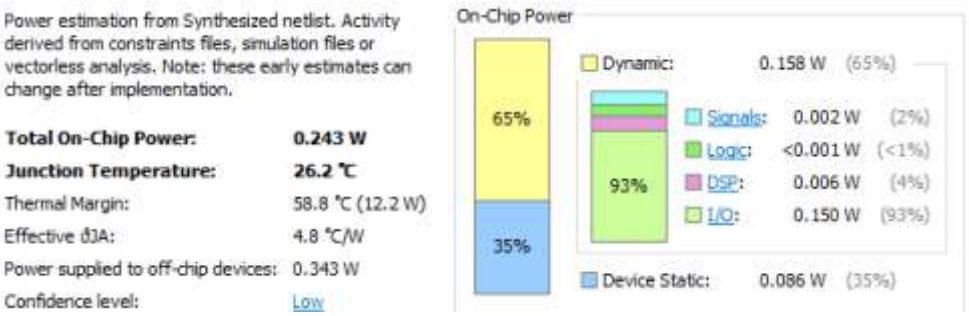

Figure 28. Power Analysis of FIR Filter for Maximum Voltage Level

For maximum voltage level, dynamic power is 158mW. Junction Temperature is 26.2^{o}C. Total on-chip power is 243mW as shown in Figure 28.

4. Conclusion

We are able to reduce 91% power dissipation with usage of LVCMOS15 in place of power hungry IO standards of SSTL family. We have also verified that our design is able to operate on all three levels of voltage. Junction temperature is always below 30^{o}C. The IO power dissipation of HSTL, HSUL, MOBILE_DDR, PCI33_3 and LVTTL is in between power dissipation of both LVCMOS and SSTL.

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