International Journal of Control and Automation
Vol. 10, No. 11 (2017), pp.51-60
http//dx.doi.org/10.14257/ijca.2017.10.11.05

Integrated Design of Low-power Adiabatic Dynamic CMOS Logic using 0.18μm Standard CMOS Model for Circadian Rhythm OLED Illumination System

Seung-Il Cho[1] and Michio Yokoyama[2*]

[1]*Innovation Center for Organic Electronics, Yamagata University, 1-808-48, Arcadia, Yonezawa, Yamagata, 992-0119, Japan*
[2]*Graduate School of Science and Engineering, Yamagata University, 4-3-16, Jonan, Yonezawa, Yamagata, 992-8510, Japan*
[1]*cho_si@yz.yamagata-u.ac.jp*, [2]*yoko@yz.yamagata-u.ac.jp*

Abstract

The organic light emitting diode (OLED) illumination systems are dimming using not only analysis results of the big data which is correlation analysis about vital signs and parameters in the bedroom but also circadian rhythm which is any biological process displayed an endogenous, entrainable oscillation of about 24 hours. Therefore, a low-power and compact design of dimming part is required for circadian rhythm OLED illumination system. In this paper, the influence on the load capacitance (C_L) value of the adiabatic dynamic CMOS logic (ADCL) is examined. The adiabatic operation and reduction effect of power consumption are confirmed using hspice with 0.18μm standard MOS model. Layout area of the 3-bit digital PWM using ADCL without voltage holding capacitance (C_S) was 6,279.7um^2. Furthermore, integrated design of that is simulated for circadian rhythm OLED illumination system. The power consumption of the ADCL digital PWM without C_S for all bit patterns decreased by 57.7 % compared to that of the ADCL PWM with C_S.

Keywords: *adiabatic dynamic CMOS logic (ADCL), voltage holding capacitance, parasitic capacitance, low-power design, digital PWM, circadian rhythm OLED illumination system*

1. Introduction

In recent years, the number of patients of lifestyle-related diseases and their preliminary group have been increasing. The prevention of lifestyle-related diseases is very important to save healthy living [1-2]. Therefore, personal health check and care have attracted significant attention and are increasing using wearable device, ubiquitous device and internet of things (IoT) service [3-4]. Moreover, environment development for deep sleep has been studied using correlation analysis results of the big data about vital signs and parameters in the bedroom; breath rate, heart rate, temperature, humidity, brightness of illumination *etc*. The organic light emitting diodes (OLEDs) have been widely used for illumination of the bedroom because those are the closest to natural light. Presently, the OLED illuminations are dimming using not only analysis results of the big data but also circadian rhythm which is any biological process displayed an endogenous, entrainable oscillation of about 24 hours as shown in Figure 1[5-6]. An institution of Yamagata university, Smart MIRAI House, was built to demonstrate the research results for the living environment of the near future and to verify correlation between big data

Received (April 1, 2017), Review Result (July 21, 2017), Accepted (September 15, 2017)

ISSN: 2005-4297 IJCA

analysis and deep sleep using circadian rhythm OLED illumination system as shown Figure 2.

Recently, the circadian rhythm OLED illumination system consists of a power part, dimming circuit part and OLED part, as shown in Figure 1[7-8]. Although power consumption of the dimming circuit part is the lowest, size and power consumption of the

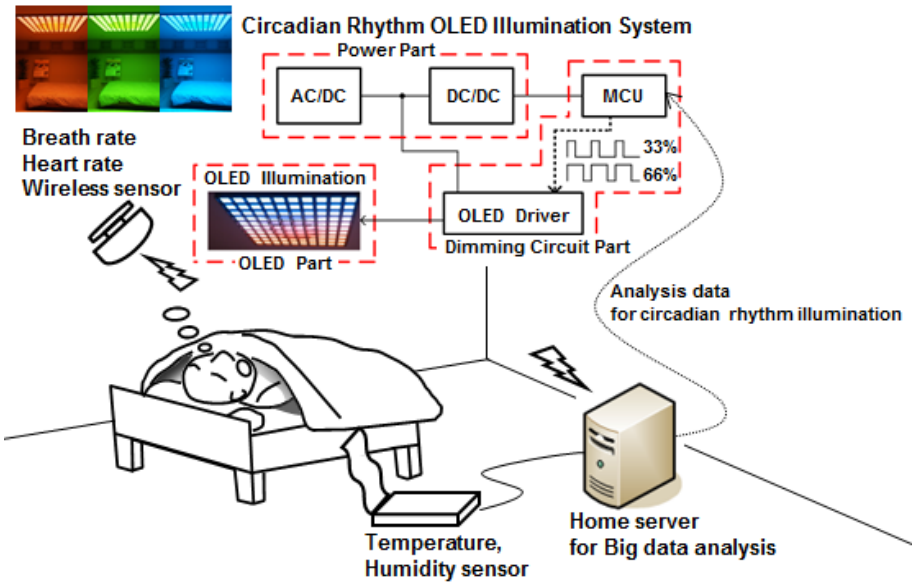
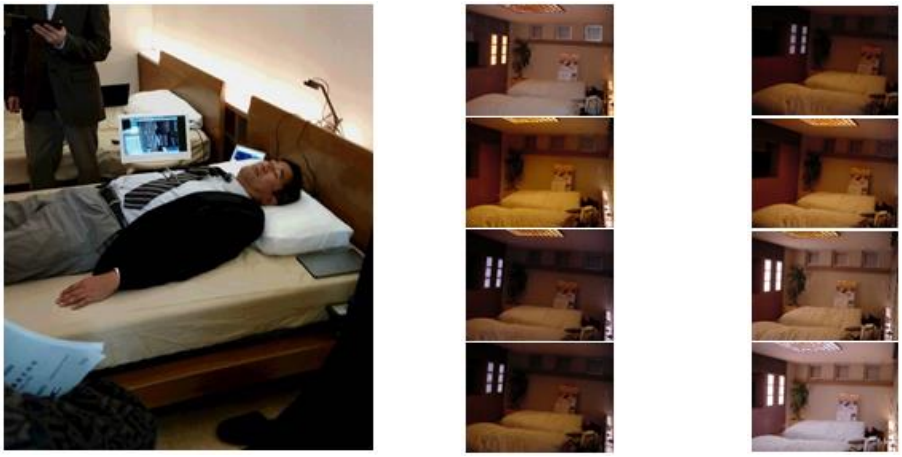


Figure 1. Circadian Rhythm OLED Illumination System using Big Data Analysis

digital circuit, including the dimming circuit part will increase for high-performance OLED illumination systems in the near future. Therefore, a low-power and compact design of the dimming circuit part is required for low-power circadian rhythm OLED illumination systems. The pulse width modulation (PWM) is normally used for the dimming circuit [9-11].

The adiabatic dynamic CMOS logic (ADCL) was studied to reduce the power loss in a conventional CMOS logic for the low-power design of a logic circuit [12-21]. Power loss occurs by a sudden change in voltage from high to low and from low to high in CMOS logic with a direct current (DC) power supply. On the other hand, this power loss is reduced by slowly increasing and decreasing the power supply voltage in ADCL with the alternate current (AC) that is synchronized with for a change to high or low.



(A) Experiment On Bed **(B) Sleep Mode** **(C) Wake Up Mode**

Figure 2. Experiment Environment using Circadian Rhythm OLED Illumination System at Smart MIRAI House

The ADCL needs a load capacitance (C_L) to maintain the output voltage and to prevent backflow of the current. However, power consumption is increased by the C_L. Recently, the miniaturization of integrated circuits is progressing year by year, and it is expected that the voltage holding capacitance (C_S) can be reduced and removed in ADCL because the power supply voltage is lowered and the parasitic capacitance (C_P) exist on transistors. In this paper, the influence on the C_L value of the ADCL is examined. And layout of the ADCL 3-bit digital PWM was designed using Rohm 0.18μm standard CMOS model. Furthermore, the adiabatic operation and reduction effect of power consumption are confirmed by hspice computer simulation.

The remainder of this paper is organized as follows. Section 2 describes the adiabatic charging, and standard operation of adiabatic logic. And the influence on the C_L value of the ADCL is examined. A low-power ADCL digital 3-bit PWM was designed for the circadian rhythm OLED illumination systems. And layout of that was designed using the Rohm 0.18μm standard CMOS model in section 3. Section 4 reports the post-simulation results of designed integrated circuits using the hspice. Finally, section 5 concludes the paper.

2. Adiabatic Logic

2.1. Adiabatic Charging

During a sudden transition between high and low levels of the input voltage, a load capacitor cannot be charged and discharged immediately. Power dissipation occurs by the resistive component of the logic circuit in the conventional CMOS logic because this logic circuit uses a constant voltage; DC power supply. To reduce the power dissipation, adiabatic charging is one of the promising candidates with AC power, which has a slower rising/falling time than charge/discharge time constant [12-15].

Figure 3 shows the operations at a normal RC circuit with a DC signal, adiabatic charging, and unsynchronization. The input signal $v_I(t)$, voltage drop of the resistance $v_R(t)$ and power dissipation $P_R(t)$ in Figure 3(a) are expressed in equation (1), (2), and (3), respectively, where τ is the rising time of input, ϕ is unsynchronized period and $u(t)$ is the unit step function [15-21].

$$v_I(t) = \frac{V_I}{\tau}(t+\phi)[u(t) - u(t-(\tau-\phi))] + V_I[u(t-(\tau-\phi))] \quad (1)$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u(t-(\tau-\phi))\right]+\frac{V_I\phi}{\tau}e^{-\frac{t}{CR}} \quad (2)$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u(t-(\tau-\phi))\right]+\frac{V_I\phi}{\tau R}e^{-\frac{t}{CR}}\right]^2 \quad (3)$$

In the case of the DC signal ($\tau = \phi$) at the input signal, the energy dissipation occurred at the load R until the end of charging at the load C, as shown in Figure 3(b). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ at Figure 3(a) are

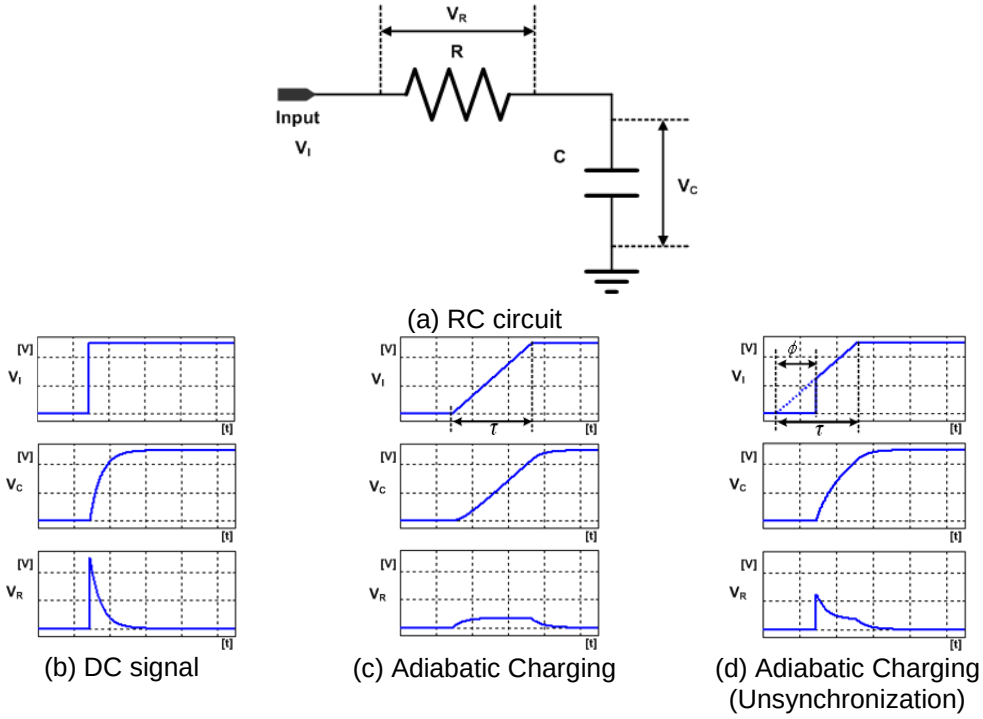


Figure 3. Operation of the RC Circuit

$$v_I(t) = V_I[u(t)], \quad (4)$$

$$v_R(t) = V_I e^{-\frac{t}{CR}}, \quad (5)$$

$$P_R(t) = \frac{V_I^2}{R}e^{-\frac{2t}{CR}}. \quad (6)$$

On the other hand, in the case of the AC signal ($\phi = 0$) as the input signal, adiabatic charging and little power dissipation are shown in Figure 3(c). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are

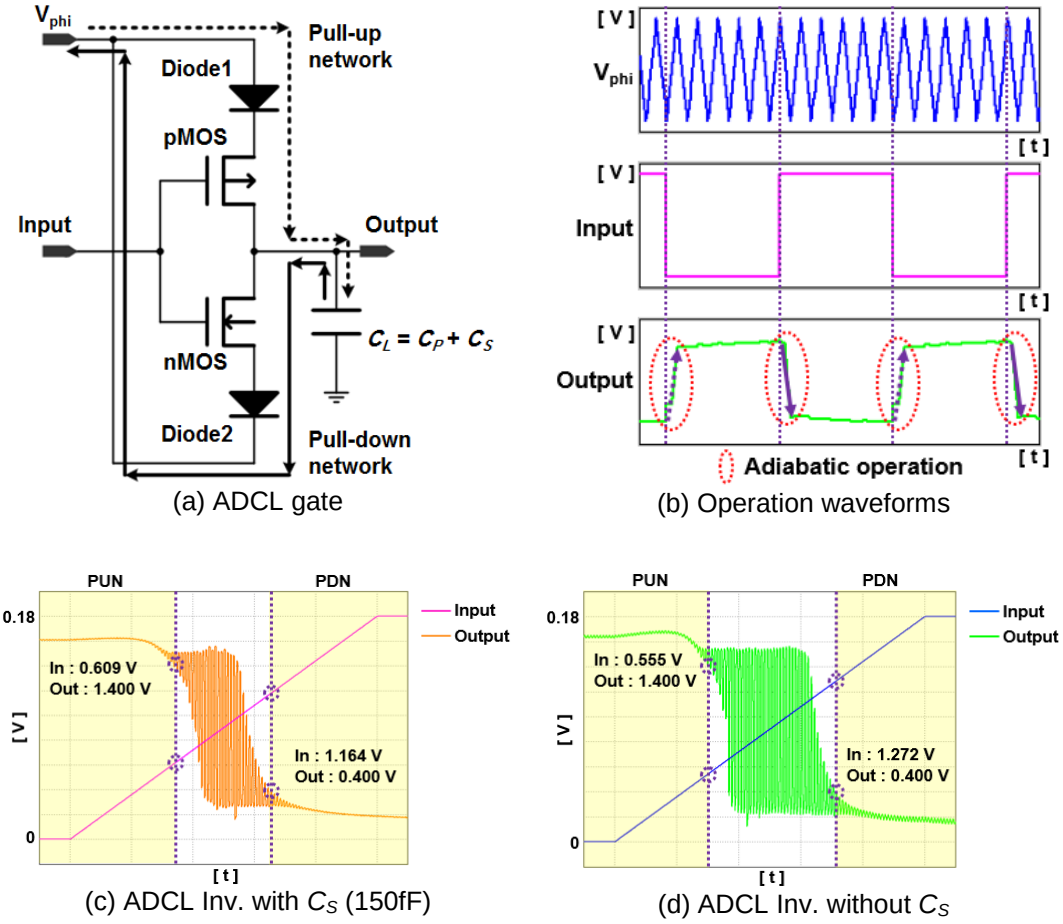
$$v_I(t) = \frac{V_I}{\tau}t[u(t)-u(t-\tau)]+V_I[u(t-\tau)], \quad (7)$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \quad (8)$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2 . \quad (9)$$

The region of adiabatic charging decreased with increasing ϕ of the AC signal, as shown in Figure 3(d). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are expressed as equation (1), (2), and (3) respectively [19]. There is an influence of power consumption depending on the size of the C_L as shown in equation (3), (6), and (9) respectively.

2.2. Adiabatic Dynamic CMOS Logic (ADCL) using Parasitic Capacitance



(a) ADCL gate (b) Operation waveforms

(c) ADCL Inv. with C_S (150fF) (d) ADCL Inv. without C_S

Figure 4. Principles of ADCL Inverter

The ADCL gate consists of the CMOS logic, AC power and two diodes for the adiabatic charging/discharging as it is applied to the CMOS logic. Figure 4 shows an ADCL inverter gate. In this circuit, because the output voltage of the ADCL gate is synchronized with the power supply, V_{phi}, the operating speed of the ADCL circuits is determined by the frequency of V_{phi}. Figure 4(a) and (b) show the principle of the ADCL inverter [14-21].

Principle (I) : Pull-up network (PUN)

In Figure 4(a), pMOS and nMOS are on and off, respectively. In this case, the supply current path is generated and the load capacitor C_L is charged adiabatically by V_{phi}. The high level is then kept with diode1.

Principle (II) : Pull-down network (PDN)

Under this condition, pMOS and nMOS are off and on, respectively. In this case, the current path is generated, as shown in Figure 4(a) and the charge in C_L is discharged adiabatically into V_{phi}.

Consequently, the ADCL inverter works in the adiabatic mode, as shown in Figure 4(b). On the other hand, if the difference between V_{phi} and the voltage across C_L is large, adiabatic operation will not be established and power will be largely dissipated. The ADCL operates the adiabatic charging whenever logic level of the output is changed from high level to low and vice versa. Furthermore, the charge can be reused because the charge reverts to the power source at the discharge of C_L. In this conventional ADCL circuit, the C_L is the C_P and the C_S [17-20]. It is possible to maintain the output voltage using only the C_P of 0.18μm standard COMS model without C_S as shown in Figure 4(d).

3. Integrated Design of 3-bit Digital PWM using ADCL without C_S

The PWM is normally used for the dimming circuit of illumination systems. Figure 5 shows integrated design of 3-bit digital PWM using ADCL gates without C_S. When input bits (LD0, LD1, LD2) are LLH, LHH, the output pulse width of PWM is approximately 33.3 %, 66.6 % respectively and characteristics of ADCL, the adiabatic charging/discharge are confirmed. The power consumption of ADCL digital PWM is lower than it of CMOS digital PWM through adiabatic charging/discharging operation.

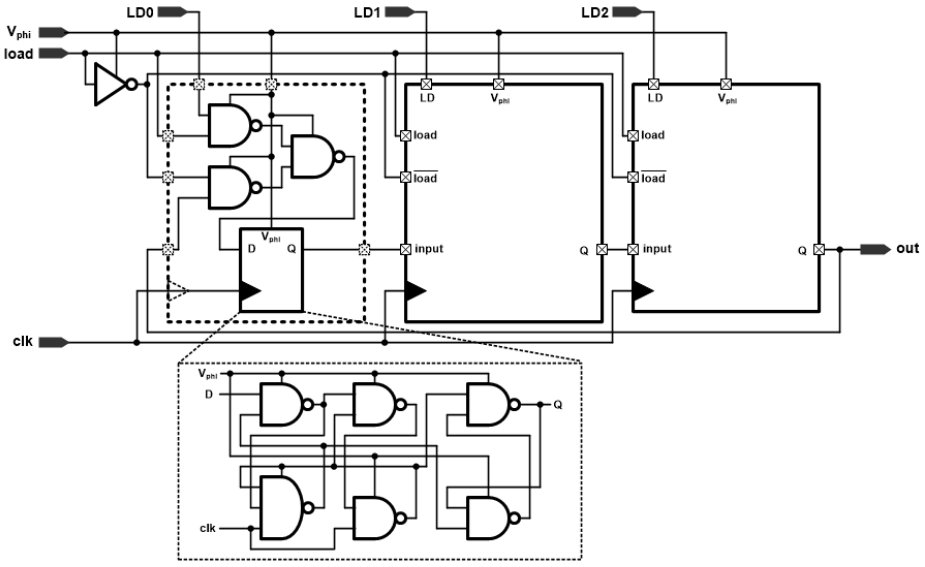
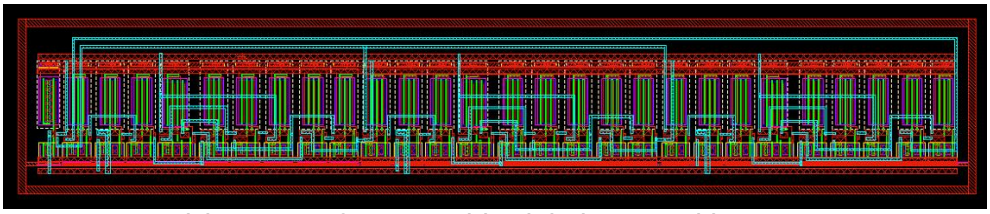
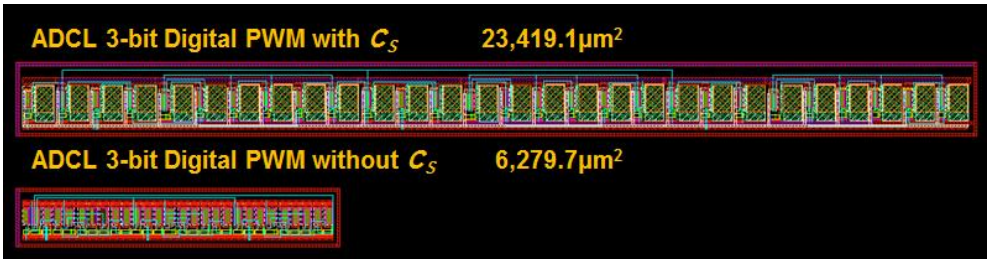


Figure 5. 3-bit Digital PWM using ADCL without C_S

Figure 6 shows layout of the ADCL 3-bit PWM digital PWM with C_S and without C_S using Rohm 0.18μm standard CMOS model. Layout area of the ADCL 3-bit PWM digital PWM with C_S is 23,419.1um^2 and that of the ADCL 3-bit PWM digital PWM without C_S is 6,279.7um^2, which decreased by approximately 73.18 % compared to that of the ADCL 3-bit PWM digital PWM with C_S.



(a) Layout of ADCL 3-bit Digital PWM without C_S



(b) Comparison of Layout Area

Figure 6. Layout of ADCL 3-bit Digital PWM

4. Post-simulation Results

The 3-bit digital PWM using ADCL without *Cs* was simulated using hspice with 0.18μm standard MOS model. The DC power, AC power and clock were 1.8V, 33kHz triangular wave, 3kHz, respectively. Figure 7 shows post-simulation results of ADCL 3-bit digital PWM without C_S. Adiabatic charge/discharge was confirmed using only C_P of 0.18μm standard CMOS model by post-simulation. When input bits (LD0, LD1, LD2) are LLH, LHH, the output pulse width of PWM is approximately 33.3 %, 66.6 % respectively. Moreover, characteristics of ADCL, the adiabatic charging/discharge are confirmed as shown in Fig.7 a, b.

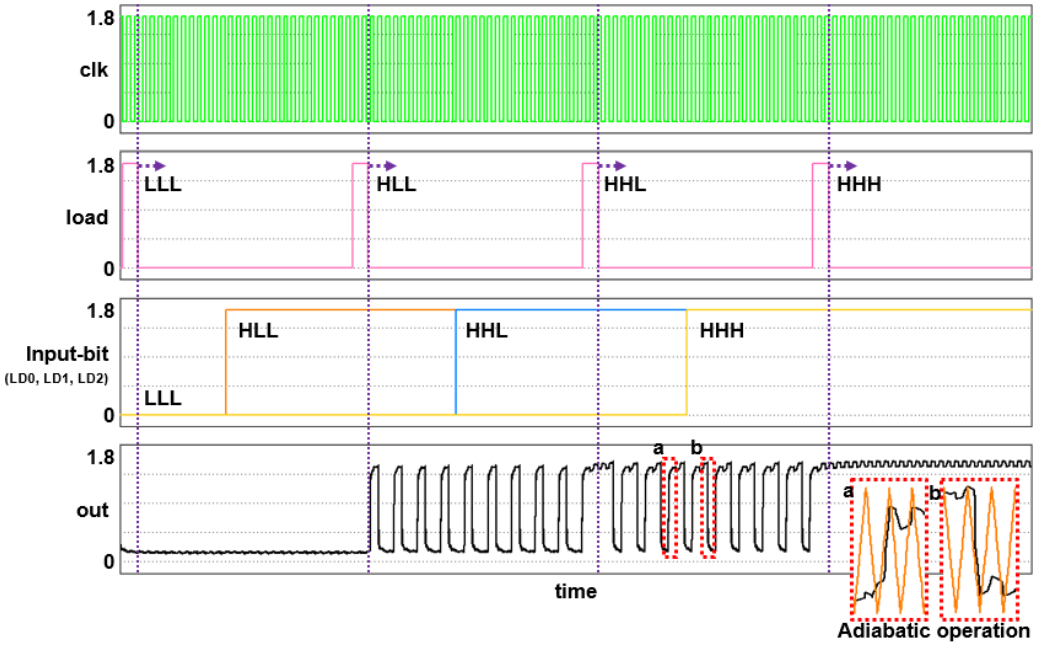


Figure 7. Post-simulation Results of ADCL 3-bit Digital PWM without C_S

Tabla 1 shows power consumption of digital 3-bit PWM respectively. The power consumption of the ADCL digital PWM with C_S and without C_S were compared, as shown in Fig. 8. The power consumption of the ADCL digital PWM without C_S for all bit patterns decreased by 57.7 % compared to that of the ADCL PWM with C_S.

Table 1. Power Consumption of Digital 3-bit PWM [nW]

input-bit / Digital PWM	LLL (PW = 0%)	HLL (PW = 33.3%)	HHL (PW = 66.6%)	HHH (PW = 100%)
CMOS	10.390	21.170	21.670	9.163
ADCL with C_S	3.276	9.214	9.230	3.288
ADCL without C_S	1.560	3.675	3.716	1.624

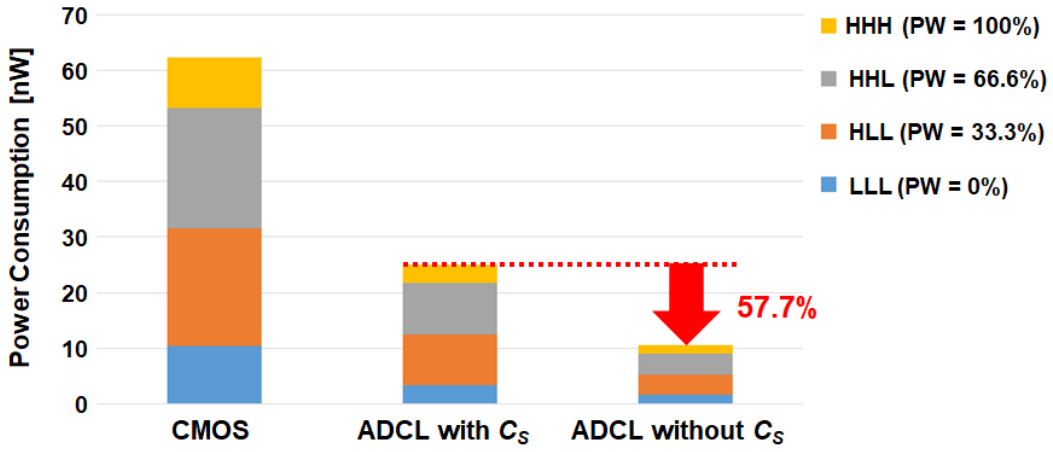


Figure 8. Comparison of the Power Consumption

5. Conclusion

The influence on the C_L of the ADCL was examined and layout area of the ADCL 3-bit PWM digital PWM without C_S was lower than that of the ADCL 3-bit PWM digital PWM with C_S using 0.18μm standard CMOS model. Furthermore, the adiabatic operation and reduction effect of power consumption were confirmed. The power consumption of the ADCL digital PWM without C_S decreased that of the ADCL PWM with C_S.

This shows the potential of the ADCL digital PWM in future low-power and miniaturization of OLED dimming systems. Moreover, at the Smart MIRAI House, the research results for the living environment of the near future are demonstrated and correlation between big data analysis and deep sleep using circadian rhythm OLED illumination system are verified.

Acknowledgments

This paper is a revised and expanded version of a paper entitled Low-power Design of Adiabatic Dynamic CMOS Logic using Parasitic Capacitance of 0.18μm Standard CMOS Model presented at the 6th International Conference on Next Generation Computer and Information Technology, Ho Chi Minh City, Vietnam, August 16-18, 2017.

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

[1] N. C. Gassen, G. P. Chrousos, E. B. Binder and A. S. Zannas, "Life stress, glucocorticoid signaling, and the aging epigenome: Implications for aging-related diseases", Neuroscience & Biobehavioral Reviews, vol. 74, part B, **(2017)**, pp. 356-365.
[2] M. Yokoyama, T. Negishi, M. Mizunuma, K. Otani, H. Hanaki and K. Nishimura, "Multiple Reression Analysis and Learning System for Estimation of Blood Pressure Variation using Photo-Plethysmograph Signals", International Journal of Computers and Their Applications, vol. 23, no.1, **(2016)**, pp. 12-18.
[3] SS. Al-Majeed, IS. Al-Mejibli and J. Karam, "Home telehealth by internet of things (IoT)", Proceedings of the 28th Canadian Electrical and computer engineering (CCECE), Halifax, Canada, **(2015)**.
[4] S. M. Riazul Islam, D. Kwak, MD. Humaun Kabir, M. Hossain and K.-S. Kwak, "The Internet of Things for Health Care: A Comprehensive Survey", IEEE Access, vol. 3, **(2015)**, pp. 678-708.
[5] K. Keränen, J. Ollila, E.-M. Sarjanoja, S. Yrjänä, A. Huttunen, M. Korkalainen and P. Makkonen, "Large area flexible lighting element controlled by mobile phone user interface", Proceedings of the 6th Electronic System-Integration Technology Conference (ESTC), Grenoble, France , **(2016)**, September, 13-15.
[6] M. Kayaba, K. Iwayama, H. Ogata, Y. Seya, K. Kiyono, M. Satoh and K. Tokuyama, "The effect of nocturnal blue light exposure from light-emitting diodes on wakefulness and energy metabolism the following morning", Environmental Health and Preventive Medicine, vol. 19, no.5, **(2016)**, pp. 354-361.
[7] S. Tarashioon, S.W Koh, W.D van Driel and G.Q. Zhang, "Temperature dependency in performance of solid state lighting drivers", Proceedings of the 12th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, Linz, Austria, **(2011)**.
[8] J.Y. Tsao, M.E. Coltrin, Mary H. Crawford and J. A. Simmons, "Solid-State Lighting: An Integrated Human Factors, Technology, and Economic Perspective", Proceeding of the IEEE, vol. 98, no. 7, **(2010)**, pp. 1162-1179.
[9] B.J. Huang, M.S. Wu, P.C. Hsu, J.W. Chen and K.Y. Chen, "Development of high-performance solar LED lighting system", Energy Conversion and Management, vol. 51, no. 8, **(2010)**, pp1669-1675.
[10] D. Gacio, J.M. Alonso, J. Garcia, L. Campa, M. Crespo and M. Rico-Secades, "High Frequency PWM Dimming Technique for High Power Factor Converters in LED Lighting", Proceedings of the Applied Power Electronics Conference and Exposition (APEC) 2010, Palm springs, USA, **(2010)**.
[11] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin and S.-C. Mou, "A High-Efficiency Dimmable LED Driver for Low-Power Lighting Applications", IEEE Transactions on Industrial Electronics, vol. 57, no. 2, **(2010)**, pp735-743.
[12] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzains and E. Y.-C. Chou, "Low-power digital systems based on adiabatic-switching principles", IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 2, no. 4, **(1994)**, pp. 398-407.
[13] A. G. Dickinson and J. S. Dencker, "Adiabatic dynamic logic", IEEE Journal of Solid-State Circuits, vol. 30, no. 3, **(1995)**, pp. 311-315.
[14] Y. Takahashi, S. Nagano, N.Anuar, T. Sekine and M.Yokoyama, "On chip LC resonator circuit using an active inductor for adiabatic logic", Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and System. Cancun, Mexico, **(2009)**.
[15] N. Anuar, Y. Takahashi and T. Sekine, "4x4-bit array two phase clock adiabatic static CMOS logic multiplier with new XOR", Proceedings of the 18th IEEE/IFIP VLSI System on Chip Conference (VLSI-SoC), Madrid, Spain, **(2010)**, pp. 27-29.
[16] Y. Takahashi, K. Konta, K. Takahashi, K. Shouno, M. Yokoyama and M. Mizunuma, "Carry propagation free adder/subtracter using adiabatic dynamic CMOS logic circuit technology", IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences, vol. E86-A, no. 6, **(2003)**, pp.1437-1444.
[17] S.-I. Cho, T. Harada, and M. Yokoyama, "Design of the ultra-low-power synchronizer using ADCL buffer for adiabatic logic", IEICE Electronics Express, vol. 9 no. 20, **(2012)**, pp1576-1585.
[18] S.-I. Cho, S.-K. Kim, T. Harada and M. Yokoyama, "Design of low-power clock generator synvhronized with AC power for adiabatic dynamic CMOS logic", IEICE Electronics Express, vol. 10 no. 20, **(2013)**, pp1-9.
[19] S.-I. Cho, M. Mizunuma and M. Yokoyama, "Optimized Design of Low-power Adiabatic Dynamic CMOS Logic Digital 3-bit PWM for SSL Dimming System", IEIE Transactions on Smart Processing and Computing, vol. 2, no.4, **(2013)**, pp. 248-254.
[20] S.-I. Cho, S.-D. Yeo, S.-K. Kim and M. Yokoyama, "Optimization of Control Block of 3-bit PWM using Adiabatic Dynamic CMOS Logic for OLED Illumination System Based on Internet of Things Service", International Journal of Smart Home, vol. 10, no.9, **(2016)**, pp. 317-328.

[21] S.-I. Cho and M. Yokoyama, "Low-power Design of Adiabatic Dynamic CMOS Logic using Parasitic Capacitance of 0.18μm Standard CMOS Model", Proceedings of the 6th International Conference on Next Generation Computer and Information Technology, Ho Chi Minh City, Vietnam, **(2017)**.

Authors

Seung-Il Cho, he was born in Gwang-ju, Korea, on August 9, 1980. He received his B.S. and M.S. degree in marine electronic and communication engineering from Mokpo National Maritime University, Korea in 2006 and 2008, respectively. He was an associate research engineer at R&D division of Tomato LSI in 2008 to 2010. He received his Ph.D degree in Bio-systems engineering, Graduate school of Science and Engineering from Yamagata University, Japan in 2013. He is currently an Assistant Professor in the Innovation Center for Organic Electronics, Yamagata University. His research interests include adiabatic dynamic CMOS logic (ADCL), digital/analog integrated circuit design, organic thin film transistor (OTFT) circuit design and organic light emitting diode (OLED) flexible display.

Michio Yokoyama, he was born in Yamagata, Japan, on March 1st, 1967. He received his B.E. degree in electrical engineering from Yamagata University in 1989, and his M.E. degree in electrical and communication engineering and Ph.D degree in electronic engineering from Tohoku University in 1991 and 1994, respectively. From 1994 to 2001, he joined the Research Institute of Electrical Communication (RIEC), Tohoku University, Sendai, Japan, where he was engaged in research on the design and development of RF-CMOS devices, such as power amplifier modules for digital cellular phone systems. Since 2001, he has joined Yamagata University, Yonezawa, Japan, and was engaged in research on ubiquitous healthcare system, Information and Communications Technologies (ICT), Internet of Things (IoT). He is a member of The Japan Institute of Electronics Packaging, The Japan Society of Applied Physics, The Institute of Electrical Engineers of Japan and The Institute of Electronics, Information and Communication Engineers.

