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Study of SRAM Standby Leakage Reduction Techniques for Deep-submicron CMOS Technology

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Abstract

With scaling down of the technology, share of leakage is increasing in total power consumption of Static Random Access Memories (SRAMs). This paper presents the detailed study of conventional and proposed 6T SRAM standby leakage reduction techniques for advanced technology node. A 6T SRAM bitcell, in 45 nm technology with size 0.38 μm^2, has been designed. This study shows that the performance of these leakage reduction techniques depends on the composition of cell standby leakage in terms of its components, and the composition of cell standby leakage itself depends on technology as well as temperature. Finally, efficient combination of SRAM standby leakage reduction techniques for advanced technology, have been proposed here.

Keywords*: Low voltage, low power, SRAM, standby, leakage currents, subthreshold, process variation*

1. Introduction

With the progression of technology and continuous device scaling, Static Random Access Memory (SRAM) has been and continues to be the largest component in state-of-the-art VLSI systems or Systems-on-Chip (SoC) [1-2]. However, one of the negative side effects of technology shrinking is the increase in transistor leakage current [2]. Thus for every new technology generation the contribution of leakage in total chip power consumption, of caches and other SRAM memory content is increasing significantly since leakage power is proportional to the number of transistors on chip [3-5]. To minimize the leakage power, logic circuits can be gated but SRAM array has to remain powered to retain data as these are volatile memories. Thus it becomes important to focus on reduction of standby leakage power of SRAMs to achieve low power consumption.

Various techniques have been suggested to reduce the leakage power of SRAMs. At the device level, dual V_T devices and/or new device geometries have been proposed [4-6]. At the circuit level, controlling the cell nodes voltages were exploited to create low leakage paths during standby periods [7-9]. Following four basic techniques have been used to control the cell nodes voltages for SRAM standby leakage current reduction. (1) VDD lowering (VDDL) (2) VSS rising (VSSR) (3) Bitline floating (BLF) (4) Reversing body bias (RBB) [10, 14]. In this paper, firstly we have designed a 6T SRAM bitcell in 45 nm CMOS technology node, characterized by parameters like read SNM (static noise margin), hold SNM, WM (write margin) and read current [12]. Then, we have analyzed the standby leakage composition of this cell with temperature. This paper evaluates the conventional SRAM leakage reduction techniques and proposes a new combination of leakage reduction techniques for their leakage reduction efficiencies with cell stability.

Remaining part of this paper is organized as follows. Section 2 gives an overview of standby leakage currents in conventional 6T SRAM bitcell. Section 3 describes the design

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of 45 nm SRAM cell and also discusses the standby leakage components variations as well as their contribution in cell leakage with temperature. Section 4 and 5 evaluate existing SRAM leakage reduction techniques as well as proposed combination of leakage reduction techniques, with cell standby stability for the cell presented in section 3. Section 6 presents the results and analysis for all the reduction techniques listed in section 4. Finally, this work is concluded in section 7.

2. Standby Leakage in a Conventional 6t Sram Cell

Leakage power in a short channel MOS transistor constitutes with various current components flowing in the device [13]. Leakage current in a non-conducting (off-state) MOS transistor is comprised of subthreshold current (I_{SUB}), gate induced drain/source leakage ($I_{GI(D/S)L}$) and depletion punch-through leakage (I_{PUNCH}), while gate tunneling leakage (I_{GATE}) and reverse-biased pn junction leakage I_{JUNC} (from both source and drain), are independent of the state of the device [3]. I_{JUNC} contains a number of components and it is dominated by band-to-band tunneling effect [13]. For sub 100 nm technologies, subthreshold (I_{SUB}), gate (I_{GATE}) and gate induced drain/source leakage ($I_{GI(D/S)L}$) are the dominant leakage components [14, 16]. Figure 1 shows the paths of these dominant leakage components in a 6T SRAM cell held in standby mode. As shown in this figure for standby/retention mode word line (WL) is deactivated to ground and bitlines are kept at VDD. In this figure both the pass transistors (PG1,PG2) with pull-down transistor (PD2) and pull-up transistor (PU1) are in off-state, while pull-down (PD1) and pull-up (PU2) transistors are in on-state. Subthreshold current flows in off-state transistor whose |VDS| is approaching or exceeding to VDD. Thus I_{SUB} is flowing in transistors PG1, PU1 and PD2. As I_{GATE} is independent of the transistor state, so it is contributed by all the six transistors of the cell at all time. While the magnitude of I_{GATE} varies with the appearing gate voltage with respect to source and/or drain bias of the respective device. Gate induced drain/source leakage ($I_{GI(D/S)L}$) is associated to all the off-state transistors due to the electric field crowding in gate-drain overlap and/or gate-source overlap regions [13-14]. Finally, as shown in Figure 1 total SRAM standby leakage current is given by the following equation [10].

$$I_{STANDBY} = I_{SUB}(PU) + I_{SUB}(PD) + I_{SUB}(PG) + I_{GATE}(PU) + I_{GATE}(PD) + I_{GATE}(PG) + I_{GIDL}/I_J(PU) + I_{GIDL}/I_J(PD) + I_{GI(D/S)L}/I_J(PG) \quad (1)$$

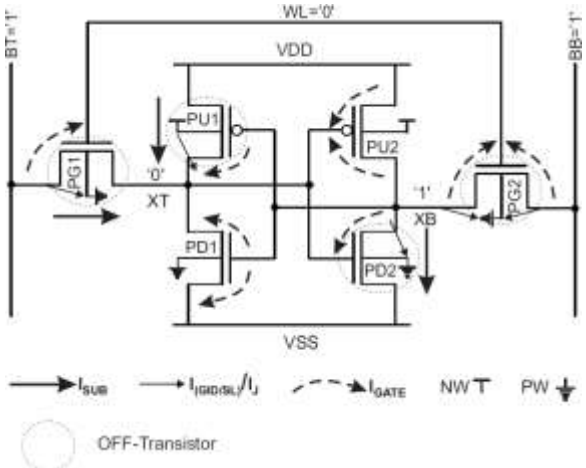


Figure 1. Schematic of Leakage Paths in the 6T SRAM Cell for Standby Mode

3. Design and Leakage Analysis of 45nm Sram Bitcell

Stability and write-ability of SRAM cell are measured in terms of its static noise margin (SNM) and write margin (WM) respectively. The stability of the bitcell in standby mode is characterize by its hold SNM, which is measured by putting both the pass transistors of the cell, OFF, with the help of WL kept at ground. WM and SNM of the cell decrease with reducing the supply voltage VDD [11] and also degrade further with process variation. Next bitcell characterization parameter, read current is a measure of read performance of the cell. These characterization parameters with design details of 6T SRAM cell, are shown in Table 1.

To see the area aspect in addition to the above mentioned cell characterization parameters the layout of this SRAM cell has been designed here as shown in Figure 2. Figure 3 demonstrates the relationship of dominant leakage components with temperature for the bitcell characterized above in 45 nm CMOS technology. For temperature 0 ^{o}C or below it, gate leakage is the dominant component and $G_{I(D/S)L}$ is recessive component of total standby leakage while subthreshold leakage comes in between. Also I_{GATE} is nearly independent of temperature. I_{GIDL}/I_J has a number of leakage current mechanisms like $G_{I(D/S)L}$, band-to-band tunneling, reverse-biased pn junction, later one increases exponentially as temperature rises. Thus with temperature rise I_{GIDL}/I_J increases slowly because it is dominated by $G_{I(D/S)L}$ component, which is independent of temperature. Even at 150 ^{o}C, I_{GIDL}/I_J is less than I_{GATE}. However I_{SUB} increases exponentially with rise of temperature and at higher side of temperature it becomes the dominant component of total cell leakage.

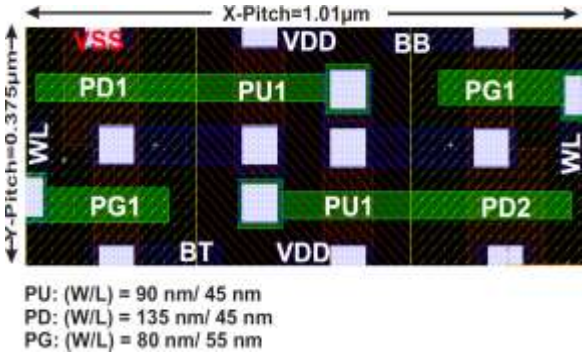
Furthermore, Figure 4 is representing the percentage distribution of all nine kinds of leakage components in total standby cell leakage for 25 ^{o}C and 85 ^{o}C temperature, for 45 nm bitcell designed in previous part of this section. At room temperature, gate leakage is the dominant component and at 85 ^{o}C subthreshold becomes the dominant leakage component. At high temperature, subthreshold leakage becomes the dominant component and $G_{I(D/S)L}$/junction leakage and gate leakage components are negligible.

Table 1. Design Summary of SRAM Bitcell

Technology	$(W/L)_{PU}$	$(W/L)_{PD}$	$(W/L)_{PG}$	SNM(V)	HOLD SNM(V)	WM(V)	I_{READ}(A)
45nm	90nm / 45nm	135nm / 45nm	80nm / 55nm	1.62E-01	3.58E-01	3.04E-01	5.13E-05

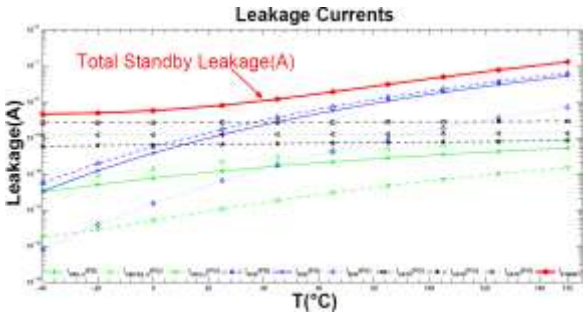
4. SRAM Cell Standby Leakage Reduction Techniques

Leakage currents are directly driven by the electric fields inside the device [6, 14]. In this paper, circuit level techniques have been used to control the voltages of different 6T SRAM cell nodes (VDD, VSS, BT/BB, PW, NW), to reduce the electric fields inside the devices of the cell, since leakage reduces drastically with lowering the electric fields inside a device. These SRAM cell standby leakage reduction techniques are named according to the used control of cell node/nodes voltages.



(a)

Figure 2. Layout of 6T SRAM Bitcell in 45 nm CMOS Technology



(b)

Figure 3. Leakage with Temperature of 6T SRAM Bitcell

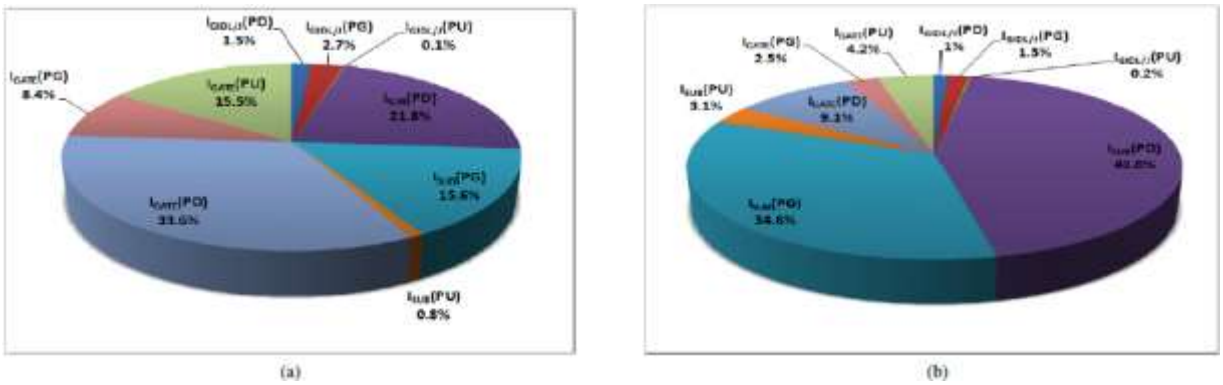


Figure 4. Leakage Composition of 45 nm CMOS Technology SRAM bitcell for (a) 25 °C (b) 85 °C

As these techniques take distinct control on SRAM transistor terminals, their leakage reduction effects are entirely different [10]. In the following part of this section these techniques have been investigated for 45 nm SRAM cell designed in section 3. To investigate leakage reduction techniques, we have carried out simulations to collect cell leakage data for each technique at worst leakage process corner (FF, 1.0V, 125°C).

4.1. VDD Lowering (VDDL)Technique

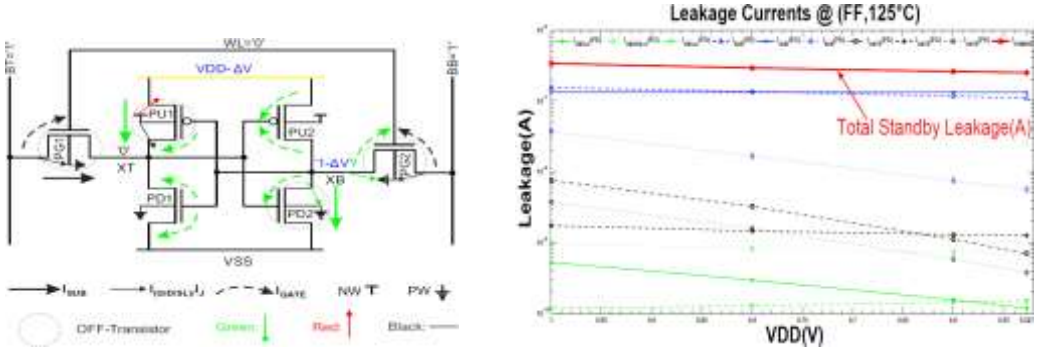
Figure 5 shows the schematic of VDDL technique along with its effect on leakage components of 45 nm bitcell. As shown in this schematic, lowering the VDD reduces the voltage of storage node XB. Thus reduction in $|V_{DS}|$ of PU1 and PD2, which results in improvement of I_{SUB} for these two transistors. Also with the lowering of VDD and hence V_{XB}, voltage difference between the gate and drain/source of all the devices of the cell except PG1 reduces, which leads to reduction in I_{GATE} of these devices exponentially. With reduction of VDD, I_{GIDL}/I_J of PD2 and PG2 decreases but for PU1 it increases because junction current varies with $|V_{BD}|$ of the device.

4.2. VSS Rising (VSSR) Technique

Figure 6, with schematic of VSSR technique illustrates its effects on leakage components of the bitcell designed in section 3. With rising VSS, I_{GATE} of all four devices of both the inverters are well reduced while for access transistor PG1 new path is created for gate leakage. In this scheme, in addition to reduction in the |VDS| of PU1, PG1 and PD2 devices, the threshold voltage of PG1 and PD2 devices also increases due to reverse body bias effect. Which results in significant reduction in I_{SUB} for these devices without creating new leakage paths. I_J of both PD2 and PG1 devices increases, while for PU1 it decreases. This technique reduces cell standby leakage $I_{STANDBY}$ significantly as I_{SUB} is the dominant leakage component.

4.3. Bitline Floating(BLF) Technique

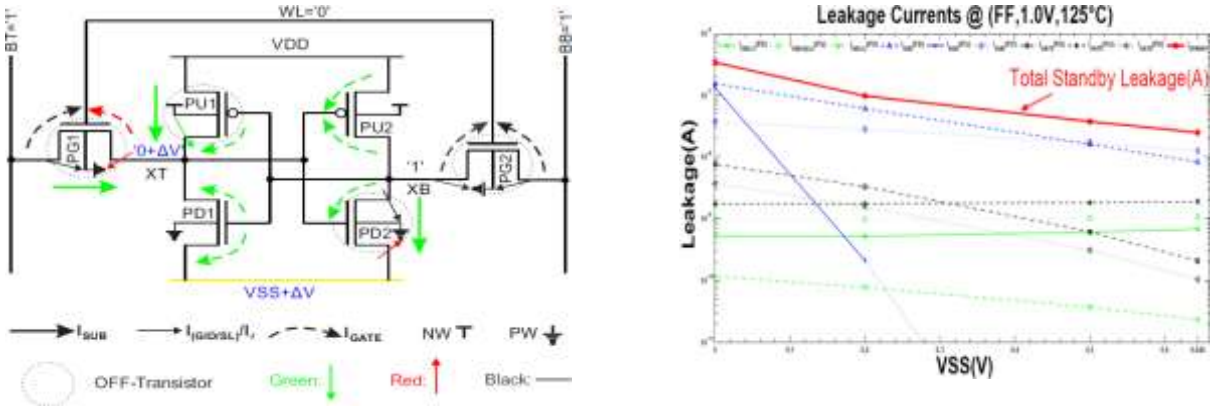
Figure 7, with the schematic of BLF technique elaborates the impact of this technique on leakage components of the bitcell designed in section 3. This technique demonstrates the reduction in I_{SUB}, I_{GATE} and I_{GIDL}/I_J for access transistors of the cell.



(a)

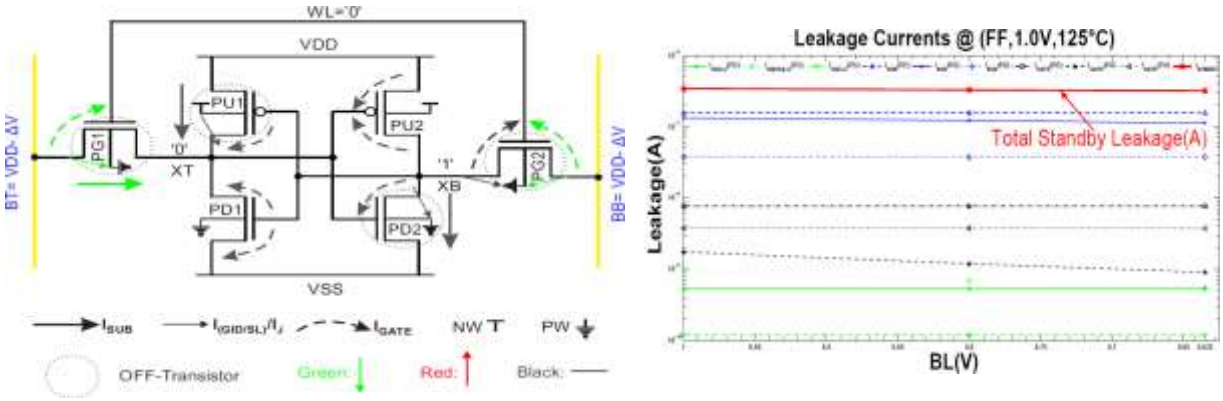
(b)

Figure 5. VDDL Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



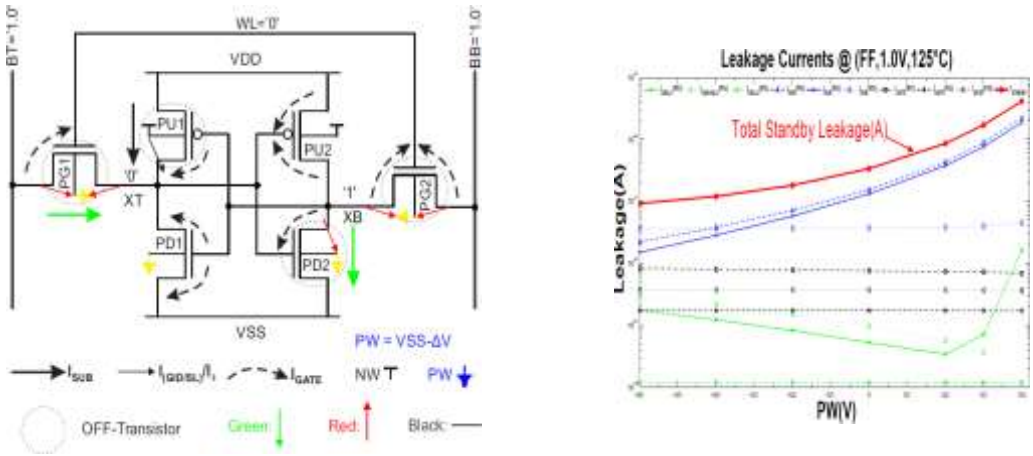
(a) (b)

Figure 6. VSSR Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



(a) (b)

Figure 7. BLF Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



(a) (b)

Figure 8. P-well Biasing Technique (a) Schematic (b) Effects on Leakage Currents of the Cell

4.4. Reversing Body Bias Techniques

As illustrated in Figure 8 and 9 with slightly forward body bias p-well as well as n-well does not allow I_{GIDL}/I_J to increase while I_{SUB} increases, further increase in forward bias increases junction as well as subthreshold currents drastically for all three type of devices. Thus forward body bias technique is not recommended for leakage reduction. Reverse body bias for both NMOS as well as PMOS devices increases threshold voltages of both the type of devices, hence I_{SUB} of off-devices is reduced while I_J of these devices is increased. Thus with reverse body bias technique, $I_{STANDBY}$ of the cell improves

significantly because I_{SUB} is the dominant component of cell standby leakage.**4.5. Combined Leakage Reduction Techniques**

Leakage reduction techniques discussed above, are only partially successful in reducing the standby leakage of a SRAM cell. Thus the combination ofthese techniques has been investigated to optimize the cell standby leakage reduction.

4.5.1. Combined VDD Lowering and Bitline Floating (VDDL+BLF) Technique

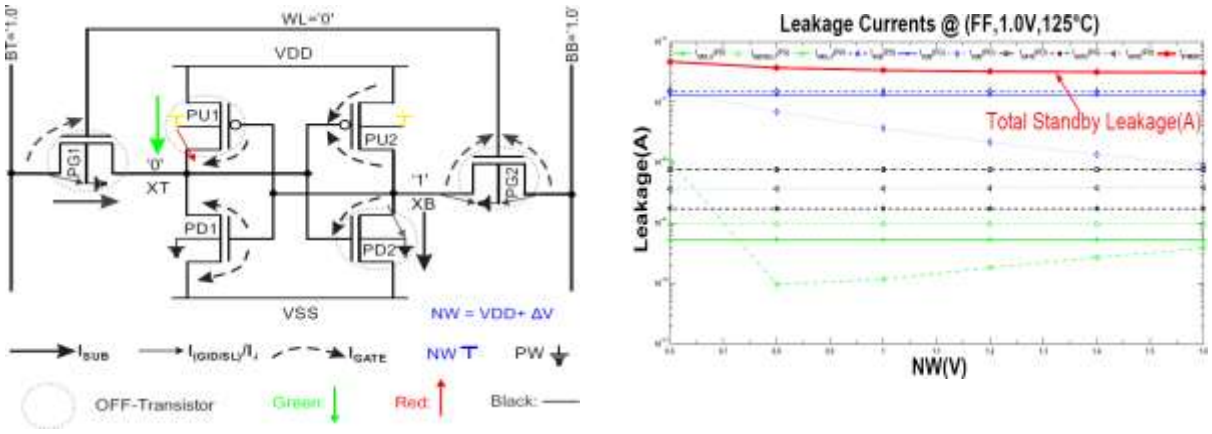
VDDL technique does not address the leakage associated to access transistors properly, whereas BLF technique deals effectively with the leakage of access transistors. Thus as demonstrated with the help of simulation results, shown in Figure 10, the combination of VDDL and BLF techniques promises better leakage reduction efficiency as compared to these two individual techniques.

4.5.2. Combined VSS Rising and Bitline Floating (VSSR+BLF) Technique

VSSR technique addresses the I_{SUB} of access transistor (PG1) upto a certain level, but it also leads to an increase in I_{GATE} and I_{GIDL}/I_J of this transistor instead of reducing it. These components of pass transistors can be addressed effectively with the help of BLF technique. Thus the combination of VSSR and BLF is a good approach to reduce the standby leakage of bitcell, which is demonstrated with the help of simulation results shown in Figure 11.

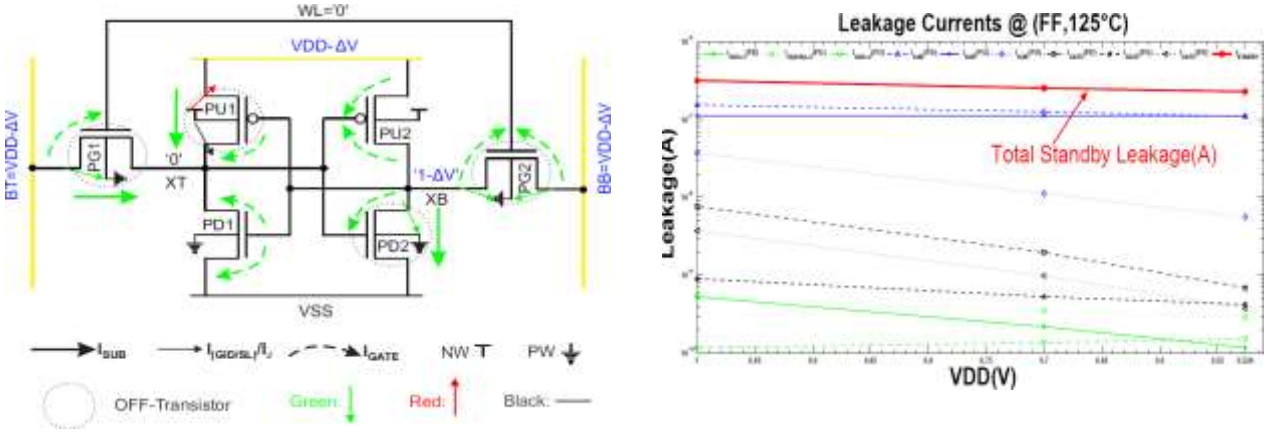
4.6. Proposed Combined Leakage Reduction Techniques

As per the discussion in sub-sections 4.5.1 and 4.5.2 of this paper, combined VDDL+BLF and VSSR+BLF leakage reduction techniques demonstrate significant reduction in bitcell standby leakage. The scope of further reduction in cell stand- by leakage has been investigated and achieved with the help of proposed combined techniques, without compromising the cell stability.



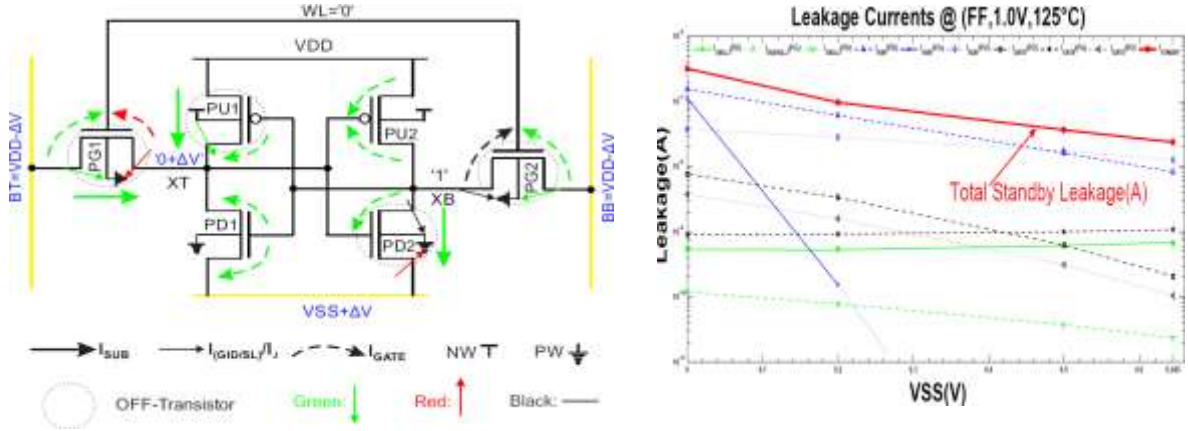
(a) (b)

Figure 9. N-well Biasing Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



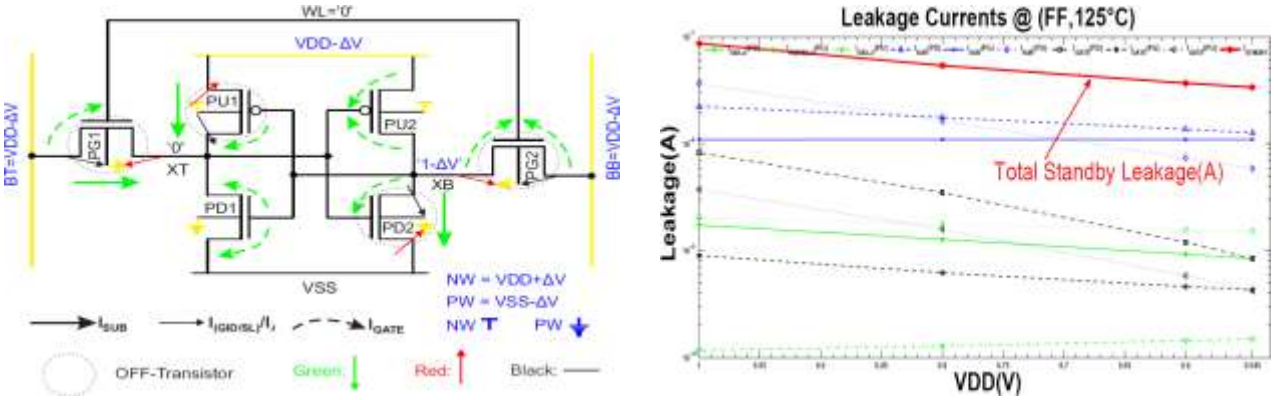
(a) (b)

Figure 10. Combined VDDL and BLF Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



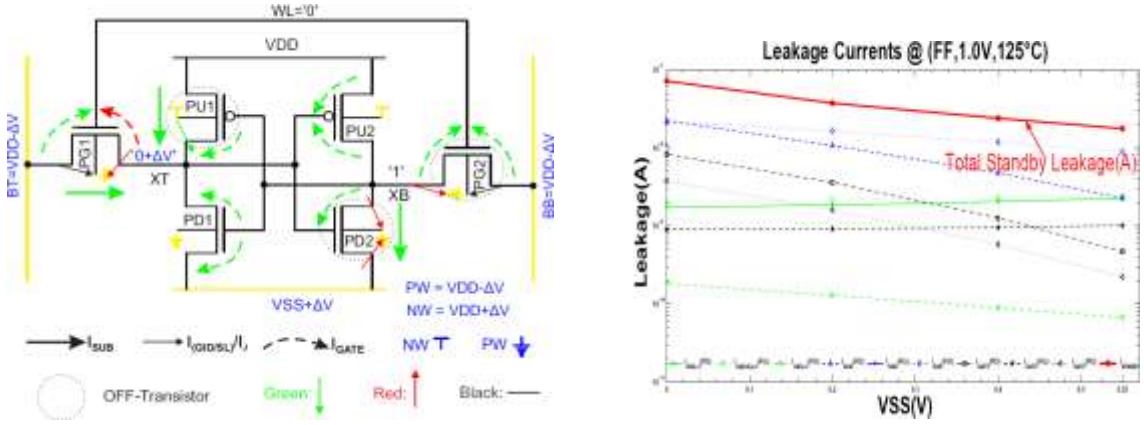
(a) (b)

Figure 11. Combined VSSR and BLF Technique (A) Schematic (B) Effects on Leakage Currents of the Cell



(a) (b)

Figure 12. Combined VDDL+BLF+RBBPW+RBBNW Technique (a) Schematic (b) Effects on Leakage Currents of the Cell



(a) (b)

Figure 13. Combined VSSR+BLF+RBBPW+RBBNW Technique (a) Schematic (b) Effects on Leakage Currents of the Cell

4.6.1. Proposed Combined VDD Lowering, Bitline Floating,Reverse Biased P-well and N-well (VDDL+BLF+RBBPW+RBBNW) Technique

This technique is further combination of VDDL+BLF approach with reverse biased p-well and n-well. The idea behind this technique is to reduce further the dominant components of cell standby leakage, which are subthreshold leakages of PD, PG devices at higher side of temperature, since higher temperature is a worst case parameter for cell leakage. Also, at higher temperature I_{SUB} of PU device is more dominant than its I_{GIDL}/I_J. Use of reverse biased p-well and n-well approaches to VDDL+BLF technique, further reduces I_{SUB} of PD, PG and PU devices due to body bias effect but increases I_{GIDL}/I_J of these devices. Thus as demonstrated in Figure 12, this scheme can be used to improve further the cell standby leakage, since the dominant leakage components are reduced at the cost of increase in recessive components.

4.6.2. Combined VSS Rising, Bitline Floating, Reverse Biased P-well and N-well (VSSR+BLF+RBBPW+RBBNW) Technique

As shown in Figure 13 this technique is a combination of VSSR+BLF with reverse biased p-well and n-well approach. Dominant leakage components of $I_{STANDBY}$ at higher temperatures are I_{SUB} of PD, PG and PU devices of the cell, which are reduced significantly by VSSR+BLF technique, further reduction of I_{SUB} of PD and PU devices can be achieved by using reverse biased p-well and n-well approaches with VSSR+BLF technique since threshold voltage of concerned devices increases due to reverse body bias effect. While this technique increases I_{GIDL}/I_J for these devices, which are recessive components for cell standby leakage. Thus, reduction in dominant components and rise in recessive components of cell leakage results in effective reduction in $I_{STANDBY}$ of the cell.

5. Cell Stability With Leakage Reduction Techniques

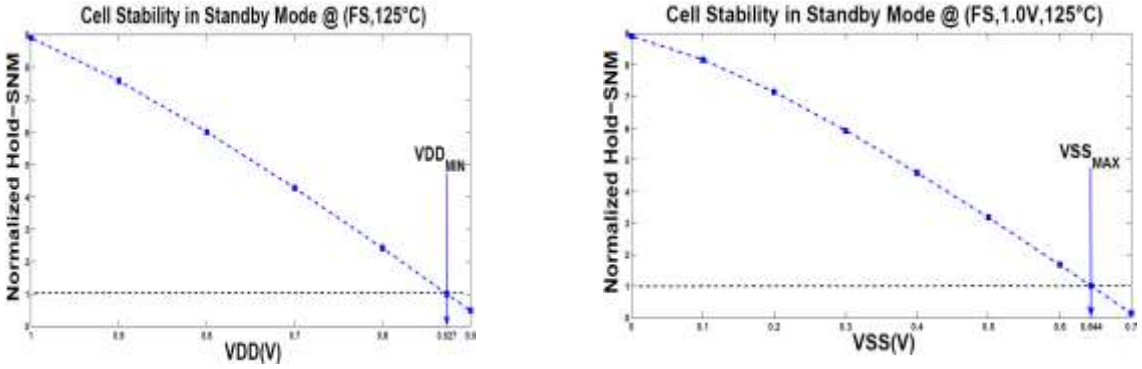
Read SNM and hold SNM of SRAM bitcell are the measures of its stability in respective read and standby modes of the cell [12]. To optimize the yield of memory chip, the impact of process variation on the design metrics should be taken up front during the design phase [17]. In general process variation is divided into two classes: global and local. In case of global process variation, all the devices on a chip are affected in same way, therefore it is not a significant threat to cell stability. Local process variation

introduces the mismatch between the cross-coupled inverters of the cell, which results in significant threat to the cell stability. Intrinsic device variability can be represented in terms of transistor threshold voltage standard deviation σV_T , which is given by the following equation [18].

$$\sigma V_T = 3.19 \times 10^{-8} \frac{t_{ox}.N_A^{0.401}}{\sqrt{L_{eff} \times W_{eff}}} [V] \quad (2)$$

Equation (2) is being used to compute the device mismatch in terms of its threshold voltage standard deviation σV_T . In general there is a trade-off between the improvement of cell standby leakage and cell stability. Also cell stability is critical in case of read mode as compared to standby mode. For standby mode, normalized cell stability of the cell being used here, is the ratio of cell hold SNM to read SNM. To improve the yield of memory chip, we have carried out simulations for SRAM cell stability parameters with each leakage reduction technique under 6σ local variation along with worst process and temperature corner for cell stability (FS, 125°C). With the help of these simulation results we can extract the optimized cell node/nodes voltage for respective leakage reduction techniques.

In Figure 14 (a) and (b), normalized hold SNM for VDDL and VSSR techniques are plotted with VDD and VSS respectively for the bitcell designed in section 3. Thus VDD_{MIN} and VSS_{MAX} of the cell, have been extracted for VDDL and VSSR techniques respectively.



(a) (b)

Figure 14. Normalized Hold SNM w. r. t. Read SNM for (a) VDDL Technique (b) VSSR Technique

In case of BLF technique, hold SNM is not affected by bitline voltage, while with decreasing BL voltage, at the start read SNM of the cell increases and after a certain level of BL drop it starts to decrease. Thus as shown in Figure 15, in order to optimize the leakage of SRAM cell, BL lower side voltage for which read SNM is same as for BL original voltage is selected for the bitcell under investigation.

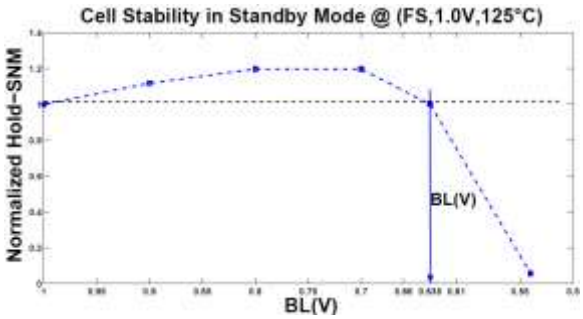
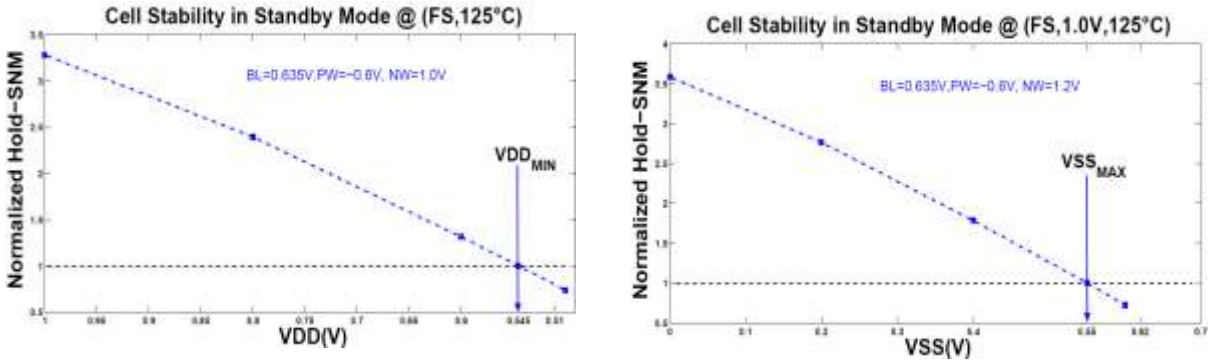


Figure 15. Normalized hold SNM for BLF Technique

Finally, as shown in Figure 16 (a) and (b), for the proposed combined (VDDL+BLF+RBBPW+RBB NW) and (VSSR+BLF+RBBPW+RBBNW) techniques, the optimized cell nodes voltages for leakage reduction of respective techniques have been extracted for the bitcell under investigation.

6. Results and Analysis

In sections 4 and 5, existing as well as proposed cell leakage reduction techniques have been evaluated at the same level of normalized stability for their efficiencies in order to reduce the cell standby leakage. Also as per Table 2, at leakage corner without any leakage reduction technique, subthreshold leakage is the dominant component of cell standby leakage, while GIDL/junction leakage is the recessive component and gate leakage lies in between for the bitcell used in this work. Thus the techniques which are reducing the subthreshold component effectively will be more demanding for SRAM cell standby
leakage reduction.



(a) (b)

Figure 16. Normalized hold SNM for (a) Combined VDDL, BLF and Reverse biased p-well and n-well Technique (b) combined VSSR, BLF and Reverse biased p-well and n-well Technique

As shown in section 4.1, VDDL technique leads to reduction in gate leakage of all the devices in the bitcell effectively, but is not very useful in reducing GIDL/junction leakages. This technique is also reducing I_{SUB} of PD devices significantly but not addressing I_{SUB} of PG devices which are the second dominant leakage component after I_{SUB} of PD devices. Thus VDDL technique demonstrates a significant improvement in SRAM cell standby leakage. In VSSR technique as shown in section 4.2, first two dominant leakage components, I_{SUB} of PD and PG devices are addressed effectively. For

the case of PG1, in addition to significant reduction in V_{DS}, threshold voltage of this device increases due to reverse body bias effect which results in diminishing the I_{SUB} of this device. Similarly for PD2, I_{SUB} effectively decreases but not up to the level in case of PG1 because for PD2, VGS remains same while for PG1 it is also decreasing. In this approach I_{GATE} reduction level is almost equal whatever is in VDDL technique. But here I_{GIDL}/I_J is increasing, thus VSSR technique is more demanding for SRAM cell standby leakage reduction because dominant leakage components are reduced effectively by this technique.

As demonstrated in section 4.3, BLF technique addresses I_{SUB}, I_{GATE} and I_{GIDL}/I_J of access devices of the cell. As discussed in section 4.4, reversing p-well bias approach reduces dominant leakage I_{SUB} of NMOS devices (PD2, PG1) and increases recessive leakage component I_{GIDL}/I_J, similar impact of reversing n-well bias approach is observed for PU1 of the cell. Simulation results discussed in this section also demonstrate significant improvement in cell standby leakage by p-well reverse bias approach as compared to n-well reverse bias approach. As illustrated in section 4.5, combined (VDDL+BLF) and (VSSR+BLF) techniques are more effective in reducing the cell standby leakage as compared to their respective individual techniques.

As demonstrated in section 4.6.1, proposed combined technique (VDDL+BLF+RBBPW+ RBBNW), further reduces the dominant leakage component I_{SUB} of PD, PG and PU devices with respect to (VDDL+BLF) technique. Similarly proposed combined technique (VSSR+BLF+ RBBPW+RBBNW), further reduces the dominant leakage component I_{SUB} of PD and PU devices with respect to (VSSR+BLF) technique. It can be observed from Table 2, that from individual cell leakage reduction approaches with normalized stability equals to 1.0, VSSR emerges the most effective approach to reduce the cell standby leakage since it addresses I_{SUB} of NMOS devices (PG1, PD2) effectively, which is the largest component of SRAM cell standby leakage. With the addition of the BLF technique to it, I_{GATE} and I_{GIDL}/I_J of access devices are also reduced. Now applying reverse bias p-well and n-well approaches to (VSSR+BLF) technique, reduces I_{SUB} of PD2 and PU1 devices further, but increases I_{GIDL}/I_J of PD, PG and PU devices. Thus as shown in Table 2, proposed combined (VSSR+BLF+RBBPW+RBBNW) technique lead to be the best leakage reduction technique for bitcell used in this work.

Table 2. Cell Stability and Leakages with Leakage Reduction Techniques

TECHNIQUES	NORMALIZED HOLD-SNM	JUNCTION LEAKAGE(A)	SUBTHRESHOLD LEAKAGE(A)	GATE LEAKAGE(A)	TOTAL STANDBY LEAKAGE(A)
W/O ANY TECHNIQUE	8.92	1.61E-09	3.23E-07	1.31E-08	3.37E-07
VDDL	1.0	9.84E-10	2.46E-07	2.33E-09	2.49E-07
VSSR	1.0	1.77E-09	2.08E-08	2.22E-09	2.48E-08
BLF	1.0	1.18E-09	5.02E-07	1.22E-08	1.7E-07
RBB-PW	10.8	4.83E-09	7.40E-08	1.37E-08	9.25E-08
RBB-NW	8.49	1.76E-09	2.99E-07	1.31E-08	3.14E-07
VDDL+BLF	1.0	5.56E-10	2.26E-07	1.49E-09	2.28E-07
VSSR+BLF	1.0	1.35E-09	2.08E-08	1.38E-09	2.35E-08
VDDL+BLF+ RBB-PW-NW	1.0	2.52E-09	2.95E-08	1.70E-09	3.37E-08
VSSR+BLF+ RBB-PW-NW	**1.0**	4.70E-09	**1.12E-08**	**1.70E-09**	**1.76E-08**

Table 3. Leakage Components Improvements with Leakage Reduction Techniques

TECHNIQUES	IMPROVEMENT IN CELL LEAKAGE COMPONENTS (%)		
	I_{GIDL}/I_J	I_{SUB}	I_{GATE}
VDDL	38.77	23.75	82.16
VSSR	-10.61	93.54	83.03
BLF	26.61	6.31	6.40
RBB-PW	-200.55	77.07	-5.08
RBB-NW	-4.01	4.74	-0.27
VDDL+BLF	65.43	30.06	88.62
VSSR+BLF	15.88	93.57	89.84
VDDL+BLF+RBB-PW-NW	-56.68	90.86	86.97
VSSR+BLF+RBB-PW-NW	-192.62	96.54	86.95

Also as shown in Table 2, combined leakage reduction technique (VDDL+BLF+RBBPW+RBBNW) is more efficient in leakage reduction as compared to (VDDL+BLF) technique but less efficient as compared to (VSSR+BLF+RBBPW+RBBNW) and (VSSR+BLF) techniques for same normalized stability level equals to 1.0. (VDDL+BLF+RBBPW+RBBNW) technique is more leaky as compared to (VSSR+BLF+RBBPW+RBBNW) and (VSSR+BLF) techniques because

dominant leakage component I_{SUB} of PD and PG devices are not reduced as effectively as in the case of (VSSR+BLF+RBBPW+RBBNW) and (VSSR+BLF) techniques, for the same level of normalized cell stability.

7. Conclusions

In this paper, a 6T SRAM bitcell has been designed in 45 nm CMOS technology node, then a comprehensive study has been carried out to evaluate existing as well as proposed SRAM standby leakage reduction techniques. We conclude that the efficiency of these techniques depends on the composition of the cell standby leakage by its components as well as the impact of respective techniques on stability of the cell. Composition of the cell standby leakage varies with temperature. At leakage corner (FF, 1.0V, 125°C), subthreshold leakage is the dominant component of the cell standby leakage, which is 95.66%. While gate leakage is 3.87%, and GIDL/Junction leakage is 0.48% of cell standby leakage, which is almost negligible component of cell leakage.

As per the performances of these techniques summarized in Table 3, proposed combined (VSSR+BLF+RBBPW+RBBNW) technique is most efficient to reduce the cell standby leakage, which is followed by (VSSR+BLF) and (VDDL+RBBPW+ RBBNW) techniques respectively.

For advanced technology nodes where GIDL/Junction leakage becomes dominant component, (VDDL+BLF) technique is more demanding, where as in the case of gate leakage being dominant both (VDDL+BLF) and (VSSR+BLF) techniques are almost equally efficient.

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