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24GHz CMOS Power Amplifier for Automotive Radar

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Abstract

This paper proposes 24GHz CMOS power amplifier (PA) for the short-range automotive collision avoidance radar. The proposed amplifier is implemented using TSMC 0.13µm RF CMOS technology with f_T/f_{max} of 120/140GHz. It is also powered by a 1.5V supply. The layout optimization technique is used to reduce total die size and parasitic capacitances. To improve power gain of the amplifier, the circuit has a 2-stage architecture and cascode scheme in the first stage. The proposed circuit showed the smallest chip size of 0.25mm^2, the highest power gain of 29.3dB, the lowest power dissipation of 42mW, and the maximum PAE of 18.5% as compared to recently reported research results.

Keywords: *24GHz, CMOS power amplifier, short range automotive collision avoidance radar*

1. Introduction

The increasing demand for low-power and low-cost radio frequency integrated circuits (RF ICs) in millimeter-wave applications requires high-level integration of RF front-end, analog blocks and digital blocks for system-on-a-chip (SoC). The rapid growth in wireless communications has also resulted in a strong motivation toward developing GHz-band high performance RF systems [1]-[11]. The design and implementation of single-chip transceivers has already been demonstrated in CMOS technologies for RF CMOS ICs. These systems have lots of applications such as various portable products, automotive collision avoidance radars, wireless local networks, etc. The unlicensed industrial, scientific, and medical (ISM) frequency band at 24GHz is attractive for commercial, industrial and automotive applications [1]-[8]. For wireless communication circuits, a power amplifier is one of the transceiver's key elements. The 24GHz automotive applications using the standard CMOS technology pose a particular challenge on circuit design because of the high robustness and performance. Numerous publications have reported 24GHz radar in CMOS technology, and active study on 24GHz radar is still underway [1]-[8], [12]-[14].

In this paper, we present a small-area, low power, and high-gain 24 GHz power amplifiers (PA) for the short-range automotive radar. This circuit is fabricated using TSMC 0.13µm RF CMOS process, and it is powered by a 1.5V supply. The proposed circuit is designed using a 2-stage architecture and cascode scheme in the first stage. We

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used the layout optimization technique for 24GHz band to reduce parasitic capacitances.

2. Design and Analysis of Power Amplifier

2.1. Overview of 24GHz Radar

The radar-based autonomous cruise control (ACC) at 77GHz, first introduced from Mercedes-Benz in 1999, is widely available in many high and mid class automotive vehicles. Silicon-based 24GHz short-range automotive radars have been investigated by both industry and academia in the last 20 years [5]-[6], [15]. Most of all, automotive collision avoidance radar using 24GHz band offers safety functions such as pre-crash sensing and collision. Most well known car companies and supplies are already working on the development of the next generation vehicle known as Advanced Safety Vehicle (ASV). Therefore, next generation radars may well be required to support 24GHz band for compatibility and lower overall cost [5]-[9], [15].

The short-range radar (SRR) sensors with coverage up to 30 meters are under development for various further applications. The SRR will be used to expand ACC to stop-and-go operation, to perform pre-crash warning, to act as parking aid, or to warn during backing up or changing lanes [15]. The short range radar sensors can enable a variety of applications such as ACC support with stop and go functionality, collision warning collision mitigation, blind spot monitoring, forward and reverse parking aid, lane change assistant, rear crash collision warning, etc. as described in Figure 1 [15].

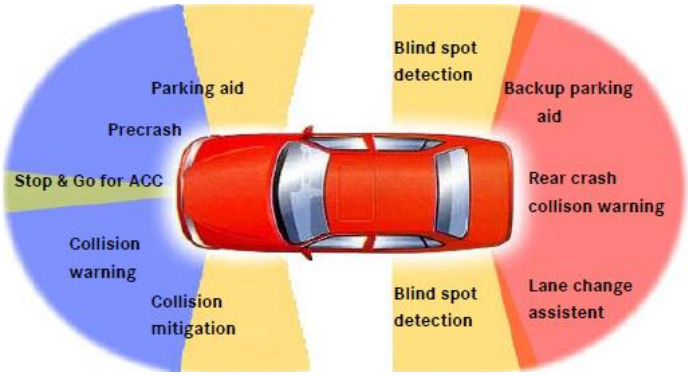

Figure 1. Possible Application for SRR

2.2. Design of 24GHz CMOS Power Amplifier

(1) Design and Analysis

The 24GHz CMOS PA is implemented using TSMC 0.13μm RF CMOS technology. The unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) have 120GHz and 140GHz, respectively. Successful integration of the PA at 24GHz depends on minimization of parasitic capacitances and losses to maintain adequate gain, designing with low voltage swings for low breakdown devices, and achieving sufficient linearity required for spectrally efficient and variable envelope modulation scheme [12]-[14]. Multi-stage PA topologies are essential to obtain high gain at W-band, and it is really true in the case of CMOS technology [12]. It is very important to get high gain, since nanoscale MOSFET is degraded by 3dB due to the limited load impedance that can be realized at the drain output at the high frequency [12].

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Multi-stage PA topologies are essential to obtain high gain at W-band, and this is really true in the case of CMOS technology. It is very important to get high gain, since nanoscale MOSFET is degraded by 3~4dB due to the limited load impedance that can be realized at the drain output at the high frequency and the losses in the matching networks [12]. The optimal distribution of power gain and bias current (and hence P_{1dB}) for the inter-stage of the PA can be obtained using the well-known expression for linearity in a cascaded system as shown in Equation (1).

$$\frac{1}{OP_{1dB\_cascade}} = \frac{1}{OP_{1dB\_3}} + \frac{1}{OP_{1dB\_2}G_3} + \frac{1}{OP_{1dB\_1}G_2G_3} \quad (1)$$

Figure 2 shows the proposed 24GHz CMOS PA. The PA consists of common-source stage with inter-stage conjugate matching operating in Class-A mode, and it is powered by a 1.5V supply. This circuit also has 2-stage cascade structure to achieve higher gain due to the larger output impedance and the alleviated miller capacitance. To input impedance matching, we use inductor L_1 and MIM capacitor, C_1. The inter-stage matching networks are designed using L_2~L_3 and C_2. The L_4 and C_3 are used for output matching network. To reduce RF noise, power supply noise and EMI, we used a decoupling capacitor, C_4. We also realized an optimization technique in width and length of transistors, M_1~M_3.

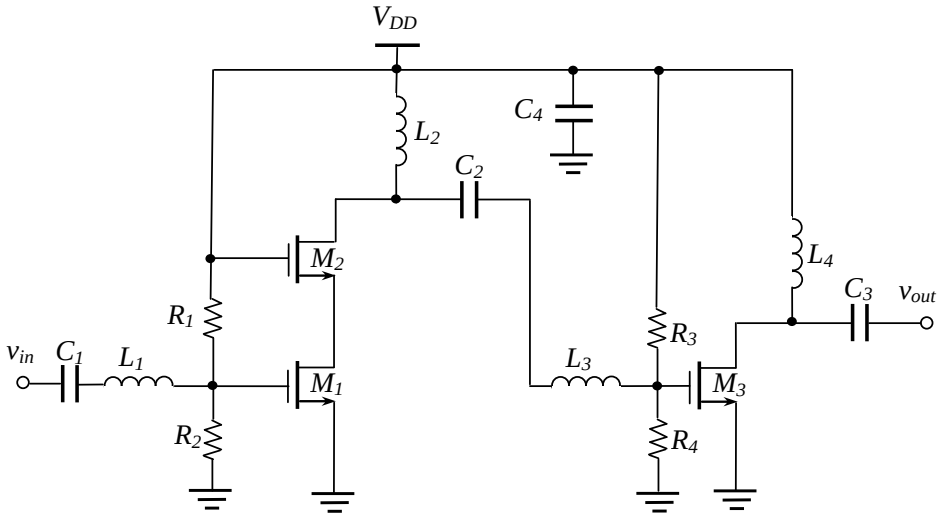


Figure 2. 24GHz CMOS Power Amplifier

(2) Measurement Set-up

Figure 3 shows S-parameter network analyzer measurements for PA Vector network analyzers measure the transmission and reflection characteristics of devices and networks by applying a known swept signal from a synthesized source. Device reflection parameters such as input and output reflection coefficients, return loss, complex impedance, and transmission parameters such as reverse isolation and voltage gain can be measured using the instrumentation. Consider the test set-up for S-parameter measurement shown in Figure 3. It contains vector network analyzer, wafer probe station, DC power supply, digital multi-meter and PC. The wafer probe station has two RF probes to provide RF input powers at ports 1 and 2 of PA, and two DC probes to provide DC power and ground. The measurements have been used here represent 2-port

measurements. These measured values are translated into PA specifications such as input impedance, voltage gain, reflection coefficients and reverse isolation.

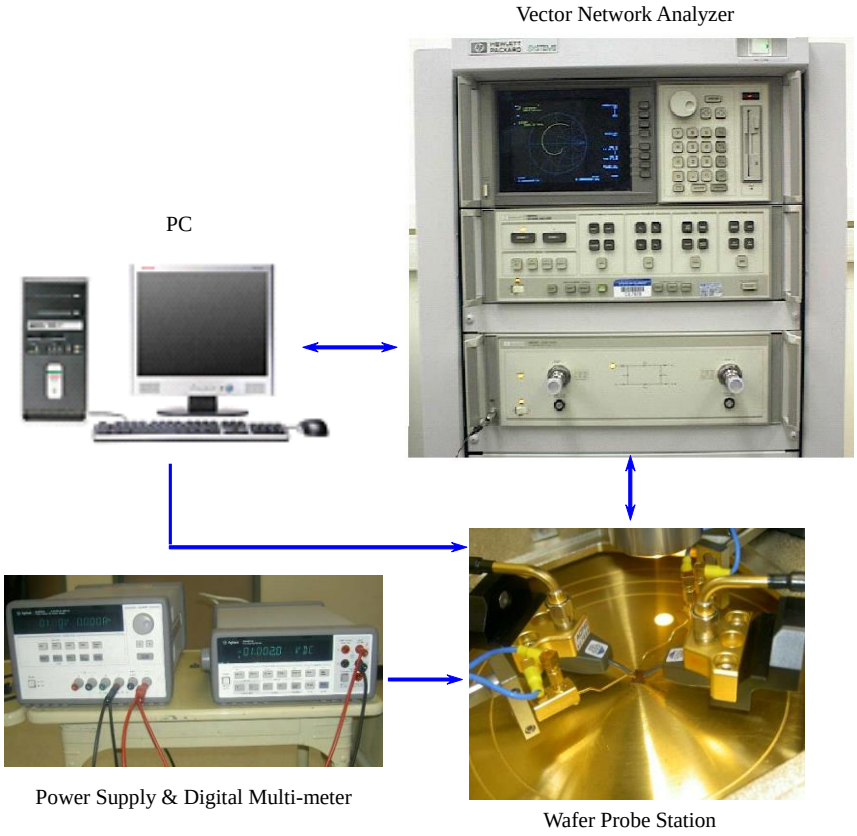


Figure 3. S-Parameter Measurement Set-Up

Figure 4 shows the measurement set-up for the S-parameter of the PA. Vector network analyzer and probe station measure the S-parameter by applying a known swept signal from a synthesized source. The S-parameter measurement has been used here which represent 2-port measurements. The powers of -20dBm are applied from the synthesized sources at both port 1 and port 2. We applied the attentions of 0dB at both port 1 and port 2. The measured S-parameter was transferred to voltage gain, return losses and reverse isolation using conventional equations of ADS or MATLAB tool.

Let's consider Figure 4 with the source (V_{in}) forming part of a network analyzer with a matched load ($Z_L = 50\Omega$) at port 2 to measure transfer function (S_{21}) for the PA. The S_{21} can be obtained by applying an incident wave at port 1, V_1^+, and by measuring the out-coming wave at port 2, V_2^-. This is equivalent to the transmission coefficient from port 1 to port 2. Since S_{21} is a measurement of the gain at the network analyzer output, the transfer function $H(f)$ can be derived to be reference [2].

$$H(f) = S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} . \quad (2)$$

Figure 5 shows simplified high-frequency small-signal model for the input side of the PA. The simultaneous matching including the effect of the load impedance is considered for the simplified small-signal MOS models and inductor model with lossy resistances. The transistor is replaced with hybrid-π model, and the inductor is replaced with series lossy resistance R_L and its inductance L. From hand analysis of the PA, the input impedance, power gain, S11/S12/S22 and transfer functions are obtained.

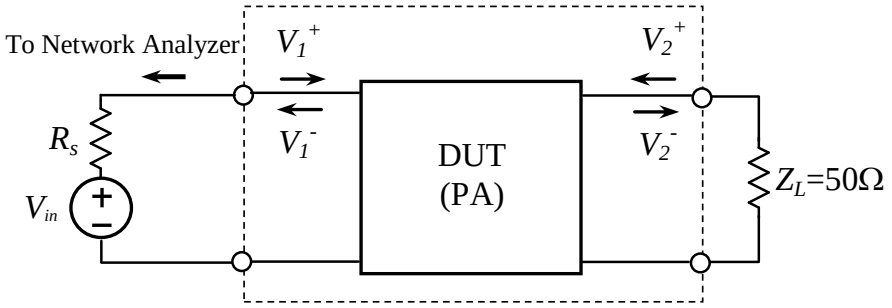


Figure 4. 2-Port Measurement Set-Up

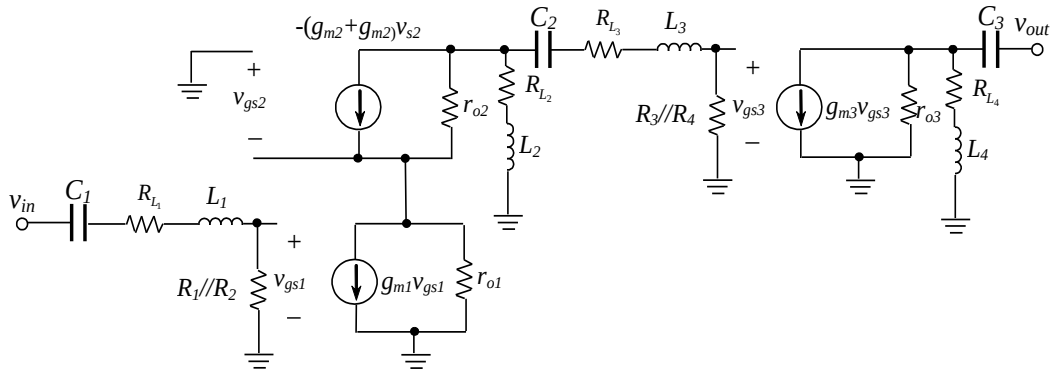


Figure 5. High-Frequency Small-Signal Model for the PA

3. Results

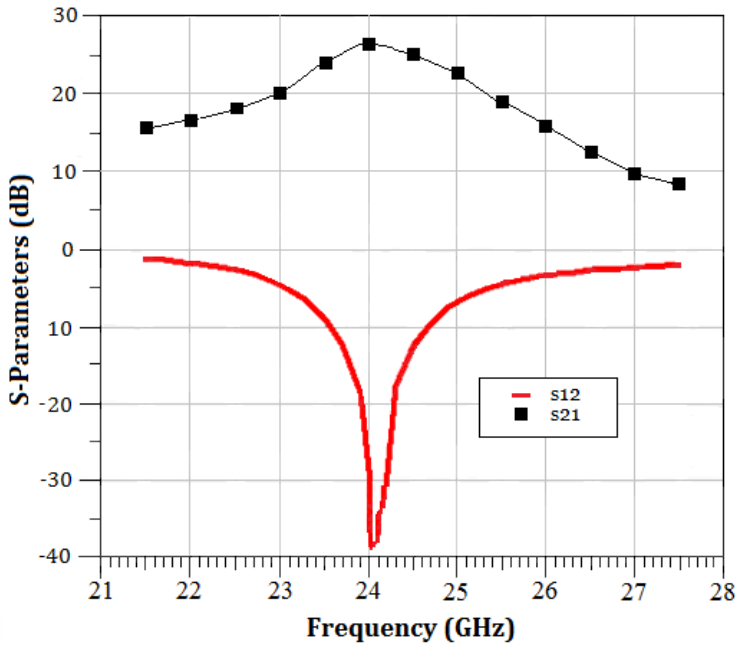
The extracted S-parameter models have been included in circuit simulation using Agilent advanced design system (ADS). The circuit is simulated using Agilent ADS, and full-wave EM analysis is performed for all the passive structures. The speed of the bias mechanism is determined by the bias resistor and gate-source parasitic capacitor at the gate of the lower FET, and the settling time is about 4ns based on the time-domain simulation when the input power of the PA changes from 5 to -5dBm. The amplifier is tested with a power supply of 1.5V, and the DC current drawn without applied RF input signal is 28mA.

The input and output pads are laid out in ground-signal-ground (GSG) configuration, with a pitch of 150μm to do wafer level testing for the PA using a probe station with network analyzer. The measurements for the PA used here 2-port measurements. The measurements are based on a separate PA test chip. The powers of -20dBm are applied from the synthesized sources at both port 1 and port 2. We applied the attenuators of 0dB at both port 1 and port 2. The measured S-parameter was translated into power gain, reflection coefficients (S11/S22), reverse isolation (S12), and input impedance.

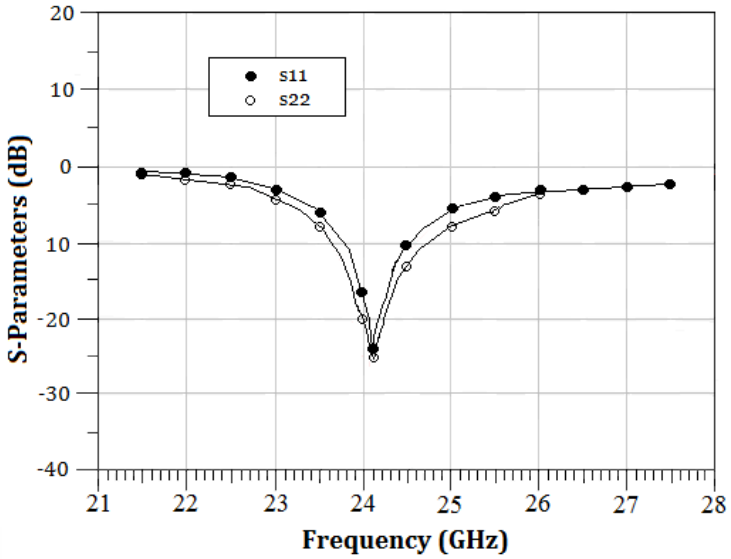
The PA is tested by probing the input and output ports. The input, output and power supply pads are laid out in ground-power-ground (GPG) and GSG configurations with a pitch of 50μm to perform packaged level testing. The power and ground pads are wire-bonded to the testing board.

Figure 6 shows the S-parameter (S11, S12, S21 and S22) of the PA at the frequency range of 21.5 to 27.5GHz. The PA achieves an excellent peak voltage gain (S21) of approximately 26dB at 24GHz, and the S12 indicates that the reverse isolation from the output to the input is also excellent value of approximately –39 dB at 24GHz.

The input reflection (S11) and output reflection (S22) indicate how well the input and output are matched to 50Ω, respectively. The S11 showed excellent value of -24.5dB at 24GHz, but it was not designed for an input match to 50 Ω for the entire 21~28GHz band. It should be noted that the requirement on S11 could be relaxed if the amplifier is integrated with the transmitter stages. Both S11 and S22 are < -5 dB in the range of 21~28GHz.



(a) Reverse isolation and voltage gain



(b) Input and output reflection coefficients

Figure 6. S-parameters for the PA

Figure 7 shows the large signal performance of the PA, where an output 1-dB compression point (OP_{1dB}) of 18dBm and a saturated output power of 22.3dB were obtained at 24GHz with a 1.5V supply. The simulated output power agrees well with hand analysis, which predicts an output P_{1dB} of -12.9dBm. The linearity and gain depends on the bias current of the final stage. Since the PA has available dynamic range, output

power and power gain are changed for the input power. As seen in Figure 7, the PA showed the highest power gain of 29.3dB, and high output 1-dB compression point (OP_{1dB}) of 18dBm at the input 1-dB compression point (IP_{1dB}) of -12.9dBm, respectively. These results verify that the proposed amplifier shows excellent output power and power gain as compared to recently reported results [12]-[14], [16].

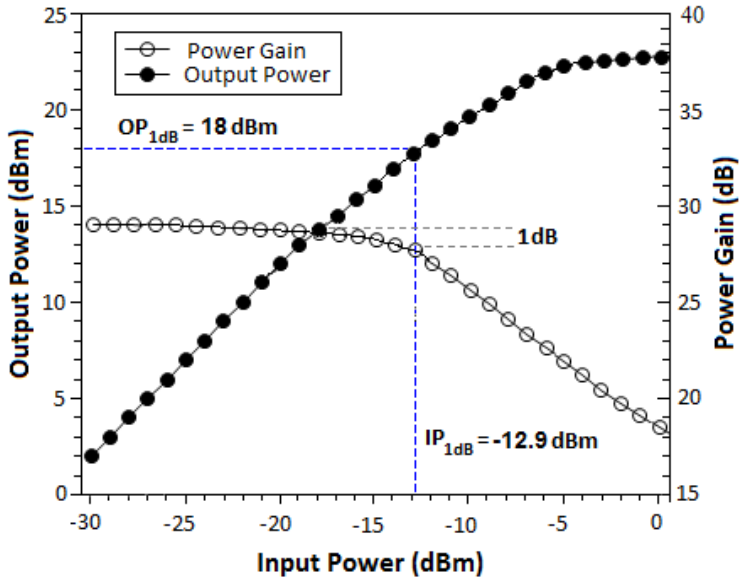


Figure 8. Output Power and Power Gain versus Input Power

Figure 9 shows output power and power-added efficiency (PAE) versus input power at the frequency of 24GHz. The results showed the highest power gain (P_{sat}) of 22.3 dB and the highest maximum PAE (PAE_{max}) of 18.5% as recently reported research [12]-[14], [16]. The proposed PA for automotive radar applications is required to be good phase linearity with small group delay variations to sustain good shaped pulse forms using transmission antenna. The high power gain and high PAE_{max} verify that the proposed PA shows excellent phase linearity.

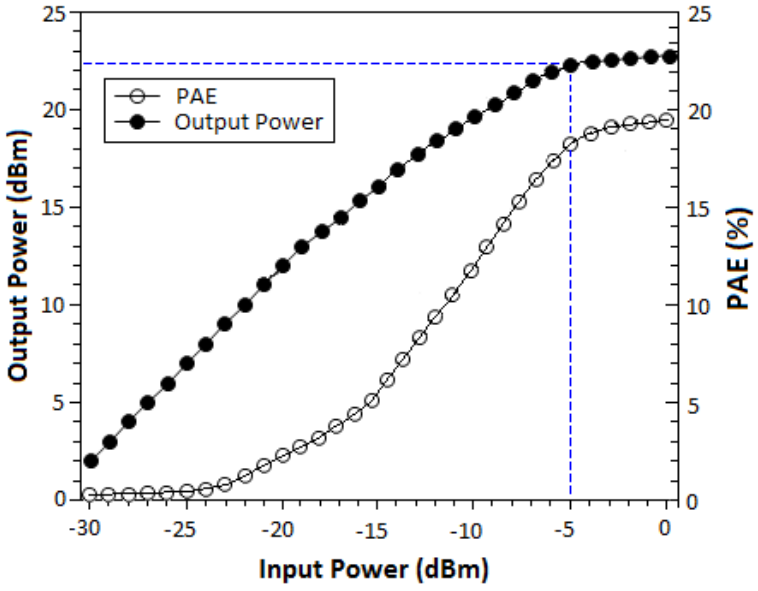


Figure 9. Output Power and PAE versus Input Power

Figure 10 shows power-added efficiency (PAE) and saturated output power (P_{sat}) versus input power when the amplifier is operating under saturated output power condition driven by the -5dBm input. Maximum output power of 20.3dBm (107.2mW) is achieved at 24GHz. At 24GHz, the final gain stage of the power amplifier achieves a maximum output power density (power per source area) of 2mW/μm^2. The PAE exceeds 6% between 20 and 29GHz. The amplifier has power gain of more than 20 dB from 20 to 29GHz with 3dB gain flatness. Over 15dB gain at maximum output power level facilitates integration of the amplifier in a transceiver as fewer pre-driver stages are required. When biased at 14mA (*i.e.*, 50% of 28mA DC current with no RF signal applied), there is less than 3dB reduction in output power and slightly power PAE, despite the transistor trans-conductance g_m being reduced by half for all three stages. As shown in Figure 10, the proposed PA showed a high-saturated output power of 20.3dBm and maximum PAE of 18.5% at the operation frequency of 24GHz, respectively.

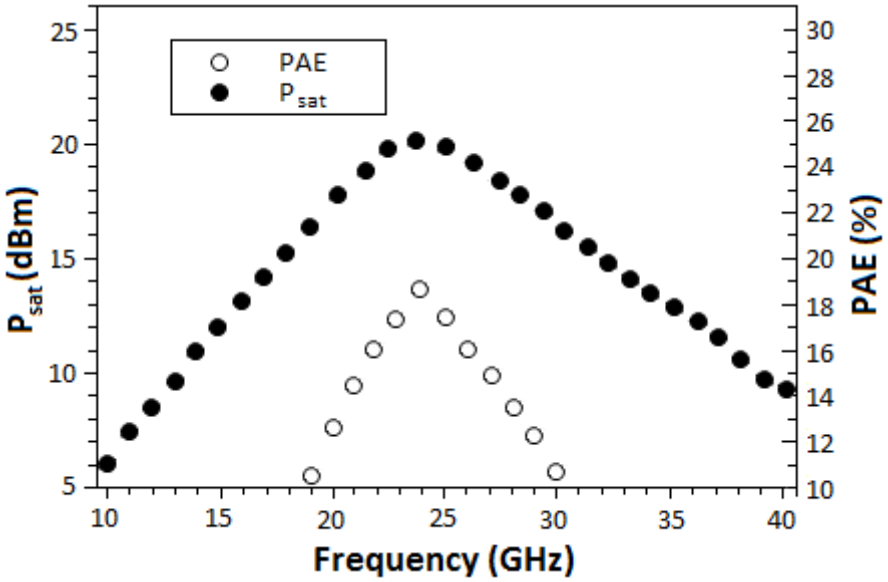


Figure 10. Saturated Power (P_{sat}) and PAE versus Frequency

The complete measured performance comparison of the PA is summarized in Table 1. The circuit correlation function is determined by varying the delay R_x trigger in the pulse generator. Due to the circuit mask constraints at 24GHz, multiple pulses need to be integrated to raise the signal above the noise floor. This is demonstrated in measurement results of Table 1, which shows the integrator output after coherent integration of 100 pulses for each delay setting. A 1ns pulse is generated, corresponding to a 12cm range resolution, and the delay is varied in 100ps steps, corresponding to 2cm range accuracy. As can be seen from this comparison, the proposed CMOS PA showed the highest power gain of 29.3dB, the lowest power dissipation of 42mW, the smallest chip size of 0.25mm^2, the highest saturated power (P_{sat}) of 20.3dBm, and the maximum power-added efficiency (PAE) of 18.5% as compared to recently reported research results. This PA also showed very high output IP3 of 18 dBm, very low input/output reflection coefficients (S11/S22) of -24.5/-25.1dB and very low reverse isolation (S12) of -41.2dB.

4. Conclusions

In this paper, we presented small-area low-power and high gain 24GHz CMOS power amplifier based on automotive collision avoidance radar application. The proposed circuit was fabricated using TSMC 0.13μm RF CMOS technology. The layout techniques for RF circuits were used to reduce parasitic capacitances at the

frequency range of 22~26GHz. The proposed circuit showed the highest power gain of 29.3dB, the lowest power dissipation of 42mW, the smallest chip size of 0.25mm^2, the highest saturated power of 20.3dBm, and the maximum power-added efficiency (PAE) of 18.5% as compared to recently reported research results. This circuit also showed very high output IP3 (OIP3) of 18dBm, very low S11/S22 of -24.5/-25.1dB and very low S12 of -39.2dB.

Table 1. Comparison to Recently Reported 24GHz Power Amplifiers

References / Parameters	[12]	[13]	[14]	[16]	This Work
Process (μm)	0.18	0.18	0.18	0.20	0.13
Frequency (GHz)	24	22	24	24	24
OIP3 (dBm)	7	15.4	14	23	18
Power Gain (dB)	22.8	11.9	7	19	**29.3**
P_{sat} (dBm)	15.9	17.4	14.5	15	**20.3**
DC Power Consumption (mW)	163.8	108	280	939	**42**
S11/S22 (dB)	-14.3/-17	-8/-10	-6.9/-16	-12.4/NA	**-24.5**/**-25.1**
S12 (dB)	-64	NA	-40	-10.5	-39.2
Maximum PAE (%)	14.6	12	6.5	13	**18.5**
Chip Area (mm^2)	0.84	0.4	1.26	6.003	**0.25**

Acknowledgments

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