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Two Dimensional QCA XOR Logic Using NNI Gate

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Abstract

Quantum-dot Cellular Automata (QCA) as a promising nanotechnology to implement digital computing architecture at nano-scale. The QCA based circuits have been implemented and proposed to QCADesigner. XOR gate is an important in encryption operation and error detection. Previous XOR gate used a multi-layer structure in QCA. Multi-layer wire crossing is one of wire crossing techniques. By dividing coplanar circuit to three or more layer, it can reduce area consumption in QCA. However, multi-layer method is difficult to fabricate and has a noise problem in intersection cell. In this paper, we propose two dimensional XOR gate by using Nand-Nor-Inverter (NNI) gate. An NNI gate is used as one of universal gate which can simplify to logic circuits. The proposed design is simulated in QCADesigner tool version 2.0.3.

Keywords*: Nanotechnology, Quantum-dot Cellular Automata, XOR gate, NNI gate, Coplanar wire crossing*

1. Introduction

Since Gordon Moore said that number of transistors on integrated circuits doubles approximately every two years, the reduction of feature sizes and the increase of processing power have been successfully achieved by very large scale integration (VLSI) technology [1]. The microprocessor is one of typical examples, based on VLSI technology, and it is being actively studied in order to increase the integration, performance, efficiency and to minimize the feature sizes [2].

As CMOS devices reach their fundamental limits, they will increasingly suffer from lower design tolerances and fabrication variability, which have negative impacts on reliability and result in increased device failure rates. Some reports of the International Technology Roadmap for Semiconductors (ITRS) indicate that with the current pace of scaling, CMOS technology will encounter serious problems in the next few years. It cannot be further scaled down due to several reasons like high power consumption, short channel effects, expensive lithography, electro migration, heat generation and interconnect delay. Scaling has been the key for having more and more computing power in each new generation of integrated circuits. To keep scaling further down we need to adapt other nanotechnology devices, which can be scaled down to a level way beyond what CMOS can achieve [3].

These future limitations of CMOS have led many to consider novel nanometer-scale devices that are expected to have faster switching speed, lower power consumption, and better scaling characteristic [4]. A quantum-dot cellular automata(QCA) is one of the promising new technologies that not only gives a solution at nano-scale, but also it offers a new method of computation and information transformation [5]. A QCA is the computing with cellular automata composed of arrays of quantum dot devices, and basic concepts of it were introduced by Tougaw and Lent in 1993 [6].

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The QCA concept represents an approach to binary computing which may be more suited to nano-scale implementation than conventional transistors and current switches [7]. QCA based circuits have an advantage of high speed, high integrity and low power consumption and also QCA circuits have an advantage of high parallel processing [8]. Recent work showed that QCA can achieve high density, fast switching speed, and room temperature operation [9, 10]. In recent years, various QCA based combinational circuit designs such as multiplier [11], full adder [12], binary converter [13], full comparator [14], subtractor [15] have been proposed. QCA cell is a basic element, and composed of four dots and two excess electrons. These electrons can tunnel between dots due to columbic repulsion and diagonally occupy corners of the cell, hence leading to two stable arrangements for QCA cell [16]. It is possible to construct majority gate, inverter and logic circuit by arranging QCA cells.

Exclusive-OR (XOR) can be used in error detection and cryptography encryption. Various XOR gate has been proposed but has problem of multi-layer. Multi-layer crossovers are not easy to fabricate due to the multiple layer structure, and the cost to fabricate a multi-layer crossover is expected to be significantly greater than that of a coplanar crossing [17]. On the other hand, most of conventional XOR design proposed smaller and faster circuits by locating input or output location at the internal circuit. It causes scalability problem that needs wire crossing or multi-layer to extend circuits in QCA. In this paper, we propose a QCA structure of the XOR gate using NNI gate.

The paper has been organized in five sections. In Section 2, a brief technical background for QCA operation and previous research on QCA NNI and XOR design are presented. In Section 3, the proposed XOR gate is presented and the properties of the proposed XOR design are discussed. Conclusions are offered in Section 5.

2. Related Work

2.1. QCA Basic

QCA circuit composes of arrays of identical cells, with each cell containing four quantum wells, or dots. Each cell contains two electrons, which are allowed to tunnel between dots but are not allowed to leave the cell. Although QCA cells switch states internally via quantum-mechanical tunneling of electrons between quantum dots, the electronic configuration of a QCA array is determined by the classical Coulombic repulsion between electrical charges [18].

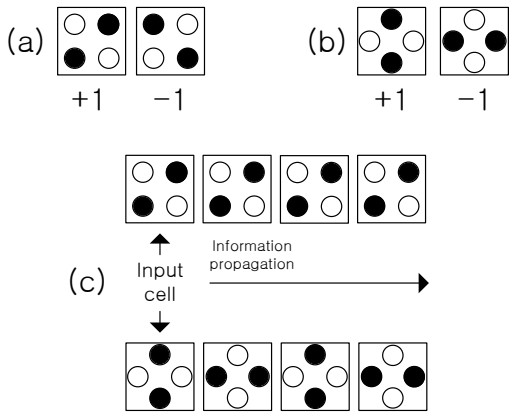

Figure 1. QCA Basic Concept: (a) QCA Standard Cell, (b) 45° Rotated Cell and (c) Two Wires Based Standard Cell and 45° Rotated Cell [19]

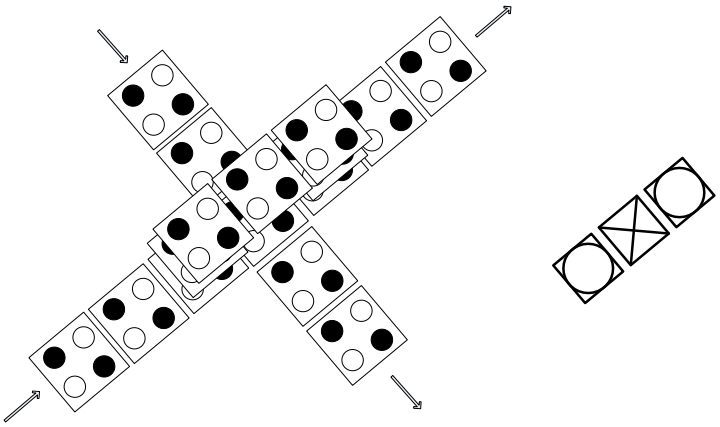

Figure 2. Multi-Layer Wire Crossing

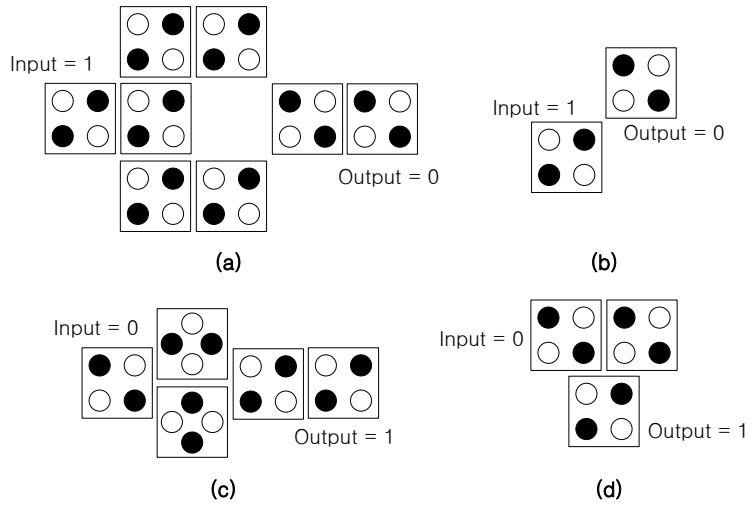

Figure 3. Various Types of Inverter Gate: (a) Robust Inverter, (b) Simplest Inverter, (c) Inverter using 45 Degrees Rotated Cells and (d) Inverter Using Three Cells

Due to Coulomb repulsion, the two excess electrons always occupy diagonally opposite dots as shown in Figure 1 (a). There are two configurations with energetically equivalent polarizations designated as '+1(1)' and '-1(0)'. Tunneling out of a cell is suppressed due to high inter-cell barriers. In a second type of QCA cells, the dots are located at the middle of the sides of cells as shown in Figure 1 (b). 45 degree rotated cells induce the additional space between cells. It significantly decreases the energy separation between the ground state and the first excited state, which degrades the performance of such a device in terms of maximum operating temperature, resistance to entropy, and minimum switching time [20]. The wires constructed using the two types of cells are shown in Figure 1 (c). It is like a contiguous array of QCA cells in physical sense. The effect of applied input signal on the first cell moves to the second and it is polarized by the induced polarity of the first cell, from second cell the effect moves to the third and the polarization moves forward accordingly [21].

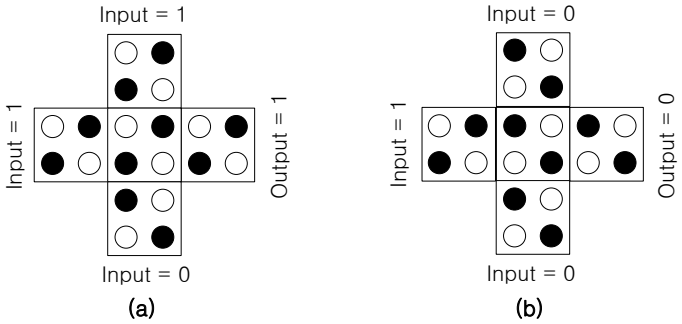

Figure 4. Two Types of Majority Gate: (a) Majority Gate (output is 1) and (b) Majority Gate (output is 0)

Figure 2 shows multi-layer wire crossing. The central part of multi-layer structure, three cells can be represented to the right symbol in QCADesigner. Two cells which include round circle are bridge cells between layers and middle cell is intersection cell. This technique can reduce circuit area however there exists problems that noise problem at intersection cell and fabrication. Four types of QCA inverter are shown in Figure 3. An inverter is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum dots corresponding to different polarizations are misaligned between the cells [5]. Figure 3 (a) shows a robust inverter. By dividing an input to two wires, it can make stronger output signal. Figure 3 (b) is simple inverter and Figure 3 (c) inverter uses 45 degrees rotated cells. Figure 3 (d) uses three cells and makes to propagate signals both horizontal wire and vertical wire.

A majority gate is one of basic building blocks in QCA. Two layouts of a QCA majority gate are shown in Figure 4. A majority gate has three inputs and one output. The output is decided by majority of three input values. Figure 4 (a) shows that two inputs are ‘1’ and one input is ‘0’ so output is ‘1’. Figure 4 (b) also shows output is ‘0’. By fixing the polarization of one input cell, it can be AND or OR gate. If an input cell is fixed to ‘1’, the majority function of two inputs performs as AND gate, and if an input cell is fixed to ‘0’, the majority function of two inputs performs as OR gate.

2.2. QCA Clocking

The adiabatic switching is firstly proposed by Lent *et al*. to remedy the metastable

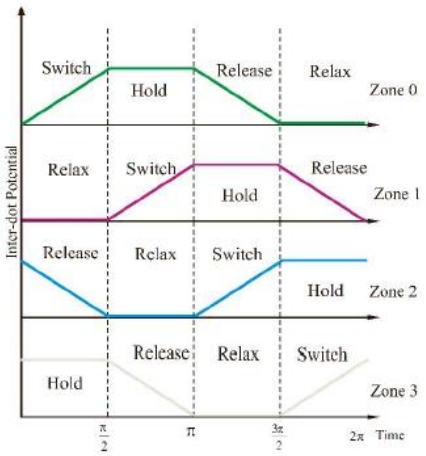

Figure 5. QCA Clocking Phases within Clock Zones

state which was one of the disadvantages of abrupt switching. QCA system will always remain in instantaneous ground state. This kind of switching is achieved by an underlying clocking circuit which needs only the slow discharging and charging of a capacitor [22]. As it is shown in Figure 5, QCA clocking concept can be realized with tracing of four phases (switch, hold, release and relax) over the four clock zones [23]. Considering a 90 degrees out of phase between successive phases, a QCA system is synchronized. In the switch phase, inter dot barriers are steadily raised and the electrons can transfer between dots. By taking a certain polarization value during the hold phase, when the inter-dot barriers are completely high, the cell can only bias the neighboring cells. In the release and relax phases, the cell will lose its polarization [24].

2.3. QCA NNI Gate

An NNI (Nand-Nor-Inverter) gate is a universal gate, and it is possible to perform various functions. This gate is as effective as the AOI gate, and it requires less overhead and variable than the AOI gate using a small space [24]. The logic expression for NNI is drawn in Equation (1) below. QCA NNI gate layout and simulation are shown in Figure 6. There are only four cells and without arranging an intermediate cell of the majority gate, and NNI gate can be performed as a Nand or Nor gate. The NNI function is shown in Table 1. When B = '1', NNI gate performs as a Nand gate and when B = '-1', as a NOR gate.

$$\mathrm{NNI(A,B,C)} = MV(A', B, C') = A'B + BC' + C'A' \quad (1)$$

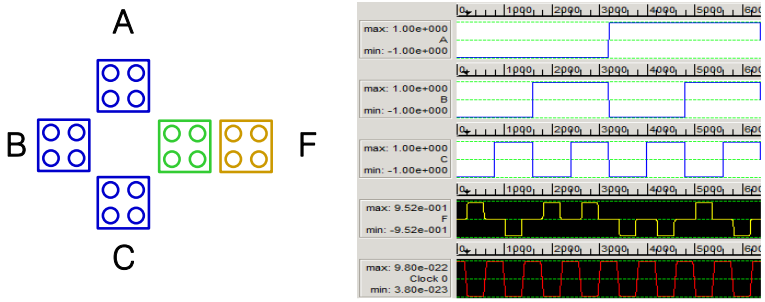

Figure 6. NNI Gate and Simulation Result [25]

Table 1. Function Realized by NNI Gate [25]

Fixed polarization	F	Function
B = 1	(AC)'	Nand
B = -1	(A + C)'	Nor
B = 1, C = 1	A'	Inverter
B = 1, A = 1	C'	Inverter
B = 1, A = C	A'	Inverter
A = C	A'	Inverter
A = B	C'	Inverter
B = C	A'	Inverter
A = -1, C = 1	B	Wire

2.4. Previous XOR Gate

Conventional block diagram and layout of Walus's XOR gate are shown in Figure 7 and Figure 8 respectively [26]. Figure 7 shows a conventional XOR block diagram with OR gate and two AND gates. Input A' and B' of the diagram are inverted values. Walus's QCA XOR gate and its simulation are shown in Figure 8. Walus's XOR gate uses one AND gate and one OR gate. This gate uses multi-layer wire crossing to connect signal to input value. A fixed cell can be used as an AND gate or OR gate. The cell which is fixed to '-1' performs AND gate and affect to both wires propagation. In this result, two AND gates are reduced to one. The multi-layer design can reduce gate and circuit area but it is not easy to fabricate. Walus's XOR uses 83 cells and 4 clocks.

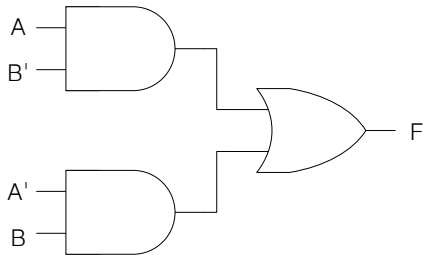

Figure 7. Conventional XOR Block Diagram

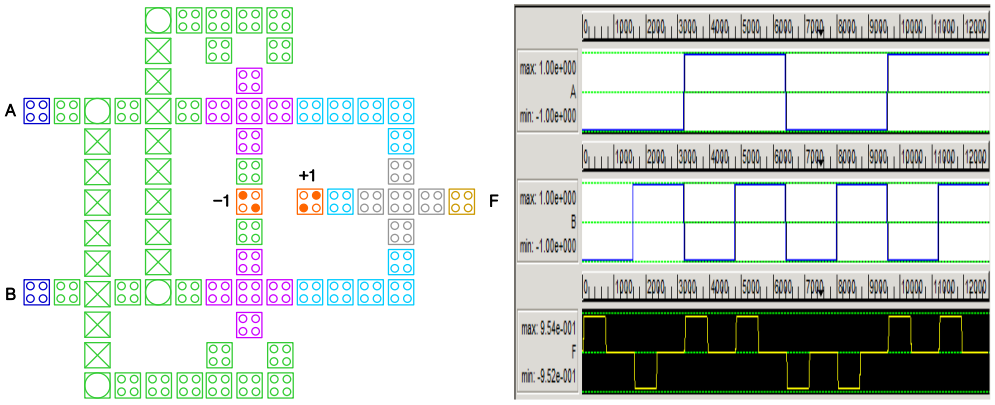

Figure 8. Walus's QCA XOR Gate [26]

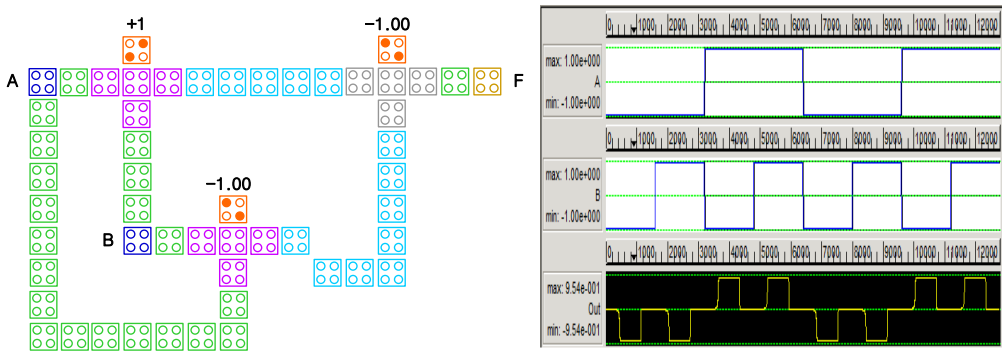

Figure 9. Beigh's QCA XOR Gate [27]

Beigh's QCA XOR gate and simulation shows in Figure 9 [27]. Input A and B are at the corner of wire and propagate signal to different direction. The XOR gate set input B to internal circuit. This method reduces wires but require a crossover in order to connect signal to input B. It is not suitable for large scale circuit design. Beigh's uses 52 cells and 5 clocks.

3. XOR Gate Design using NNI Gate and Analysis

An XOR simple function is $A \cdot \overline{B} + B \cdot \overline{A}$. If we implement XOR using this expression, it needs a combination of AND gates, OR gates, and inverters. In many XOR expressions, we can implement an XOR gate using four Nand gates. The logic expressions for XOR are drawn in Equation (2) below. Figure 10 shows an XOR gate block diagram with two Nand gates and two NNI gates. An XOR gate can implement by four Nand gates and we replace two Nand gates to two NNI gates due to reduction of circuit area. A Nand gate consists of one And gate and one inverter but an NNI gate uses only four cells. Furthermore, it can perform as a Nand gate by fixing one input to value '1' and as part of XOR gate. The output is verified by comparing with truth table as shown 2.

The proposed XOR gate and its simulation result are shown in Figure 11. Each NNI gates has one fixed cell and perform as Nand gates. Two inverters in the XOR gate are in Figure 3 (d). These inverters reduce cell count and area and are suitable for small circuit. Proposed XOR gate uses 28 cells and 4 clocks.

$$\begin{aligned} F_{XOR} &= ((\mathrm{A} \cdot (\mathrm{AB})')' \cdot (\mathrm{B} \cdot (\mathrm{AB})')')' \\ &= \left(A \cdot (A' + B')\right)' \cdot \left(B \cdot (A' + B')\right)' \\ &= ((A' + B) \cdot (B' + A))' \end{aligned} \tag{2}$$

$$= (A + B)(A' + B')$$
$$= A \cdot B' + B \cdot A'$$

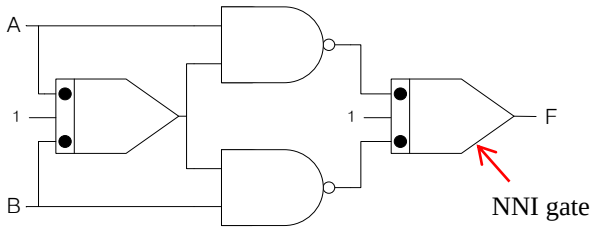

Figure 10. XOR Gate Block Diagram using NNI Gate [19]

Table 2. Truth Table of XOR Gate

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

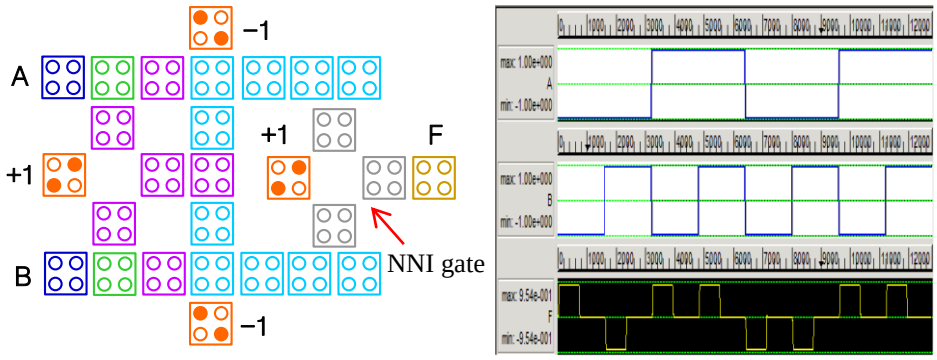

Figure 11. Proposed XOR Gate Using NNI Gates

Table 3 shows comparison of proposed design and previous designs as shown in Figure 8 and Figure 9. Walus's XOR design [26] has 4 clocks delay and uses multi-layer wire crossing so that connects signal to input. A multi-layer wire crossing uses to reduce wire and overall size of circuit but the XOR gate has 83 cells and 63,180nm^2. This circuit size is bigger than other circuits in Table 3. Beigh's XOR gate is coplanar design and has 52 cells and 48,600nm^2. It uses 52 cells but there is unnecessary space. Beigh's XOR requires a crossover wire with more clocks and cells due to connection of input B. Beigh's design [27] has more clocks than other XOR gate in Table 3. The proposed XOR has 4 clocks and smaller cell count and circuit area. Our XOR gate using NNI gates has 28 cells, 19,278nm^2 and shows clear simulation result with strong signal than other previous XOR circuits.

Table 3. Comparison of Logical Structures

QCA circuit	Delay (clocks)	Cell count (cells)	Area (in nm^2)
Walus's XOR[26]	4	83	63,180
Beigh's XOR[27]	5	52	48,600
Proposed XOR	4	28	19,278

4. Conclusions

In this paper, QCA XOR gate is presented using NNI gates. These NNI gates have reduced the area complexity. Our XOR gate needs only four clock phases. Clocking is important in QCA due to circuit computing speed. The area complexity of the proposed gate has much less than typical circuits. We can make ours to extend or connect to other circuit easily. Our circuit compared with other XOR circuits and confirmed in terms of clocks delay, cell count and circuit area. The proposed circuit has been designed and simulated using QCADesigner tool.

Acknowledgments

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